Design Optimization of Multi-Barrier Tunneling Devices Using the Transfer-Matrix Method

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I. Introduction

Multi-barrier tunneling devices propose a possibility to boost the density and performance of non-volatile memory cells. Phase-State Low Electron Device Memory (PLEDM) cells have been presented by Nakazato et al. in [1] and promising results have been reported in [2], [3], [4], and [5]. The principle of a PLEDM is to put a PLED transistor (PLEDTR) on top of the gate of a conventional MOSFET, see Fig. 1. The charge on the Memory Node is provided by tunneling of carriers through a stack of Si_3N_4 barriers sandwiched between layers of intrinsic silicon. Upper and lower barriers prevent diffusion from the poly-Si contacts, while the middle barrier blocks tunneling current in the off-state. In the on-state the energy barriers are heavily suppressed by the voltage on the Word Line, causing tunneling current to flow at the interface to the side gate oxide. Since the charge on the Memory Node is used to control the MOSFET transistor, the cell has gain and only a small charge is necessary to flip the state of the memory cell. The purpose of this paper is to investigate the effects of device design related issues on the performance of such PLEDTR-based memory cells.

II. Tunneling Model

In common device simulators tunneling is usually taken into account by a Fowler-Nordheim analytical formula or a more sophisticated WKB or Gundlach approximation [6]. However, those models are bound to fail for energy barriers which are not of triangular or trapezoidal shape. Additionally, the effect of resonances due to quasi-bound states can only be reproduced within the Gundlach model, but again only for trapezoidal barriers [7]. Thus, the PLEDM device needs a more rigorous approach, including the solution of the Schrödinger equation in the barrier region. Such a solution can be found using the Transfer-Matrix method. This formalism is based on the work of Tsu and Esaki on resonant tunneling diodes, see for example [8]. Descriptions can also be found in [9], [10], and [11]. The main principle is to replace an energy barrier of arbitrary shape by a series of rectangular energy barriers. Following the work of Tsu and Esaki, the tunneling current can be written as

$$J_t = \frac{4\pi m q k_B T}{h^3} \int\limits_{E_{min}}^{\infty} TC(E) \cdot \ln \left[\frac{1 + \exp\left(\frac{E_{f,1}-E}{k_B T}\right)}{1 + \exp\left(\frac{E_{f,2}-E}{k_B T}\right)} \right] dE \qquad (1)$$

where $E_{f,1}$ and $E_{f,2}$ denote the Fermi levels in the Data Line and the Memory Node, respectively. The integration is performed starting from the higher of the two conduction band edges in the Data Line and the Memory Node. The energy barrier is divided into several regions $i = 1, 2, ..., n$ with constant potential V_i. The wave function in each region $\Psi_i(x)$ is written as the sum of an incident and a reflected wave, with A_i and B_i being their amplitudes, and k_i the complex wave number

$$\Psi_i(x) = A_i \exp(jk_i x) + B_i \exp(-jk_i x) \qquad k_i = \frac{\sqrt{2m_i(E - V_i)}}{\hbar}. \qquad (3)$$

The boundary conditions for energy and momentum conservation

$$\Psi_i(x-) = \Psi_{i+1}(x+) \qquad (4)$$

$$\frac{1}{m_i}\frac{d\Psi_i(x-)}{dx} = \frac{1}{m_{i+1}}\frac{d\Psi_{i+1}(x+)}{dx} \qquad (5)$$

yield relations between the wave amplitudes in region n and $n+1$ which lead to

$$\begin{pmatrix} A_n \\ B_n \end{pmatrix} = \underline{T} \cdot \begin{pmatrix} A_1 \\ B_1 \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} \cdot \begin{pmatrix} A_1 \\ B_1 \end{pmatrix} \tag{6}$$

with $\underline{T}$ being the transfer matrix. If it is assumed that there is no reflected wave in region n and the amplitude of the incident wave is unity ($A_1 = 1$ and $B_n = 0$), the tunneling coefficient $TC(E)$ can be written as [10]

$$TC(E) = \frac{k_n(E) \cdot m_1}{k_1(E) \cdot m_n} \cdot |A_n(E)|^2 \tag{7}$$

The main shortcoming of the Transfer-Matrix method is the assumption of vanishing charge density in the barrier regions. The silicon layers are effectively replaced by insulating layers with the band edge energy and permittivity of silicon. This assumption is somewhat justified by the fact that usually, intrinsic silicon is used for the silicon layers between the barriers [5]. The self-consistent contribution from the carrier charge in the insulating layers is also neglected. Only [12] gives an expression for the electron density for quasi-bound states within oxides for the case of an applied bias using the Green function formalism. Problems arise from the fact that there is no clear defined Fermi energy in the barrier region. In resonant tunneling diodes, this problem is usually solved by assigning either the left or the right Fermi level to each region. However, this choice is somewhat arbitrary and so will be the results [11]. Despite these apparent drawbacks, the Transfer-Matrix method is usually the method of choice to simulate tunneling in multi-barrier structure, see for example [13], where it has successfully been applied to study the characteristics of a InGaP/GaAs resonant tunneling bipolar transistors, or [5] where Mizuta et al. calibrated a conventional drift-diffusion simulator to the results of Transfer-Matrix simulations.

III. Simulation Results

We used the results of [5] for a single Si_3N_4 barrier diode to calibrate our simulator and found good agreement to their data, see Fig. 2. Fig. 3 and 4 show plots of the transmission coefficient and the electron wave function for a certain energy level at an applied voltage of the Word Line of 2V. It can be seen that there are various resonances which correspond to quasi-bound states within the energy wells. These resonances contribute heavily to the total current and must be resolved with high accuracy. An energy grid in the range of peV has to be used in these regions. Electron and hole tunneling processes have been considered, where electron and hole masses of 0.5 m_0 and 0.8 m_0 have been used. The Si_3N_4 barrier was modeled with a barrier height of 5eV and a conduction band offset of 2eV to the Si conduction band edge with the dielectric permittivity being 7.5.

We investigated the effect of the position and size of the central shutter barrier as well as the effect of shrinking the stack width on the $I_{\text{on}}/I_{\text{off}}$ ratio of the device. We assumed two cell states: an on-state with 3V applied on the Data Line and the Word Line, and an off-state with 0.8V applied on the Memory Node and 0V on the Word Line. The PLEDTR had a stack width of 180nm and a stack height of 100nm. The thickness of the upper and lower barriers was set to 2nm. The thickness of the side gate oxide was 3nm.

A. Position and Thickness of the Central Shutter Barrier (CSB)

Fig. 5 and Fig. 6 show the effect of different Central Shutter Barrier thicknesses. While the on-current is hardly influenced by the different thicknesses, the off-current is very sensitive to it. Also, the position of the CSB is critical, because for a CSB located near the memory node, the energy barrier will be reduced in the off-state by the charge on the memory node. If, on the other hand, the CSB is placed near the Data Line, the energy barrier is not suppressed and the off current is much lower. The effect on the on-current is visible, but much lower as compared to the off-current. Such an asymmetry in the I-V characteristics for asymmetric source and drain barrier arrangements has already been experimentally observed by [5].

B. Width of the Barrier Stack

In [14] the feasibility of very narrow silicon-insulator stacks is shown. We investigated the effect of shrinking the stack width on the device performance. Fig. 7 and Fig. 8 show simulation results for a stack width of 140 nm down to below 20nm. It can be seen that the $I_{\mathrm{on}}/I_{\mathrm{off}}$ characteristics is greatly improved by the decreasing width. The current in the on-state, which mainly floats as a surface current near the Word Line, is not reduced by the decreased area. It even increases for very low stack widths. The off-current, on the other hand, is directly proportional to the stack area and can be significantly suppressed by shrinking the stack width.

IV. Conclusion

We show quantum-mechanical simulations of a recently proposed PLEDM multi-barrier tunneling device by incorporating the Transfer-Matrix formalism into the two-dimensional device simulator MINIMOS-NT. Simulation results showed that the device performance in terms of the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio can be optimized by choosing a proper arrangement of the barriers. In particular, placing the central shutter barrier near the Data Line gives better performance independent of the barrier thickness. The reason is that in the off-state, the voltage at the memory node reduces the barriers near the memory node, while it has hardly any influence on the barriers near the Data Line. The performance can also be increased by shrinking the stack width. Reducing the stack width leads to lower off-current, but hardly influences the on-current. The on-current flows only at the interface to the side gate oxide, while the off-current flows through the whole stack area. An on-current of 10^{-7}A and an off-current of as low as 10^{-38}A can be reached, values which well correspond to results reported in [2].

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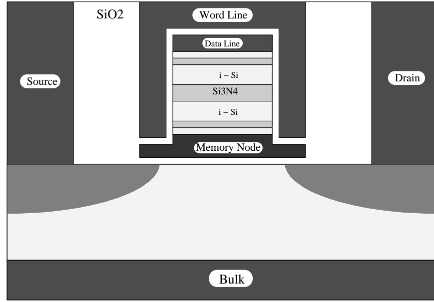

Fig. 1: The PLEDM device.

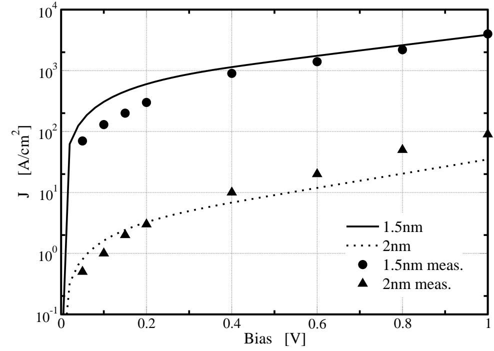

Fig. 2: Calibration to literature data.

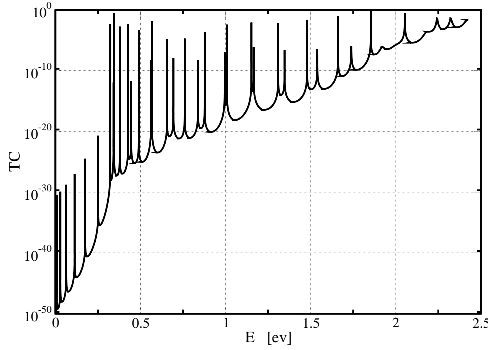

Fig. 3: Transmission coefficient.

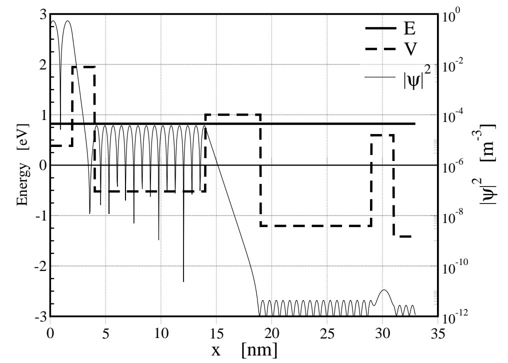

Fig. 4: Electron wave function.

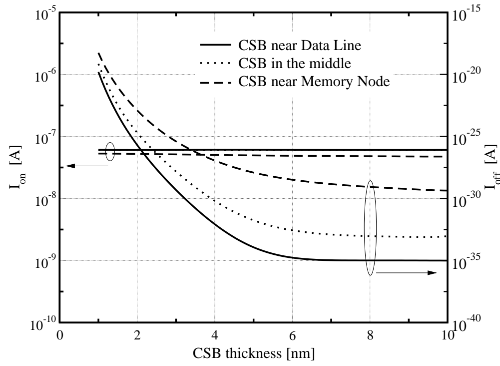

Fig. 5: I_{on} and I_{off} for different CSB thicknesses.

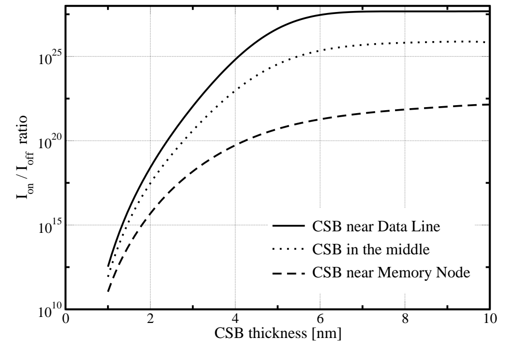

Fig. 6: $I_{\mathrm{on}}/I_{\mathrm{off}}$ for different CSB thicknesses.

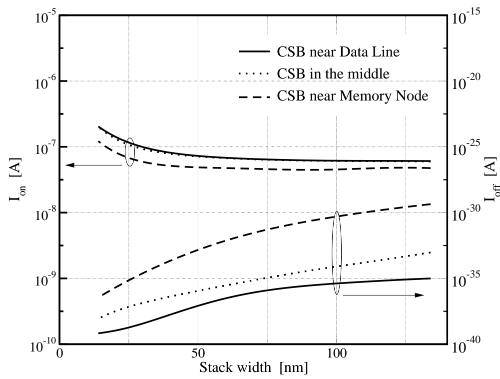

Fig. 7: I_{on} and I_{off} for different stack widths.

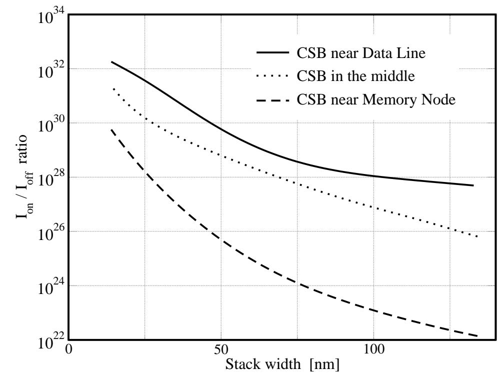

Fig. 8: $I_{\mathrm{on}}/I_{\mathrm{off}}$ for different stack widths.