Numerical Study of Partial-SOI LDMOSFET Power Devices

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I. Introduction

Smart power ICs, which monolithically integrate low-loss power devices and control circuitry, have attracted much attention in a wide variety of applications [1], [2]. Commonly used smart power devices are the LDMOS and LIGBT implemented in bulk silicon or SOI (Silicon on Insulator). One of the key issues in the realization of such 'smart power' technology is the isolation of power devices and low-voltage circuitry. SOI technology consistutes an attractive alternative to the traditional junction isolation. When high-voltage devices over 100 V are integrated on an SOI wafer, the isolation area between devices shrinks and lower leakage currents result in greatly improved high temperature performance. In general the breakdown voltage of an SOI structure is a function of the thickness of the silicon and the buried oxide layer [1]. The buried oxide helps to sustain a high electric field which results in a higher breakdown voltage. However, the operation of SOI power devices is limited by self-heating effects during switching and some fault conditions such as short circuit. Since the buried oxide underneath the device is a good thermal insulator, the temperature rise inside SOI power devices can be much higher than that of bulk silicon devices. Self-heating of SOI power devices can result in serious reliability problems during operation in a high temperature environment. To solve this problem, partial-SOI (P-SOI) technology was suggested [3], [4], where a silicon window helps to reduce self-heating. In addition, potential lines spread into the substrate. Therefore it is possible to obtain higher breakdown voltages than those of conventional SOI devices, because the depletion layer in the substrate supports some voltage. This paper discusses the dependence of the breakdown voltage and temperature distribution on the location of the silicon window. We numerically confirm that the breakdown voltage of P-SOI LDMOSFET with a silicon window under the source is higher than that of P-SOI LDMOSFET with a silicon window under the drain.

II. Device Structures

The schematic cross sections of the simulated devices are shown in Fig. 1 to Fig. 3. Fig. 1 shows a conventional SOI LDMOSFET designed for breakdown voltage of 300 V with an SOI thickness t_{soi} of 7 μm and with a buried oxide thickness t_{ox} of 2 μm. The 20 μm drift region of the device is doped according to the RESURF principle [1] to achieve a maximum breakdown voltage. P-SOI LDMOSFETs with the silicon window under the drain and under the source are shown in Fig. 2 and Fig. 3, respectively. The t_{soi} and t_{ox} of the P-SOI LDMOSFETs are the same as those of the conventional SOI LDMOSFET shown in Fig. 1.

III. Simulation Results

The potential distribution of the conventional SOI LDMOSFET and the P-SOI LDMOSFETs at breakdown are shown in Fig. 1, Fig. 2, and Fig. 3, respectively. In the conventional SOI LDMOSFET, the buried oxide supports large voltage, and it prevents potential lines from spreading into the substrate. In the case of the P-SOI LDMOSFET, however, potential lines spread into the substrate. As shown in Fig. 2, the potential distribution of the P-SOI LDMOSFET with the silicon window under the drain is similiar to that of standard junction isolation devices. Part of the voltage will be supported by the depletion layer in the substrate region. However, the buried oxide layer does not affect the breakdown voltage in this structure. In the P-SOI LDMOSFET with the silicon window under the source (Fig. 3) the potential distribution in the buried oxide layer is similiar to that of the conventional SOI LDMOSFET, so the buried oxide layer helps to increase the breakdown voltage. In addition, the temperature rise due to self-heating is reduced by the silicon window in the

P-SOI LDMOSFETs. Two-dimensional numerical simulations with MINIMOS-NT [5] have been performed to investigate the influence of the window on the breakdown voltage and on self-heating effects.

A. Breakdown Voltage of P-SOI LDMOSFETs

The simulated breakdown voltages of P-SOI LDMOSFETs as a function of the substrate doping concentration C_{sub} are shown in Fig. 4. The breakdown voltage increases with increasing C_{sub} for the P-SOI with the silicon window under the drain, because the RESURF condition of the SOI structure is affected by C_{sub}. The solid lines in Fig. 5 show the electric field strength near the surface with different substrate doping levels. The figure shows that the RESURF condition strongly depends on C_{sub} in this structure. Further increased C_{sub} reduces the depletion layer width in the substrate region which decreases the breakdown voltage (solid line in Fig. 4). The buried oxide layer does not affect the voltage in this structure. Breakdown voltages versus buried oxide layer length and n-drift layer length L_{d} are shown in Fig. 6 and Fig. 7, respectively. The maximum breakdown voltage of this structure is 355 V at $C_{\mathrm{sub}} = 6 \times 10^{14}$ cm^{-3} and $L_{\mathrm{d}} = 25$ μm. The improvement in the voltage handling capability is about 18%. In the P-SOI with silicon window under the source, the RESURF condition does not depend on the substrate doping concentration as shown by the dashed lines in Fig. 5. However, the breakdown voltage decreases slowly with increasing C_{sub} because of the reduced depletion layer width in the substrate region. As shown in Fig. 7, the maximum breakdown voltage of 397 V is obtained at $C_{\mathrm{sub}} = 3 \times 10^{14}$ cm^{-3} and $L_{\mathrm{d}} = 30$ μm. The improvement in the voltage handling capability is about 32% compared to the conventional 300 V SOI LDMOSFET. Because the buried oxide and the depletion layer in the substrate region support the voltage, a higher breakdown voltage is obtained in this structure compared to that of the P-SOI with the silicon window under the drain.

B. Temperature Dependence of the Device Characteristics and Self-Heating

Fig. 8 shows the leakage currents of P-SOI LDMOSFETs versus drain voltage as a function of the lattice temperature. The leakage current increases nearly exponentially with increasing temperature [6], because the space charge generation rate follows the intrinsic carrier density n_i. The shape of the leakage current does not change significantly with temperature, but the breakdown voltage increases. The increase of breakdown voltage is caused by the reduction of the mean free path of the carriers due to lattice scattering. As shown in Fig. 9, the breakdown voltage shows a similar temperature dependence to conventional SOI LDMOSFETs but for P-SOI LDMOSFETs the slope is somewhat larger. This means that breakdown voltage characteristics of P-SOI LDMOSFETs are between SOI and junction isolated devices. The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI LDMOSFETs [7]. In majority carrier devices such as MOSFETs, there is very little carrier recombination and as a result heat generation is mainly caused by Joule heating. This effect can be seen on SOI LDMOSFET and it is proportional to the local resistances of the n-drift and channel region. Fig. 10 and Fig. 11 show the temperature distributions inside the P-SOI LDMOSFETs with an applied gate voltage V_{G} of 15 V and a drain-source voltage V_{DS} of 10 V. The bottom of the devices is assumed to be isothermal at 300 K. To reduce the simulation time, a substrate thickness of 36 μm is used. In these structures, the silicon window acts as a good thermal conductor. In the P-SOI LDMOSFET with the silicon window under the drain, the temperature rise is highest in the gate region (310 K, white region in the figure) and decreases towards drain (308 K) as shown in Fig. 10. In the case of the P-SOI LDMOSFET with the silicon window under the source, the temperature rise is highest in the drain region (312 K) of the drift layer and decreases towards gate and source (307 K) as shown in Fig. 11. Fig. 12 shows a comparison of the temperature versus lateral distance under the surface for the conventional SOI LDMOSFET and the P-SOI LDMOSFETs. This figure shows that the silicon window in the P-SOI drastically reduces the temperature rise due to self-heating.

IV. Conclusion

We discussed the breakdown voltage and temperature dependence of partial-SOI (P-SOI) LDMOSFETs in terms of different locations of the silicon window. Our simulations confirmed that the breakdown voltage and self-heating effect of the P-SOI with the silicon window under the source are better than those of P-SOI with the silicon window under the drain. For the P-SOI LDMOSFET ($t_{\mathrm{soi}} = 7\ \mu$m and $t_{\mathrm{ox}} = 2\ \mu$m) with the silicon window under the drain, a maximum breakdown voltage of 355 V is obtained at $C_{\mathrm{sub}} = 6 \times 10^{14}$ cm^{-3} and $L_{\mathrm{d}} = 25\ \mu$m. For the P-SOI LDMOSFET with the silicon window under the source, a maximum breakdown voltage of 397 V is obtained at $C_{\mathrm{sub}} = 3 \times 10^{14}$ cm^{-3} and $L_{\mathrm{d}} = 30\ \mu$m. The improvement in the voltage handling capability is about 32% compared to conventional 300 V SOI LDMOSFET. Since the buried oxide and the depletion layer in the substrate region support the voltage, a higher breakdown voltage is obtained in this structure compared to that of a P-SOI with a silicon window under the drain.

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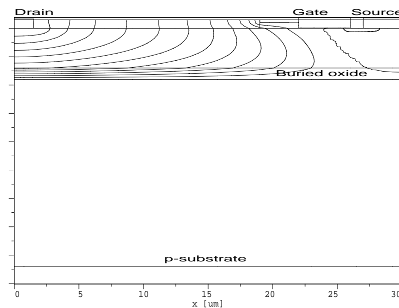

Fig. 1. Potential distribution of conventional SOI LDMOSFET.

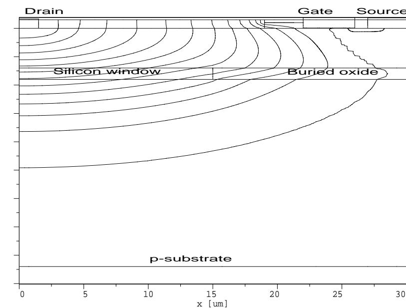

Fig. 2. Potential distribution of P-SOI LDMOSFET (Silicon window: Under drain).

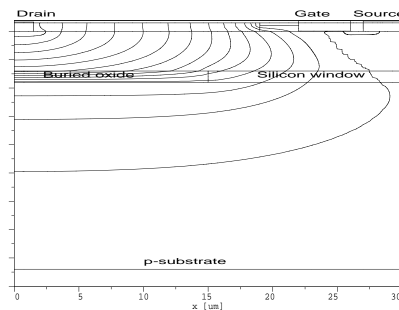

Fig. 3. Potential distribution of P-SOI LDMOSFET (Silicon window: under source).

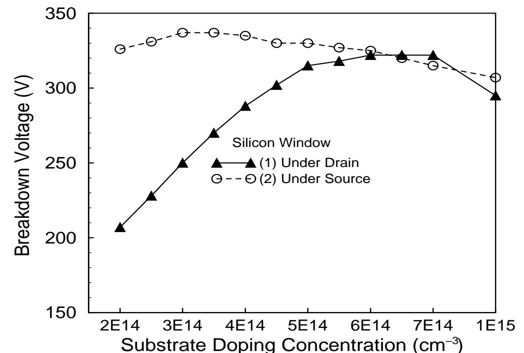

Fig. 4. Breakdown voltage versus substrate doping concentration of P-SOI LDMOSFETs (L_{d}=20 μm).

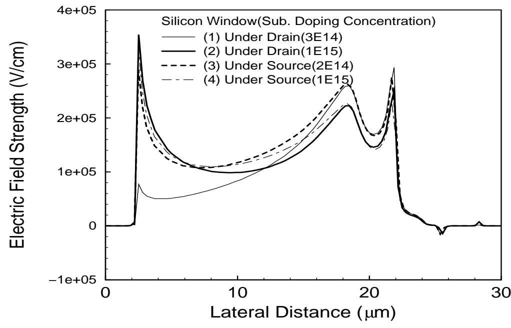

Fig. 5. Surface electric field strength for the two different silicon window positions.

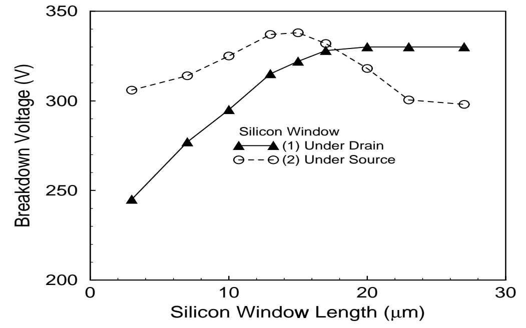

Fig. 6. Breakdown voltage versus buried oxied layer length (L_d=20 μm).

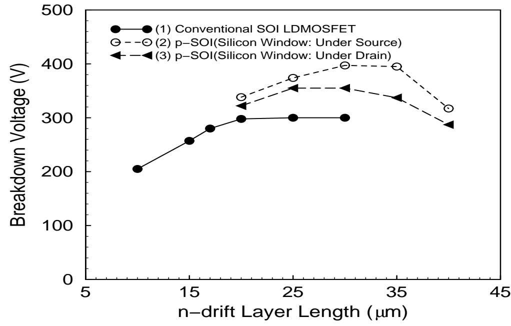

Fig. 7. Breakdown voltage versus n-drift layer length.

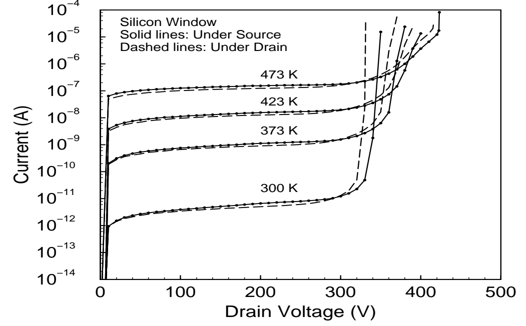

Fig. 8. Leakage current versus lattice temperature of P-SOI LDMOSFETs.

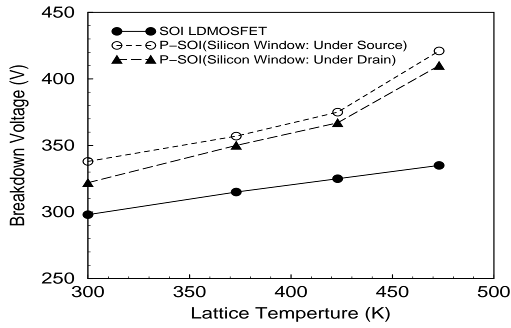

Fig. 9. Breakdown voltage versus lattice temperature (L_d=20 μm).

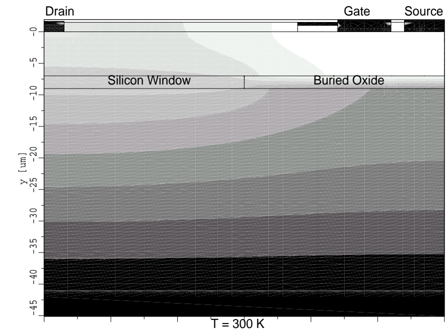

Fig. 10. Temperature distribution of a P-SOI LDMOSFET (Silicon window: under drain).

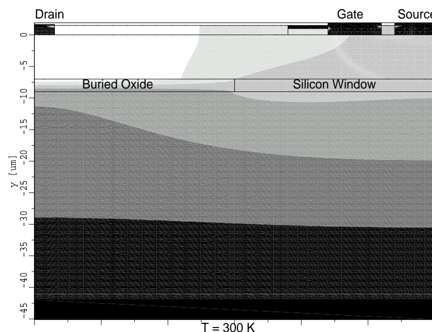

Fig. 11. Temperature distribution of a P-SOI LDMOSFET (Silicon window: under source).

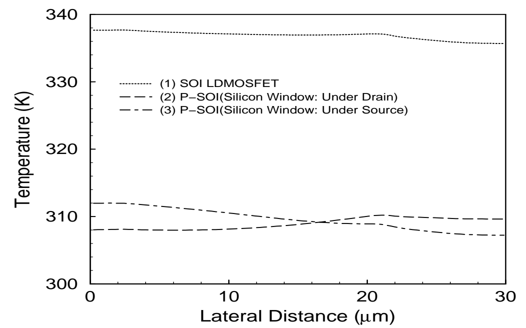

Fig. 12. Temperature versus lateral distance under top surface of the SOI structures.