Industrial Application of Heterostructure Device Simulation

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Invited Paper

***Abstract*—We give an overview of the state-of-the-art of heterostructure RF-device simulation for industrial application based on III–V compound semiconductors. The work includes a detailed comparison of device simulators and current transport models to be used, and addresses critical modeling issues. Results from two-dimensional hydrodynamic simulations of heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs) with MINIMOS-NT are presented in good agreement with measured data. The simulation examples are chosen to demonstrate technologically important issues which can be addressed and solved by device simulation.**

***Index Terms*—Heterojunction bipolar transistors, high electron mobility transistors, semiconductor device modeling, semiconductor heterojunctions, simulation software.**

I. Introduction

HETEROJUNCTION bipolar transistors (HBTs) and high electron mobility transistors (HEMTs) are among the most advanced semiconductor devices. They match well today's requirements for high-speed operation, low power consumption, high-integration, low cost in large quantities, and operation capabilities in the frequency range from 0.9 to 215 GHz. HBT ICs are used for microwave power and low power wireless communications applications, hand held communication, and high-speed digital data transmission. HEMT ICs are used for local multi-point distribution services for broadband Internet access (LMDS), for automotive cruise control (ACC) radar, and high speed transmission (40 Gbit/s and beyond).

The paper gives a review of state-of-the-art device simulators, including the two-dimensional (2–D) device simulator MINIMOS-NT, discusses critical modeling issues regarding the simulation of advanced III–V semiconductor devices, and concludes with particular simulation results of such devices obtained with the same simulation tool, model set, and set of model parameters. Using examples from an industrial vendor, we demonstrate how such a well-calibrated tool can address technologically important issues, such as process variations or reliability.

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With the shrinking of device dimensions and the replacement of hybrid mounted transistors by MMICs in mass production [1], device simulations and circuit simulations with distributed devices need to be carried out by state-of-the-art tools, accounting for physical effects on a microscopic level. Several questions during device fabrication, such as device optimization and process control, can today be addressed by device simulation.

To enable predictive simulation of semiconductor devices proper models describing carrier transport are required. The drift-diffusion (DD) transport model [2] is by now the most popular model used for device simulation. However, with down-scaling the feature sizes, nonlocal effects become more pronounced and must be accounted for by using an energy-transport (ET) or hydrodynamic (HD) transport model [3]. During the last two decades Monte-Carlo (MC) methods for solving the time-dependent Boltzmann equation have been developed [4], [5] and applied for device simulation [6]–[8]. However, the MC algorithms encounter serious difficulties when applied to the extreme conditions occurring in the advanced semiconductor devices. Thus, reduction of computation time is still an issue and, therefore, the MC device simulation is still not feasible for industrial application.

II. RF-Device Simulators

Several commercial tools, e.g., [9], [10], and university-developed simulators, e.g., [11], [12], have been successfully employed for device engineering applications. However, most of them were focused on silicon-based devices. In contrast to the silicon industry, where process-, device-, and interconnect-simulation tools form a continuous virtual workbench from material analysis to chip design, III–V simulation is mainly focused on device and circuit aspects. The latter is accompanied by few examples for MESFET technology simulation tools developed in parallel to SUPREM, e.g., [13]. For heterojunction devices due to the extensive number of process steps, device simulation is focused on process control and inverse modeling, e.g., of geometry and doping profiles.

A common feature is the lack of a rigorous approach to III–V group semiconductor materials modeling. As an example, modeling of AlGaAs, InGaAs, or even InAlAs and InGaP is restricted to slight modifications of the GaAs material properties.

Another common drawback is the limited feedback from technological state-of-the-art process development to simulator development. Critical issues concerning simulation of

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heterostructures are mostly not considered, such as interface modeling at heterojunctions and insulator surfaces, as well as hydrodynamic and high field effects modeling: carrier energy relaxation, impact ionization, gate current modeling, and selfheating effects.

The 2-D device simulator PISCES [11], developed at the Stanford University, incorporates modeling capabilities for GaAs and InP based devices. One of its many modifications G-PISCES from Gateway Modeling [13] has been extended by a full set of III–V models. Examples of MESFETs, HEMTs, and HBTs for several material systems, e.g., InAlAs/InGaAs, AlGaAs/InGaAs, AlGaAs/GaAs, and InGaP/GaAs HBTs are demonstrated. Disadvantage of this simulator is the lack of appropriate ET or HD transport model, necessary to model high-field effects, in comparison to the original version of PISCES.

The device simulator MEDICI from Avant! [14], which is also based on PISCES, offers simulation capabilities for SiGe/Si HBTs and AlGaAs/InGaAs/GaAs HEMTs. Advantages of this simulator are HD simulation capabilities and the rigorous approach to generation/recombination processes. In addition, recently an option treating anisotropic properties was announced. Next to III–V materials modeling this simulator has weaknesses in the interface modeling and in the capabilities of mixed-mode device-circuit simulation. However, it has been successfully used for the simulation of AlGaAs/GaAs HBTs [15].

At the quantum level, e.g., Gateway Modeling offers a one-dimensional (1–D) Schrödinger–Poisson solver POSES [16] for charge analysis in HEMT devices for process control.

The two- and three-dimensional device simulator DESSIS from ISE [10] has demonstrated a rigorous approach to semiconductor physics modeling. Some critical issues, as the above stated extensive trap modeling, are solved. Recently, first steps in direction of interface and III–V modeling have been reported [17].

Using a simplified 1-D current equation quasi-2-D approaches are demonstrated, formerly by the University of Leeds, e.g., [18]. This approach has also been verified for a number of examples and for gate-lengths down to 50 nm [19]. It is available as a submodule of Advanced Design System (ADS) from Agilent Technologies [20] delivering an interface to the microwave simulator. The emphasis is put on the extraction of compact large-signal models. Examples of S-parameter simulations of AlGaAs/GaAs HEMTs have been presented. This tool combines the advantages of a full HD transport model coupled with Schrödinger's equation, but has the drawback of the simplified 1-D current equation.

A similar quasi-2-D tool is Fast Blaze from Silvaco, also based on code from Leeds, which together with the 2-D ATLAS [21] has claimed the simulation of AlGaAs/GaAs and pseudomorphic AlGaAs/InGaAs/GaAs HEMTs.

Table I summarizes features of III–V device simulators discussed in the paper.

TABLE I
COMPARISON OF DIFFERENT DEVICE SIMULATORS

Simulator	Dimension	Model	Features	Remarks
POSES	1D		Schrödinger-Poisson solver	
Leeds	quasi 2D	HD	Shrödinger equation	1D current equations, interfaces
Fast Blaze	quasi 2D	HD	TE heterojunction model	1D current equations, interfaces
ATLAS	2D	DD,ET	TE heterojunction model	no tunelling, modeling
PISCES	2D	DD,ET	III-V models	
G-PISCES	2D	DD	full set III-V models	no ET(HD)
MEDICI	2D	DD,HD	anisotropic properties	mixed-mode, interfaces
MINIMOS-NT	2D	DD,HD	(see text)	
DESSIS	2D,3D	DD,HD	trap modeling, TFE model	III-V modeling

III. Critical Issues of Modeling III–V Devices

This section discusses critical modeling issues for III–V devices based on GaAs, AlAs, InAs, InP, and GaP, their ternary alloys, and nonideal dielectrics. We have addressed these issues in the 2-D device simulator MINIMOS-NT [22]. The models are based on experimental or Monte Carlo simulation data and employ analytical functional forms which cover the whole material composition range. The model parameters are checked against several independent HEMT and HBT technologies to obtain one concise set used for all simulations. Reviewing simulation of HBTs and submicron HFETs with gate-lengths down to 100 nm used for millimeter-wave devices, solutions of energy transport equations are necessary to account for nonlocal effects, such as velocity overshoot. A new model for carrier temperature dependent energy relaxation times [23] has been developed as well as a model for lattice temperature dependent saturation velocities [24].

Considering the nature of the simulated devices (including abrupt junctions) heterointerface modeling is a key issue. Thermionic emission (TE) and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces. Carrier tunneling must be included to describe the current transport from the channel to the contacts in HEMT devices depending on the alloying of the ohmic contacts. For HFET devices the Schottky contact model determines the possibility to calculate realistic gate currents, based on thermionic effects. Another critical issue for recessed HFETs and for HBTs is the description of the semiconductor/insulator interface. Fermi-level pinning prevails especially for typical barrier materials such as AlGaAs or InAlAs, for ledge materials such as InGaP, and insulators such as SiN. General agreement for HFETs demands a nonlocal description of the impact ionization. Further, when assessing a complete device description, the inclusion of holes and hot hole effects is necessary. Trap modeling, e.g., the inclusion of DX centers, and especially dynamic trap modeling are the most challenging issues for III–V devices since the carrier lifetimes cannot be generalized without deep insight into process technology, e.g., from *1/f* noise measurements. Bandgap narrowing is considered by an analytical model. A distinction between majority and minority carriers is made for the low field mobility based on Monte Carlo simulations. Yang *et al.* [25] stressed the importance of Auger recombination for InGaAs-base HBTs relative to SRH recombination.

III–V materials are known to have a reduced heat conductivity in comparison to Si [26]. Selfheating effects are accounted for by solving the lattice heat flow equation selfconsistently with the energy transport equations. Examples are given in the next

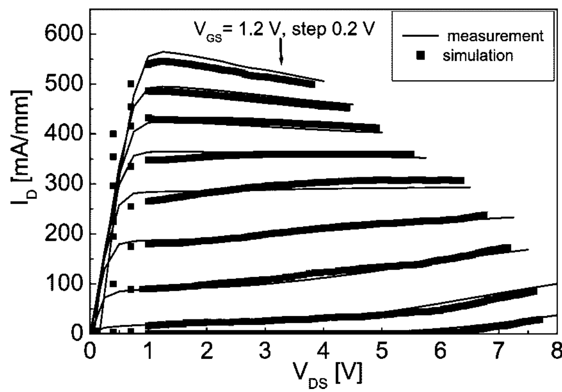

Fig. 1. Output characteristics of a pseudomorphic $Al_{0.2}Ga_{0.8}As/-In_{0.2}Ga_{0.8}As/GaAs$ high-power HEMT with gate-length $l_g = 210$ nm.

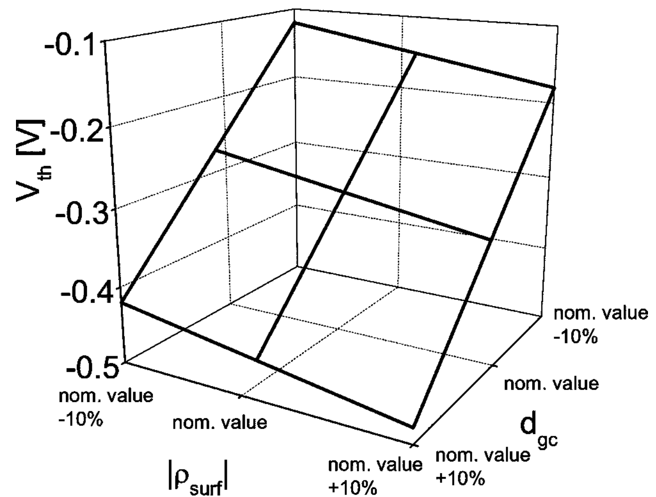

Fig. 2. Simulated variations of V_{th} due to variations of gate-to-channel separation d_{gc} and the magnitude of the negative surface charge density ρ_{surf}.

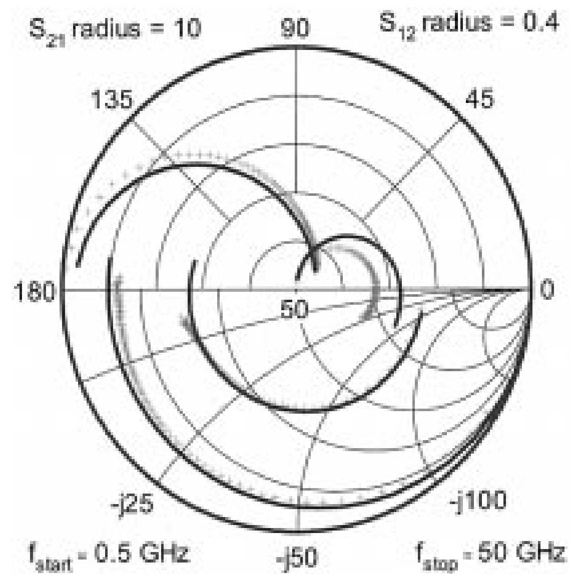

Fig. 3. Simulated (−) and measured (+) S-parameters of a $l_g = 140$ nm HEMT at $T_L = 373$ K from 0.5 GHz to 50 GHz using 0.5 GHz steps.

section for both HEMT and HBT devices. The determination of thermal boundary conditions and the verification of temperature distributions are performed in agreement with three-dimensional thermal chip simulations.

The advance of device simulation further allows a precise physics-based small-signal extraction [27]. Measured bias dependent S-parameters serve as a valuable source of information when compared to bias dependent S-parameters simulated from a device simulator, e.g., from MINIMOS-NT. This procedure reflects the full RF-information contained in the S-parameters and allows process control beyond the comparison of dc quantities, which do not completely account for the RF-properties of interest, e.g., because of the dynamic trap occupation. Note, Morton *et al.* [18] demonstrated a software interface between a quasi-2-D device model and the compact Root large signal model within the Microwave Design System (MDS).

The big challenge remaining for III–V device simulation is the improved understanding of processed semiconductors after different manufacturing steps, for example, before and after etching. Although a variety of simulators have successfully demonstrated the agreement with measurements the understanding of changes of transport and interface parameters remains the ultimate goal of process control.

IV. Selected Results of Industrially Relevant Devices

For HFET performance the very critical issues are process control and inverse modeling of geometrical structures. Fig. 1 shows the simulated and measured output characteristics of a pseudomorphic $Al_{0.2}Ga_{0.8}As/\ In_{0.2}Ga_{0.8}As/GaAs$ high-power HEMT with gate-length $l_g = 210$ nm at substrate temperature of $T_L = 300$ K. The device is designed for Ka-band applications. Selfheating effects are accounted for as well as impact ionization. Special care is put to match the output conductance for $V_{DS} > 5$ V to characterize the device in the V_{DS} region, which defines the clipping of a voltage swing on an applied load-line, and thus linearity.

The most critical region of recessed HFETs is the sub gate-contact region. For typical gate-lengths of $l_g = 150$ nm and below the definition of recess structures offers a process uncertainty due to recess etching. This uncertainty can be analyzed by device simulation. Fig. 2 shows the sensitivity analysis of the threshold voltage V_{th} toward surface charges and the gate-to-channel separation d_{gc}. The measured mean value was $V_{th} = -0.3$ V, for the surface charge density $\rho_{surf} = 10^{12}$ cm^{-2} is assumed. The device used was a $l_g = 150$ nm high gain pseudomorphic HEMT used for applications from Ka-band to the W-band. This analysis for various recess parameters allows control of the device structure, since several etch parameters used during mass production can be evaluated by inverse modeling of the device results.

Fig. 3 demonstrates a comparison of the simulated and measured S-parameters of a $l_g = 140$ nm pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.25}Ga_{0.75}As/GaAs$ HEMT at $T_L = 373$ K from 0.5 GHz to 50 GHz using 0.5 GHz steps. No fitting is applied, just the parasitic elements extracted from the measurements are used. The overall agreement is considered good. The discrepancies found for S_{12} between simulation and measurement are due to both a systematic error in the determination of S_{12} and the simulation itself.

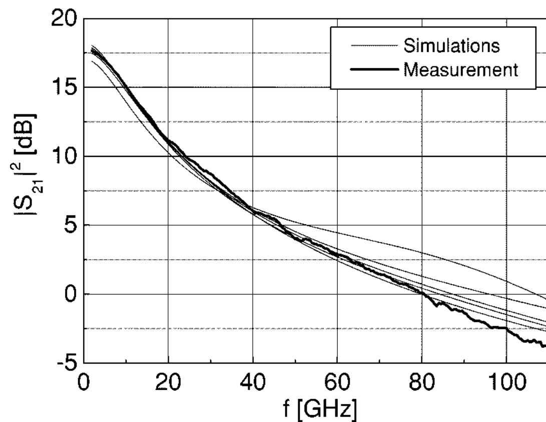

Fig. 4. Sensitivity analysis of the magnitude of $|S_{21}|^2$ to variations of gate-to-channel separation d_{gc} for a pseudomorphic HEMT.

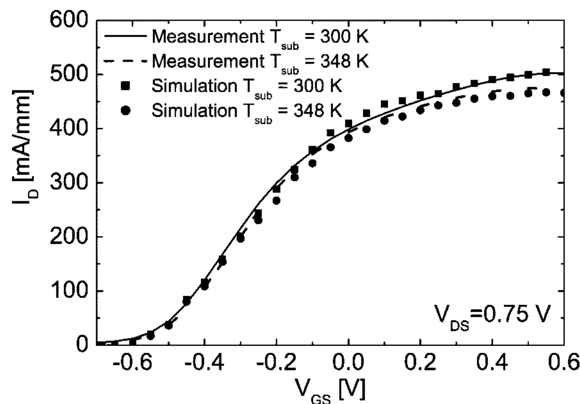

Fig. 5. Transfer characteristics of a composite channel InAlAs/InGaAs/InP HEMT with $l_g = 150$ nm for two different temperatures.

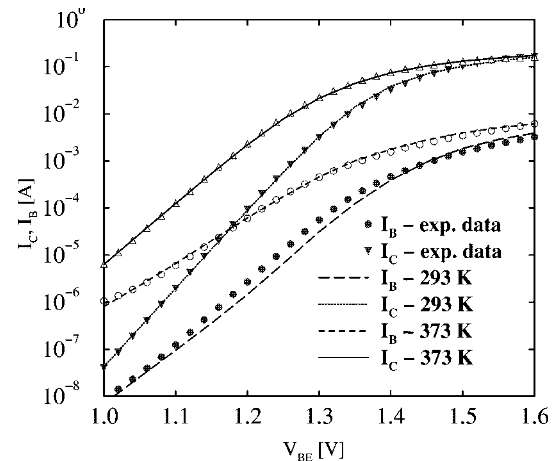

Fig. 6. Forward Gummel plots at $V_{\rm CB} = 0$ V for AlGaAs/GaAs HBT: Comparison with measurement data at $T_{\rm L} = 293$ K and $T_{\rm L} = 373$ K.

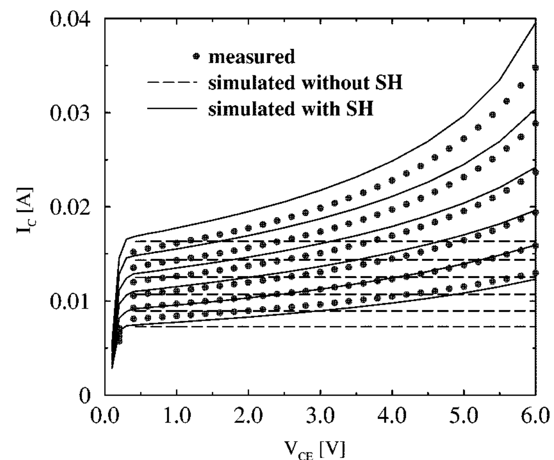

Fig. 7. HBT output characteristics: Simulation of with and without selfheating compared to measurement data at constant $V_{\rm BE}$ stepped from 1.4 V to 1.45 V.

Fig. 4 shows a sensitivity analysis of the magnitude of S_{21} to the gate-to-channel separation d_{gc} [28] for $l_g = 150$ nm 2×60 μm gate-width double heterojunction pseudomorphic HEMT. The effect of the variation of d_{gc}, which amounts to $\pm$25% of the nominal value, is visible for the whole frequency range of operation. In comparison to statistically analyzed wafer mapping results this procedure allows to separate statistical changes from longterm systematic changes for several runs in production.

Analyzing device breakdown of pseudomorphic GaAs HEMTs a detailed study of the gate currents can be performed to evaluate the two factors contributing to the gate current: thermionic field emission (TFE) effects and impact ionization, for details see [29], [30]. A nonlocal model for the gate contact is a critical issue to calculate gate currents and thus obtain realistic breakdown voltages, as was also shown by Lyumkis *et al.* [17].

For high-speed InAlAs/InGaAs HEMTs, the precise evaluation of low voltage or low power capabilities is useful for the development for high speed optical data transmission beyond 40 Gbit/s. The comparison of several lattice matched and metamorphic technologies further allowed to obtain consistent simulation parameters also for this material system. Fig. 5 shows simulation and measurements for two different substrate temperatures for a composite channel $\rm In_{0.52}Al_{0.48}As$/$\rm In_{0.66}Ga_{0.34}As$/$\rm In_{0.53}Ga_{0.47}As$/InP HEMT for $l_g = 150$ nm. High field effects such as impact ionization are considered [30]. This allows for the analysis of both, optimized speed and limiting gate current, when scaling δ-doping and gate to channel separation for the requirements of 80 Gbit/s operation.

The III–V HBTs are considered essential for high-power amplifiers at 3 V power supply, as they offer high current amplification and power-added efficiency (PAE) at 0.9/1.8 GHz [31]. A small chip-size 2 W MMIC based on AlGaAs/GaAs HBTs with excellent performance for wireless applications (62% PAE at 1.8 GHz) was demonstrated in [32]. Fig. 6 shows the simulated forward Gummel plot of such 3×30 μm^2 AlGaAs/GaAs HBT with an InGaP ledge compared to experimental data. Next to the good agreement at room temperature, the simulated Gummel plot at 373 K demonstrates the ability of `MINIMOS-NT` to reproduce the thermal device behavior correctly. It is often problematic to achieve realistic results in simulation of output HBT characteristics, especially for high-power devices. As already stated in [33] the power dissipation increases with collector-to-emitter voltage $V_{\rm CE}$, gradually elevating the junction temperature above the ambient temperature. This leads to gradually decreasing collector currents $I_{\rm C}$ at constant applied base current $I_{\rm B}$ or, respectively, gradually increasing $I_{\rm C}$ at constant base-to-emitter voltage

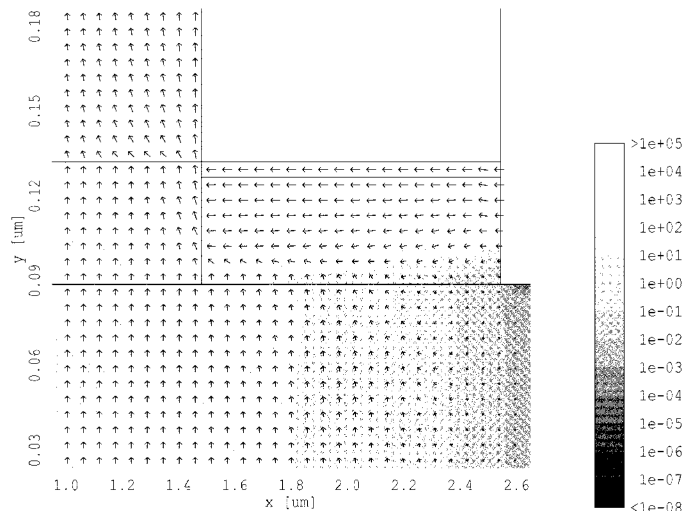

Fig. 8. Electron current density [A/cm^2] at $V_{BE} = 1.2$ V: Simulation without surface charges.

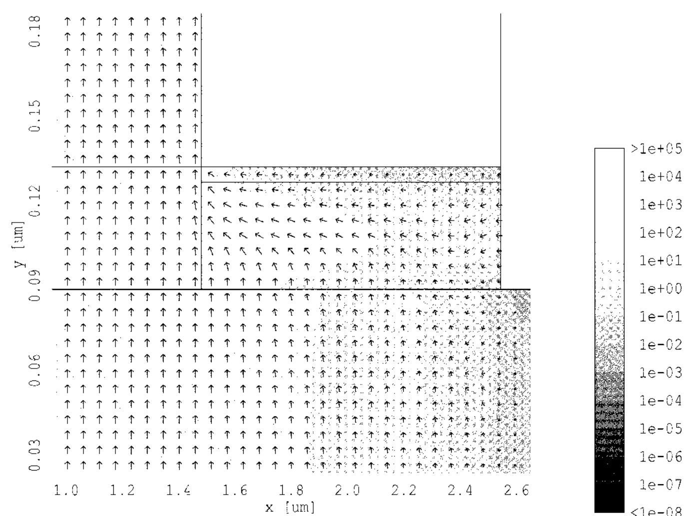

Fig. 9. Electron current density [A/cm^2] at $V_{BE} = 1.2$ V: Simulation with a surface charge density of 10^{12} cm^{-2}.

V_{BE}. Fig. 7 shows the simulated output device characteristics compared to measurements for constant $V_{BE} = 1.4$ V to 1.45 V using a 0.01 V step. Note the significant disagreement between simulation without selfheating (SH) and the measured data and the good agreement when selfheating is included in the simulation. The lattice temperature reaches as much as 400 K for the specified thermal resistance. As already stated in [34] such lattice temperatures significantly change the material properties of the device and, consequently, its electrical characteristics. This confirms the necessity of exact dc simulations at several high ambient temperatures before including selfheating effects.

It is well known that GaAs-HBTs with an InGaP ledge have an improved reliability [35]. Power amplifiers with InGaP/GaAs HBTs are part of many cellular phone today. Two-dimensional device simulation allows the analysis of experimental data in cases which cannot be explained by simple analytical assumptions. This proved to be especially useful for explaining and avoiding device degradation which occurs as a result electrothermal stress aging. The impact of the ledge thickness and the negative surface charges, which exist at the ledge/nitride interface, was studied for a one-finger 3×30 μm^2 InGaP/GaAs HBT with respect to reliability [36]. We found a surface charge density of $\rho_{\rm surf} = 10^{12}$ cm^{-2} to be sufficient to get good agreement with the measured Gummel plots at $V_{CB} = 0$ V. Simulation results for the electron current density at $V_{BE} = 1.2$ V without and with a surface charge density of 10^{12} cm^{-2}, respectively, are shown in Figs. 8 and 9. Based on these investigations it is possible to explain the base current degradation (see Fig. 10) of a strongly stressed device by a decrease in the effective negative surface charge density along the interface from 10^{12} cm^{-2} to 4.10^{11} cm^{-2} due to compensation mechanisms [37].

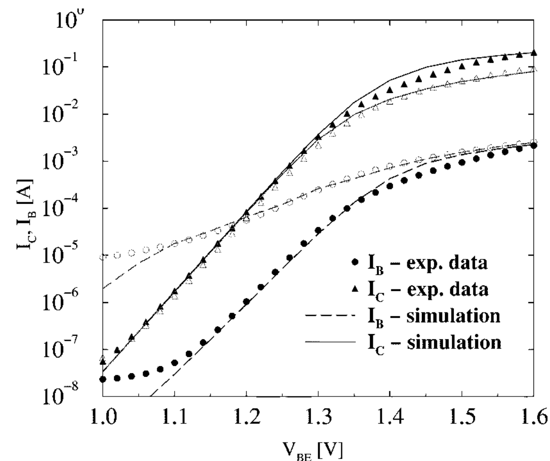

Fig. 10. Comparison of measurements (symbols) and simulations (lines) before (filled) and after (open) HBT aging.

V. Conclusion

An overview of the state-of-the-art of simulation tools for heterostructure RF-devices is presented. Simulation results for industrially relevant devices in good agreement with measured data are demonstrated. With an increasing number of stable, reliable heterostructure technologies available, a meaningful comparison between simulation results and statistically analyzed data is possible and delivers on the one hand, model verification, and on the other hand, valuable process information.

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