IMPLEMENTATION OF AN AUTOMATED INTERFACE FOR INTEGRATION OF TCAD WITH SEMICONDUCTOR FABRICATION

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ABSTRACT

The structure and systematics of automated transfer of semiconductor fabrication process data into a Technology Computer-Aided Design (TCAD) framework are described in detail. The main stages of semiconductor fabrication from design to the final product are identified and outlined. Based on this system the TCAD framework is mirrored to reflect the functionality and behavior of the fabrication system as closely as possible. The structure of the necessary interfaces for this integration is described. The implementation of this system is explained and a couple of examples of the resulting framework are given. The resulting benefits from this approach are discussed.

INTRODUCTION

This work concentrates on integrating TCAD (Dutton and Yu 1993) into the semiconductor fabrication process flow. The use of TCAD is twofold: Firstly it models the complex flow of semiconductor fabrication steps ending up with detailed information on geometric shape and doping profile distribution of a semiconductor device in scope (like CMOS- or Bipolar-Transistors). These tasks are usually summarized under the term process simulation.
Secondly device simulation uses the information of the first step to calculate the characteristics of semiconductor devices. The resulting device characteristics are used for fitting circuit simulation models as implemented in any circuit simulator, like HSPICE (Cazzani 1993), ELDO (Hennion et al. 1987) and SPECTRE (Gough and Marston 1983) The setup of such a simulation methodology requires a nearly completely documented semiconductor fabrication process flow including numerous fabrication details, like angle of incidence of ions implanted in ion implantation process steps, or etch rate distribution as a function of the local angle of the etched layer surface.
Any modern semiconductor fabrication maintains this documentation to an extremely high level of detail, but commercial TCAD simulation software offered from vendors like ISE AG, Avant! or Silvaco needs this information in a very specialized format (Strasser 1999) which cannot be directly deduced from the standard process flow documentation.
The traditional way of setting up the process- and to some extent also the device TCAD simulations is, entering required information manually, which is of course a significant source of errors. We propose a methodology with the main target to automate this conversion process to a high extent.

INTEGRATION ASPECTS

Short Outline of the Full Semiconductor Fabrication Process

Starting from the product idea the following sequential steps occur in a standard integrated circuit development and production flow.

Design: The integrated circuit is designed as a schematic taking into account the special demands of integrated circuits (crosstalk, common substrate etc.). It is now standard to use ECAD tools to simulate the behavior of any schematic design of an integrated circuit by using detailed circuit simulation models and design rules which are specific to a particular process family (technology node).

Layout: The resulting integrated circuit is drawn as a layout on the specific layers, which are given by the semiconductor process family (technology node). The combination of multiple layers, like implantation masks and etch masks, defines the shape and functionality of the electronic devices in the integrated circuit.

Mask shop: The layout is post processed to take into account process induced size variations (layer biasing) and constraints on combination of layers (logical combination). The physical mask layers are written from these data by using laser- or e-beam writing equipment.

Processing: The wafer start material is released at the beginning of the process flow into fabrication. In the following these wafers are subject to numerous single process steps like ion implantation, deposition and etching of semiconductor, dielectric and metallic materials, diffusion of

dopants, oxidation, and lithography to structure multiple of the deposited layers using the previously fabricated masks.

Test: After leaving the fabrication the now functional integrated circuits are tested electrically. Firstly on single device level with process control monitors (PCM's), secondly on integrated circuit level (wafer sort => test of circuit functionality) including inking the bad pieces. These tests select the working parts for further processing.

Assembly: Scribing into pieces and packaging of the single circuits. After the packaging a final electrical test is performed.

The ECAD simulation tools in sequence Design to Layout are already closely integrated into the development chain (Swaminathan 1997) and are therefore very efficient.
Assembly simulation is not subject to this work, but tools (Ladvanszky 1994; Nusseibeh et al. 1995) are used for analysis of new packages with respect to electromagnetic field, stress and self-heating.

For sequence Mask Shop/Processing/Test good simulation solutions exist on the market for single process steps, e.g. SIGMA-C for lithography and mask fabrication steps, TCAD tools from ISE, Avant! and Silvaco for the process- and device-simulation steps which are at least sufficient for most of the two-dimensional process- and device-simulation applications.
However, the setup of these TCAD simulators is highly complicated and time consuming. Changes in fabrication procedures, like parameter optimization of process conditions, are not reflected in simulation if the traditional way of defining this setup is carried out manually. Therefore the simulation flow definitions get asynchronous to the actual fabrication recipes very quickly.

The TCAD Simulation Flow as a Mirrored Image of the Semiconductor Fabrication Process Flow

The main concept which should be considered is to match the simulation methodology as close as possible to the fabrication methodology. The resulting workflow can be seen in Fig. 1.

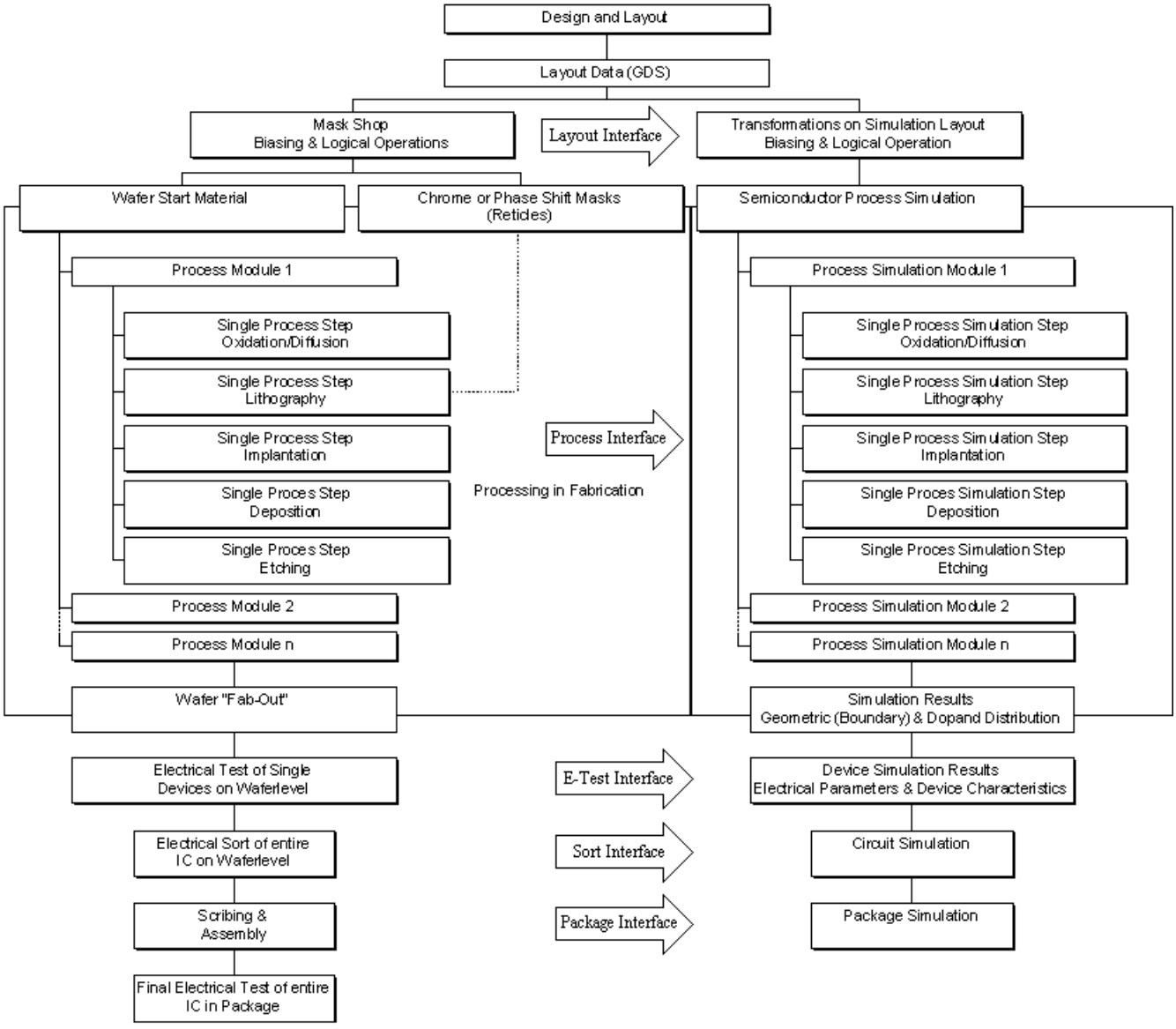

Figure 1: Structure of the semiconductor process flow and its mirror image the TCAD simulation flow

Looking at this picture the main application areas for TCAD integration into the actual fabrication are clearly identified. In the following the main aspects of the parts of this implementation are outlined.

The Interface from Design and Layout as Process Simulation Input

According to above outlined workflow, the layout of the masks is one of the two main inputs for process simulation. Normally this layout is available in GDSII-binary format, which can be read by any of the above-mentioned commercially available TCAD tools. To mirror the activities carried out in the mask shop these data must undergo the same transformations as in reality listed above.

The Interface between the Detailed Semiconductor Process Flow Description and the Process Simulation Command File

The overall process flow information is typically documented in the database of a manufacturing execution system like PROMIS from Brooks-PRI, SiView from IBM, or WorkStream from AppliedMaterials.
The process simulation relevant information inside this database is numerous, depending on the detailed level of the simulation models. Normally the following datasets are needed for process simulation:
Sequence of process steps representing the semiconductor process flow (oxidation => layer thickness measurement => implantation => diffusion => material deposition => lithography etc.)
Blocks of process sequences which are carried out on the same semiconductor fabrication equipment and are normally organized as program sequences like oxidation/diffusion programs which can consist of up to dozens of single process steps with different temperatures (temperature ramps) and gas ambients (gas steps or ramps).
The detailed process parameter set of one single process step (e.g. ion species and composition, ion dose and energy, angle of incidence and rotational orientation of ion beam with respect to wafer, ion beam divergence etc. for ion implantation)
Measurement positions in the full semiconductor process flow where selected physical characteristics like layer thickness or sheet resistances are measured by using metrology tools on wafer level.
The first three subjects above represent the hierarchy levels from highest to lowest.

The interface between electrical test and device simulation

After finished fabrication of the silicon wafers the first electrical test is the measurement of simple test structures and devices (organized in PCM's => Process Control Monitors) in the scribe-lines of the wafer. These measurements are carried out on automated tester systems (e.g. Agilent or Keithley) on wafer level. The measurement procedures are again hierarchically oriented in the following way:
Measurement program set up for actual technology node
Subprogram defined for actual PCM (normally several PCM's are inserted in the scribe-lines)
Module for device under test (DUT) consisting of single program statements measuring relevant electrical parameters
Single measurement algorithms for e.g. CMOS threshold voltage, or diffusion sheet-resistance
Single steps of carrying out the measurement algorithm for e.g. CMOS threshold voltage in saturation. These steps define how the device terminals are connected to the voltage and current sources of the automated tester and how the currents and voltages of the DUT are measured.

The last three hierarchy steps listed above are mirrored on the device simulation side to provide comparable electrical data of measurements and simulation.

The interface between device characterization and modeling (SPICE) and device simulation

This interface deals with the generation of reliable device models for circuit modeling (e.g. SPICE). The main devices (NMOS/PMOS Transistors for standard CMOS processes, additionally bipolar transistors for BiCMOS processes) of any new process node must be characterized completely in terms of output characteristics, transfer characteristics, amplification, etc. This process results in scalable electrical models (BSIM3 for CMOS, VBIC for Bipolar transistors) or compact models for circuit simulation.
In the TCAD fabrication integration scheme the source for this fitting procedure can be twofold. Firstly the usual way of measuring the characteristics on semiconductor wafer material, secondly by simulating these characteristics with device simulation.
The second approach has the enormous advantage of getting worst case predictions (Gruber et al. 1998; Williams and Varahramyan 2000) which are directly related to process parameter changes by applying statistical variations on selected semiconductor process step parameters (e.g. selected implantation doses).
Furthermore combined process and device simulations without the existence of any semiconductor material can generate preliminary models very early in the process development stage.

IMPLEMENTATION

Layout interface

The layout data is transformed by applying logical operations (bias etc.) which are specific to the semiconductor process flow in scope. This set-up is only defined once in the development phase of the process and never changes through the life cycle of the semiconductor process.

Semiconductor process flow to process simulation command file

Typically process flows under development are subject to frequent changes. Therefore the detailed flow descriptions are not implemented in the MES system until the process flow is frozen.

Normally the flow description is tabulated in a simple file format, like an ASCII-table, for reference during the process development phase and for the fast setup of short process sequences by simply typing the relevant process steps into an EXCEL-sheet.
By standardizing the flow description information for this stage, it is possible to define an automated converter which transfers the process flow information into an abstract semiconductor process simulator input language called SPR (Simple Process Representation) This input is then used by another converter to generates the final process simulator input command files.
By using the SPR language it is possible to use different process simulators even from different vendors like DIOS-ISE or TSUPREM4 with the same process flow description.
Once the semiconductor process flow is frozen and released, the MES system provides any input on the process flow, which is necessary for process simulation. However this information must be reduced to the subset relevant for process simulation.

Electrical Test to Device Simulation Command File

The measurement algorithms of important DC and AC electrical parameters like threshold voltage (VT), effective gate length (L_{eff}) of CMOS-transistors or transit frequency of bipolar-transistors are not standardized to full detail (biasing conditions etc.). Therefore the built-in algorithms inside commercial device-simulators are insufficient for many parameters measured at electrical test.
This problem is solved by using the source code of the measurement algorithms (in the case of the Keithley-software-system KITT this is a C++-Source code) and converting this code into the input language of the device simulator (e.g. DESSIS-ISE) and the extraction tool (e.g. INSPECT-ISE) directly.

Device characterization and modeling to device simulation command file

This interface is still under development since (especially for bipolar transistors) the physical models in commercially available process simulators are not sufficient for some subsets of applications (prediction of f_T characteristics, Gummel-plots etc.). This fact decreases the predictive power of the combined process and device simulation approach.
The resulting electrical characteristics are therefore not sufficient to make a circuit simulation model of the simulated device in advance of any electrical data.
However, the device simulation toolset is able to generate an equivalent set of DC- and AC-data, which may be used for circuit model generation .

APPLICATION EXAMPLES

Transfer of semiconductor diffusion and oxidation process recipes between 4” and 8” wafer fabrications

TCAD has found to be very useful in reducing the risks of semiconductor process flow transfer between different fabrications (Nilsen et al. 1999).

When transferring diffusion or oxidation process recipes from on type of equipment (e.g. 4" diffusion furnace) to another type of equipment (e.g. 8" diffusion furnace) it is generally not possible to copy the diffusion recipe without modifications.
For instance, the temperature ramp rate for 8" diffusion recipes is usually significantly slower than for 4" equipment. Although the recipes might differ significantly the impact on the wafer should be nearly identical for 4" and 8" equipment. Thus optimization of the diffusion recipes is needed in order to make the differences in doping distribution and oxide thickness between 4" and 8" recipes as small as possible.

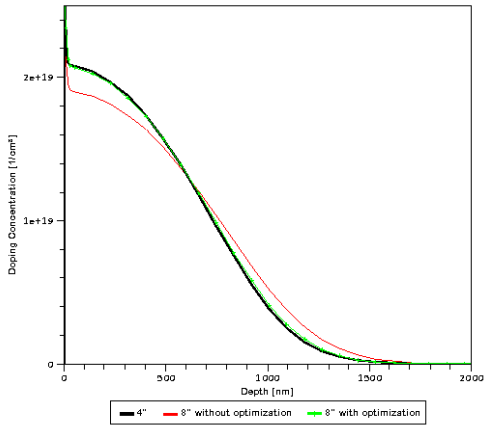

Figure 2: Doping Profiles for a 4" Diffusion Furnace Compared to an 8" Diffusion Furnace Before and After Optimization

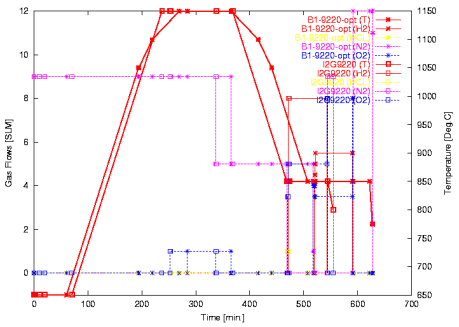

Figure 3: Graphical comparison between the 4" and 8" diffusion recipe

Automated documentation of the full semiconductor process flow for engineering training and documentation purposes

The simulation results of the semiconductor process flow contain the information of the geometry of the simulated device (e.g. CMOS-Transistor) and the complete doping distribution. This information is usually needed by process engineers but is very difficult, costly, or even impossible to obtain by other methods (e.g. SIMS, TEM).
The combination of information on the process simulation and the process flow description, results in a documentation of the process of very high quality. This information obtained by process simulation, which is usually only available for TCAD-Engineers, can be easily shared with process engineers, if a format with cross platform compatibility is used. One data format which fulfils the necessity of cross

platform compatibility is the Hypertext Mark-up Language (HTML). Furthermore, especially during the development phase of a new process it is necessary that the simulation results can be transformed very quickly into HTML.
A swift transformation of the process simulation results (which are usually in a platform dependent format or only viewable by special TCAD-software) to HTML is achieved by a PERL script which extracts the relevant simulation results and links them with the description of the respective process step.
The information of a diffusion or oxidation process recipe often consists of several dozens single process steps. This huge amount of information is best analyzed graphically as process temperature and gas flows versus time (see Fig. 3).
Fig. 4 shows the final process simulation result for a high performance bipolar transistor integrated in a BiCMOS process. This result is used for subsequent device simulation to get detailed electrical characteristics of the bipolar transistor.
Another information often needed by process engineers is the temperature versus time of the complete process as shown in Fig. 5, which allows identifying the most relevant thermal process steps quickly.

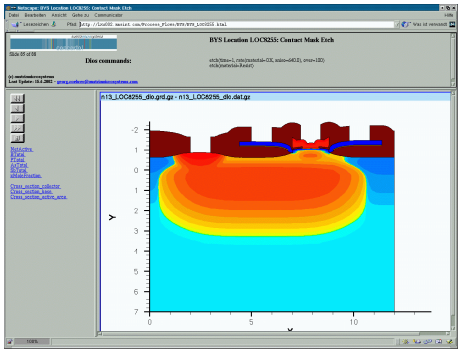

Figure 4: Example for the final simulation result of a bipolar transistor

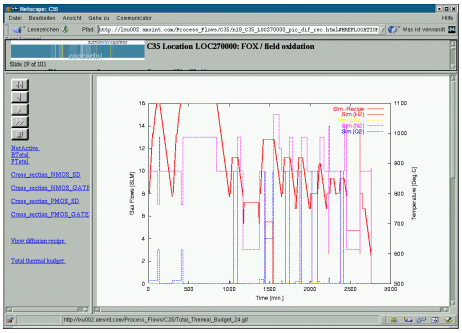

Figure 5: Overall thermal budget of a dedicated process flow

CONCLUSIONS

Implementing a framework for the integration of TCAD with the actual fabrication process results in multiple impacts on the strategic position of TCAD in a semiconductor fabrication environment. Historically TCAD was only applied on single device structures to gain better insight into the physics behind devices (Feudel et al. 1993). Additionally, information on physical quantities, which are difficult to obtain experimentally, was gained. By automated integration of the TCAD framework over the whole workflow of semiconductor circuit fabrication many additional application fields can be addressed, as shown by this work. The setup of new processes (or the transfer of existing technologies) is speeded up dramatically. The human induced errors are additionally reduced dramatically. The number of, at least passive, users of TCAD in a semiconductor company grows from a handful R&D engineers to the entire engineering and production team. This result in a much better utilization of the resources spent in TCAD (software license costs, work efficiency of TCAD engineers, computer hardware etc.).
The gap in technical information between the top management and the "engineer in the production line" is made smaller. This aspect should not be underestimated in the field of semiconductor industry because due to the high complexity of integrated circuit fabrication, any closed documentation of the processes is of inevitable value.

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