Effects of Stress-Induced Bandgap Narrowing on Reverse-Bias Junction Behavior

Venkatesh Gopinath, Sheldon Aronowitz
Process and Technology Development
LSI Logic Corp.
3115 Alfred Street
CA-95054 Santa Clara, USA
vgopinat@lsil.com

Vassil Palankovski, Siegfried Selberherr
Institute for Microelectronics
Technical University Vienna
Gusshausstrasse 27-29
A-1040 Vienna, Austria
Palankovski@iue.tuwien.ac.at

Abstract

The effects of bandgap narrowing due to stress generated during Shallow Trench Isolation (STI) are analyzed. Reverse-bias junction leakage and capacitance measurements are correlated to results from device simulation. A locally varying stress dependent bandgap model is implemented to understand the influence of stress effects. Increases in both junction capacitance and leakage agree well with experiments. Results of leakage and capacitance on the 0.18 μm and 0.09 μm technologies indicate that effects of process induced stress on device behavior need careful attention.

1. Introduction

Process induced stress occurs at several steps in the manufacturing of integrated circuits, for example, due to sharp trench corners at the top and bottom of the shallow trench, which is enhanced during subsequent liner oxidation, or due to the deposition of spacer nitride or intermetal dielectric. In many cases, stress results in undesirable negative effects on device performance. In particular, the STI integration method has a strong effect on reverse-bias junction leakage [1]-[3]. Studies by Smeys et al. [4] indicated that, even in the absence of etch induced traps in the depletion region, oxidation stress caused junction leakage. They attributed this increased generation current to stress-induced bandgap narrowing. This leakage current increased with decreasing active area pitch and their model predicted an exponential dependence of leakage current on stress. Studies done by Gopinath et al. [5] on different liner oxidation schemes indicated a strong correlation between reverse-bias junction leakage and stress due to liner oxidation. Recently, the impact of stress-induced bandgap narrowing on junction capacitance was reported by [6]. It was shown that, in addition to leakage, junction capacitance also increases due to its dependence on bandgap energy. However, none of the studies reviewed so far quantitatively simulated the effects of bandgap narrowing on device characteristics.

This is largely due to the fact, that bandgap energy in the commonly used device simulators is treated by a global variable while the stress is a local grid based variable. Relevant information about stress and its components can be obtained as a result from process simulation, e.g. with TSUPREM4 [7]. Suitable modifications to use this important information have been made to MINIMOS-NT [8] in order to, consequently, correlate process simulation, device simulation, and experiments. Stress simulated by TSUPREM4 is used as input to MINIMOS-NT, which maps these changes into local variations of the bandgap. The device simulations reflect these variations and the correlation of the results with experiments are quite satisfactory.

2. Description of the Model

Reverse-bias junction capacitance and leakage are influenced by several factors, the most important one being the bandgap energy E_g. Junction capacitance is indirectly determined by the bandgap voltage through the built-in potential (ψ_bi) and depletion width (W_d) and is given for abrupt junctions as follows [9]:

$$W_\mathrm{d} = \sqrt{\frac{2 \cdot \varepsilon_\mathrm{Si} \cdot (\psi_\mathrm{bi} \pm V_\mathrm{app})}{\mathrm{q} \cdot N_\mathrm{b}}}. \quad (1)$$

The built-in potential (ψ_bi) is

$$\mathrm{q} \cdot \psi_\mathrm{bi} \approx \frac{E_\mathrm{g}}{2} \pm k_\mathrm{B} \cdot T \ln \frac{N_\mathrm{b}}{n_\mathrm{i}} \quad (2)$$

and n_i, the intrinsic carrier concentration is given by

$$n_\mathrm{i} = \sqrt{N_\mathrm{C} \cdot N_\mathrm{V}} \cdot exp\left(-\frac{E_\mathrm{g}}{2 \cdot k_\mathrm{B} \cdot T}\right) \quad (3)$$

where N_C and N_V are the effective density of states in the conduction and valence bands, respectively. The junction capacitance per unit area is then given as

$$C_\mathrm{d} = \frac{\varepsilon_\mathrm{Si}}{W_\mathrm{d}} \quad (4)$$

ε_Si is the dielectric constant of silicon. Junction leakage, on the other hand, is an exponential function of bandgap

voltage and is given as the sum of diffusion and generation components [10] as

$$J_R = q\sqrt{\frac{D_p}{\tau_p}} \cdot \frac{n_i^2}{N_b} + \frac{q \cdot n_i W_d}{\tau_n}, \quad (5)$$

where J_R is the current density, N_b is the background impurity concentration, τ_p and τ_n are the recombination lifetimes of the holes and electrons, respectively and W_d is the width of the lighter doped region. Both terms on the right hand side of the (5) have the intrinsic carrier density n_i, which is an exponential function of the bandgap energy as seen in (3).

Therefore, process and operating conditions that affect the bandgap potential can have a profound effect on device behavior [11]. One of the process conditions that can change bandgap energy is pressure (P), which linearly decreases the bandgap energy as follows [12]:

$$\frac{dE_g}{dP} = -0.24\,[\text{meV/MPa}]. \quad (6)$$

Smeys [4] correlated their electrical results of increase in reverse-bias junction leakage and predicted a bandgap reduction of 0.1 meV/MPa of compressive stress. Pressure, a scalar, is calculated from stress, a tensor, by averaging the x and y components of stress as

$$P = -\frac{S_{xx} + S_{yy}}{2}. \quad (7)$$

3. Experiments

Devices from the 180 nm and 90 nm technology node were used to compare the simulations with measurements. The former experiment involved a combination of liner oxidation (15 nm and 30 nm) and liner undercut targets (17.5 nm, 90 nm, and no undercut) as listed in Table 1 and further detailed in [5].

Table 1. Liner and undercut splits

Split No.	Liner oxide target [nm]	Nitride undercut target [nm]
1	15	0
2	15	9
3	15	17.5
4	30	0
5	30	9
6	30	17.5

The 90 nm node experiments were done to understand the effect of trench bottom stress on device behavior. This study was performed for trench depths of 0.17 μm, 0.2 μm and 0.23 μm and the reverse-bias junction capacitance and leakage were analyzed. This study also involved the use of different background well species (Boron and Indium for p-well, and Arsenic and Phosphorus for n-well) to gauge the effect of background doping on well junction behavior [6]. Both studies indicated a strong correlation between

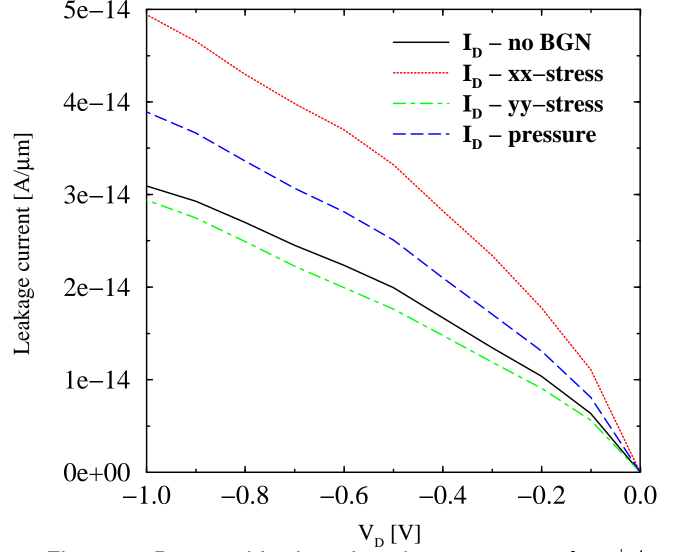

Figure 1. Reverse-bias junction characteristics of a p^+/n junction diode with varying stress.

stress as reported by TSUPREM and reverse-bias junction characteristics. In order to enable two-dimensional study of the stress induced changes, long perimeter intensive diodes (200 fingers of 0.99 μm width and 500 μm length) were used for correlating simulations with experiments. Simulating a section of the long diodes in the width direction reduces the three-dimensional problem to two dimensions. In the case of the 90 nm node, corner intensive devices, 27000 rectangles of 1.22 μm × 1.52 μm resulting in a total area of $5 \times 10^4 \mu m^2$ were used and simulated along the shorter dimension.

4. Results and Discussion

The bandgap narrowing equation shown in (6) was used to implement a locally varying bandgap in MINIMOS-NT. The simulations of a simple p^+/n junction diode with and without the model are shown in Fig. 1. It can be seen that the reverse-bias junction leakage increases with compressive stress. An understanding of the stresses generated from STI integration can be seen in Fig. 2 for device with trench depth of 0.2 μm. The S_{xx} component of the stress shows very high compressive values at the bottom of the trench and high tensile values at the top. The effect of bandgap reduction on the generation rate can be seen in Fig. 3. It can be clearly seen that the generation current in the depletion region has the highest magnitude along the high-stress STI sidewall areas.

Fig. 4 shows the comparison of experimental (error bars represent 95% confidence intervals [13]) and simulated values of reverse-bias p^+/n junction leakage. Stress predicted by TSUPREM4 simulations for the experimental conditions was used to model the bandgap in MINIMOS-NT. It can be seen that the bandgap narrowing model accurately reproduces both the magnitude and trend of the experimental data. However, the rate of change of leakage for the different process conditions is

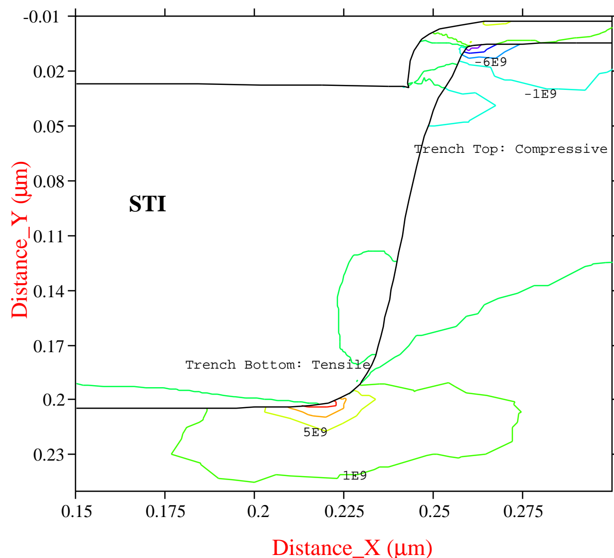

Figure 2. TSUPREM4 simulation of S_{xx} component of stress for trench depth of 0.2 μm. Note the high stress regions in the bottom and top of the trench.

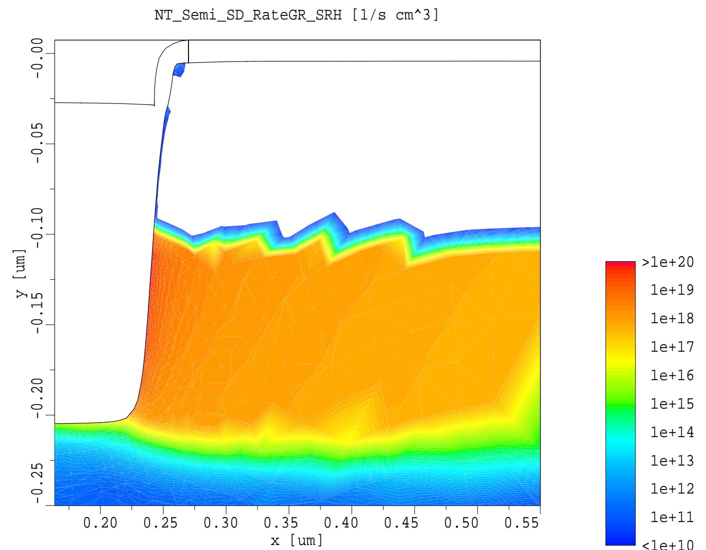

Figure 3. Generation rate [s^{-1} cm^{-3}]: Note the higher surface generation at the high-stress trench region.

somewhat stronger than the predicted by device simulation. Fig. 5 shows the same result for n^+/p perimeter diodes for the six different splits. Again, the bandgap reduction simulations show good agreement with the median values of the measurement.

Capacitance simulations using the bandgap narrowing model were performed for 90 nm junctions with varying trench depths. The experimental and simulated results agree well as shown in Fig. 6. The simulated stress was higher for the shallower trench depth case [6] which in turn leads to larger capacitance and higher junction leakage. The bandgap narrowing model in MINIMOS-NT accurately reflects this behavior. The reverse-bias junction leakage for the same structure is shown in Fig 7. While the simulator models the trend correctly, the actual values are higher than measured. However, the studies confirm that, in cases where feasible (due to limitations of gap fill), a deeper trench is preferable since the depletion region will span less of the high stress trench bottom and will lead to improved junction behavior.

It should be noted here that only stresses generated during STI liner oxidation were simulated and transferred to MINIMOS-NT for device simulations. However, the actual device undergoes many thermal cycles which lead to further stresses (and relief) during processing. The version of TSUPREM used did not carry over the stress components for the entire process sequence, hence it was decided to conduct this study with only the STI part of the stress since all the process splits were at the STI module.

5. Conclusions

A locally varying bandgap model is introduced into the device simulator MINIMOS-NT. The bandgap is then varied according to process-induced stresses and the reverse-bias junction characteristics are simulated. The results correlate well with devices fabricated on the 180 nm and 90 nm nodes.

6. Acknowledgment

We wish to thank Teresa Pinzon and Jerry Tabancay for extensive bench measurements of junction leakage and for ensuring proper processing of semiconductor material. Thanks are also due to Lesly Duong for setting up parametric tests used in this study. Vassil Palankovski acknowledges the support of the Austrian Science Fund (FWF), Project P14483-MAT.

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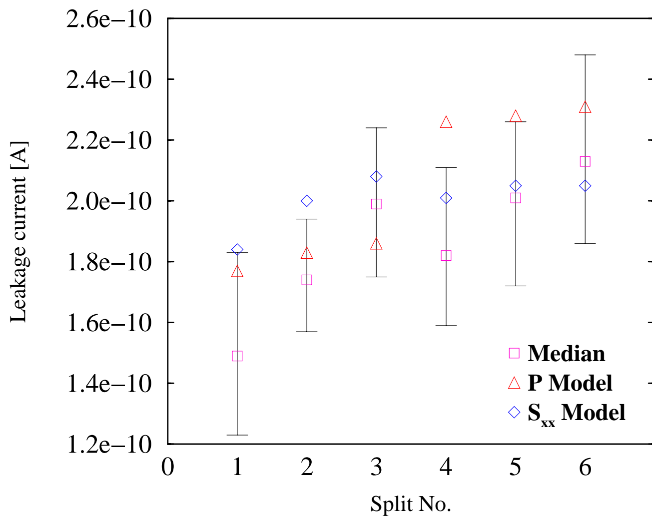

Figure 4. Reverse-bias junction leakage [A]: Results for p^+/n perimeter intensive diodes at −3.3 V bias. The pressure dependent bandgap narrowing model reproduces the value and trend of the leakage. The perimeter diode is 0.99 μm wide, 500 μm long with 200 fingers. The error bars represent 95% confidence levels.

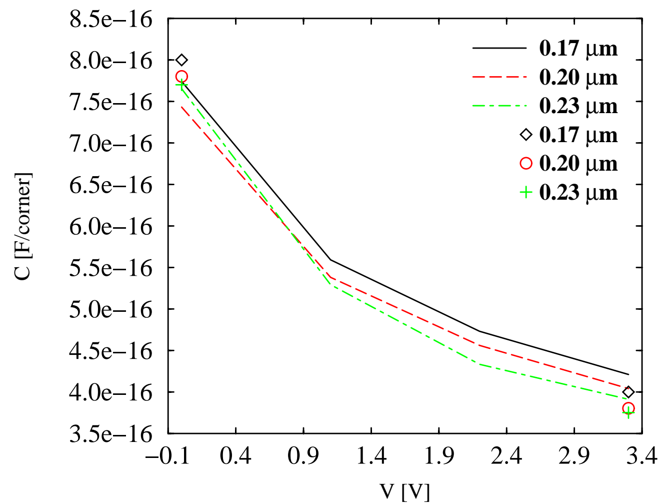

Figure 6. Reverse-bias junction capacitance [F/corner]: Simulations (lines) and measurements (symbols) for varying trench depths for n^+/p junctions. Capacitance is reported for a corner intensive diode with 27000 rectangles of 1.22 μm × 1.52 μm resulting in a total area of $5 \times 10^4 \mu m^2$.

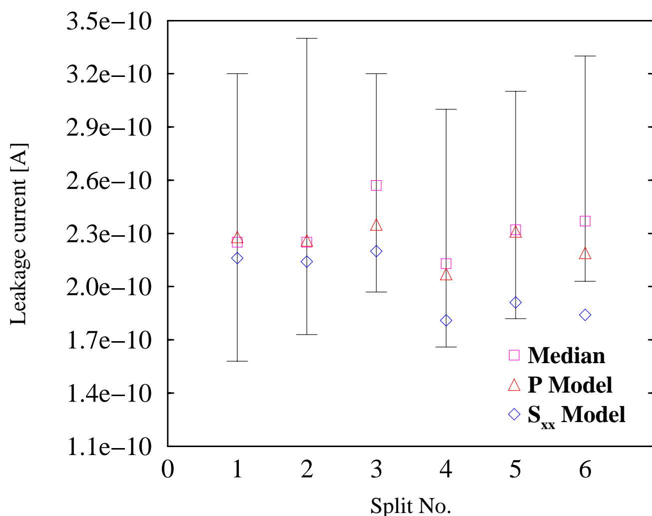

Figure 5. Reverse-bias junction leakage [A]: Results for n^+/p perimeter intensive diodes at 3.3 V bias. Measurements have higher scatter than their p^+/n counterparts.

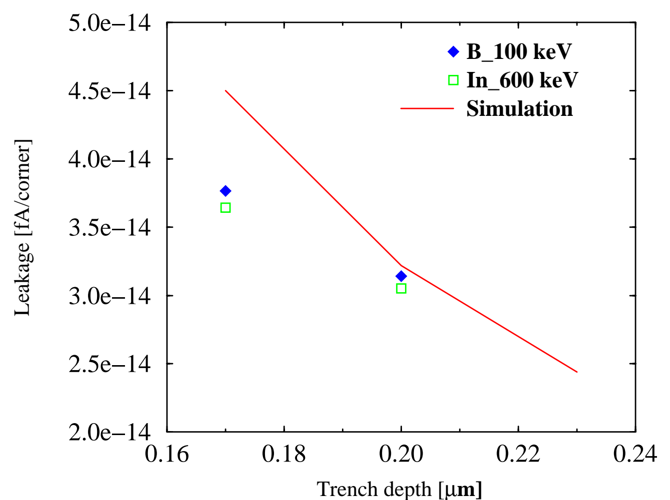

Figure 7. Reverse-bias junction leakage [A/corner]: Simulation (line) and measurements (symbols) for varying trench depths for n^+/p junctions. Choice of background doping does not impact junction leakage.

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