Eur. Phys. J. AP 21, 103–106 (2003)
DOI: 10.1051/epjap:2002121

THE EUROPEAN
PHYSICAL JOURNAL
APPLIED PHYSICS

Three-dimensional device optimization by Green's functions

J. Cervenka[1,a], R. Klima[1], M. Knaipp[2], and S. Selberherr[1]

[1] Institute for Microelectronics, TU Vienna, Gusshausstrasse 27-29, 1040 Vienna, Austria
[2] Austriamicrosystems, Unterpremstätten, Austria

Received: 21 June 2002 / Accepted: 14 October 2002
Published online: 19 December 2002 – © EDP Sciences

Abstract. Optimizing process- and layout-design in the development of modern electronic devices is key to achieve required characteristics. Coming along with the growing complexity of device structures, associated effects must be considered in an even more complex manner. The use of three-dimensional process- and device-simulation tools is inevitable. Because of the huge effort concerning computer resources from three-dimensional simulations it is of big interest to enable efficient ways for optimization, as early as possible in process flow. Hence this work shows, how it was possible, to optimize a high-voltage PMOS transistor before starting a complex three-dimensional device simulation.

PACS. 85.30.De Semiconductor-device characterization, design, and modeling

1 Introduction

For the development of electronic devices a set of design rules must be considered. Especially in the range of high voltage applications, used for instance in car manufacturing, the limits of the rules narrow. High applied voltages and relatively low dopant concentrations result in large space charge regions and an increase of the on-resistance. Shrinking the device lowers the on-resistance which is one of the most important technology parameters. As a consequence the engineers have to consider about smaller space charge regions which result in a reduced blocking voltage. These contradicting effects must be balanced by the device designer, often with the aid of modern simulation tools. While getting more complex device structures the need of accurate three-dimensional device simulators gets urgent. This work presents under which circumstances an early device optimization succeeds, before starting a complex, time consuming three-dimensional device simulation.

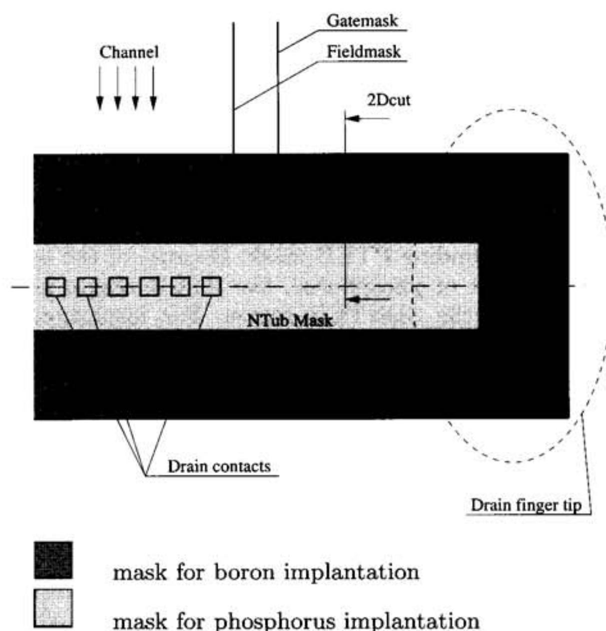

Fig. 1. Mask layout.

2 The device

The investigated device is a high voltage PMOS transistor. The drain area is built as a long rectangular PTUB finger, which is placed in a shallow/deep NTUB combination (SDNTUB), itself embedded in a p-doped substrate (*cf.* Figs. 1 and 2). Conventional two-dimensional device simulations had shown, the device would work fine. With the implanted boron and phosphorus profile the on-resistance would be acceptable, and also a maximum applicable voltage of 90 V between drain and substrate should be possible.

[a] e-mail: Cervenka@iue.tuwien.ac.at

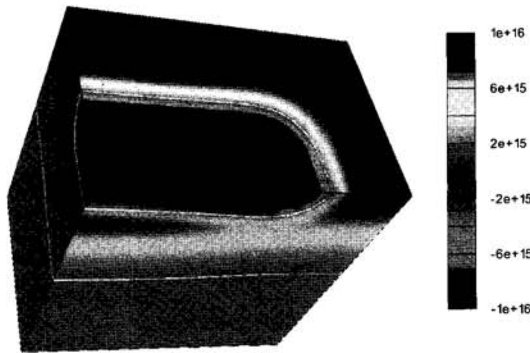

Fig. 2. Netto doping of the finger structure.

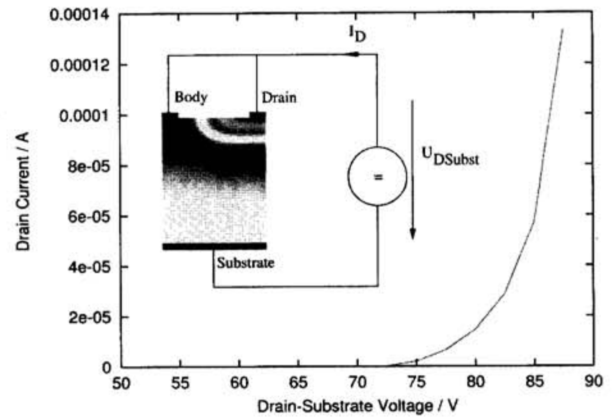

Fig. 3. Two-dimensional punch characteristic.

But more precise tests had shown, even if the main device works fine, the device will breakdown by punch-through at the borderlands of the drain finger. This can be explained by three-dimensional effects at the tip of the drain finger which dominate the device characteristics. Because of the relatively narrow NTUB finger, the diffusion of the implanted ions at the finger's tip takes place spherically, which results in a dilution of the doping compared to the two-dimensional case. Therefore an optimization of these peripheral regions would improve the electric device characteristics.

3 Layout of the drain finger

The mask layout is shown in Figure 1. The SDNTUB region results from the n-implantation through the 2.3 μm wide DNTUB mask in addition with a relatively low blanked donor implantation (SNTUB). Whereas the PTUB finger is implanted with the 2.7 μm equidistantly enlarged surrounding PTUB mask. Because of the longer diffusion width of phosphorus, the PTUB region finally resides inside the SDNTUB region. For insulation the n-region is placed in a p-doped substrate. The resulting netto doping concentration after ion implantation and annealing is shown in Figure 2.

4 Two-dimensional simulation

The two-dimensional PMOS transistor characteristics were simulated by the device simulator DESSIS [1]. For this purpose the three-dimensional structure is cut in the middle of the device (marked as 2D-cut in Fig. 1), at a position from the finger's tip where no three-dimensional effects dominate. With these simulation results the device seemed to fulfill the required guidelines. The breakdown of the device complied with the specified maximum ratings. By simulation the punch-through of the device occurs in the range of 90 V connected between drain and substrate. The simulated punch current depending on the applied drain-substrate voltage can be seen in Figure 3.

5 Verification of the simulation

After building some test examples with layout variations in the area of the drain finger, the measurements had shown a strong correlation with the layout variations. The electric breakdown of some transistors occurred at a much lower voltage, at about 45 V between drain and substrate. This can only be explained by a premature punch behavior occurring in the peripheral regions of the device.

To prove, the three-dimensional borderland was modeled. First the ion implantation was simulated by the three-dimensional implantation simulator MCIMPL [2]. For calculating the final doping profile, two ways seem to be available.

The first and classical method is, to simulate the whole diffusion process, where a very dense grid is required, to get the required resolution of the implantation profile. Next a fully three-dimensional, transient diffusion simulation must be started. Therefore the grid density has to be refined in large regions, because of the huge final well depth of the device. Hence the diffusion simulation reaches the limits of memory consumption of modern computers and demands outrageous cpu-time.

Therefore an alternative method was investigated. Because of the low implantation depth compared to the final well depth, the implanted ions could be assumed as a layer of ions located at the surface of the wafer. Only the dose of the ions has to be preserved. Then the diffusion process can be seen as the sum over all the partial diffusion processes, which can be calculated based on Green's functions theory.

A requirement for applying this method is, the appropriateness of a simple and linear diffusion model. Only in this case an analytical representation of the Green's functions is found. It is only efficient concerning time consumption, if a localized starting diffusion concentration is given. If implantation width and diffusion width get in the same range, the simplification of isolated ion concentrations on the wafer's top is not valid. As consequence the summation over the partial diffusions has to sweep over the exact distribution of the implantation, and calculation time would increase rapidly.

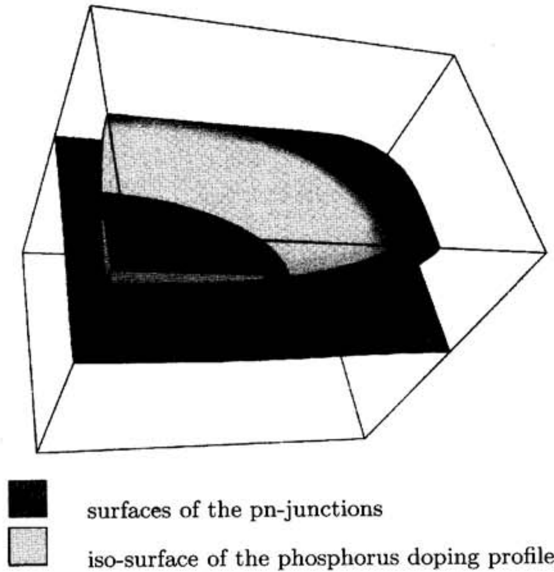

Fig. 4. Short drain finger.

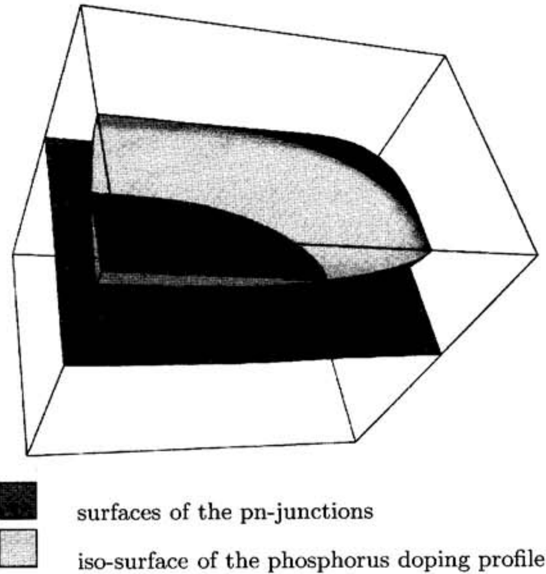

Fig. 5. 2 μm enlarged drain finger.

6 Green's functions

The simple and linear diffusion model can be written as

$$\triangle c(\mathbf{x}, t) = \frac{1}{D} \frac{\partial c(\mathbf{x}, t)}{\partial t} \tag{1}$$

with the distribution of the concentration $c(\mathbf{x}, t)$ depending on time and place, and the diffusion factor D which is assumed to be constant. The diffusion in the wafer is only defined for $z \geq 0$, which can be accounted by mirroring the wafer symmetrically. Then natural boundary conditions can be set.

A solution of this differential equation can be found with Green's functions [3]

$$c(\mathbf{x}, t) = \frac{2}{(4\,\pi D t)^{3/2}} \int_{-\infty}^{\infty} c_0(\mathbf{x}')\, \mathrm{e}^{-\frac{|\mathbf{x}-\mathbf{x}'|^2}{4Dt}}\, \mathrm{d}^3\mathbf{x}'$$

for $t > 0$, where $c_0(\mathbf{x})$ is the initial concentration distribution at time $t = 0$.

Within this special device the initial concentration can be defined as a set of Dirac like concentration points on the wafer's top. Therefore the equation can be written as a sum

$$c(\mathbf{x}, t) = \frac{2}{(4\,\pi D t)^{3/2}} \sum_i d_0(\mathbf{x}'_i)\, \mathrm{e}^{-\frac{|\mathbf{x}-\mathbf{x}'_i|^2}{4Dt}} \tag{2}$$

over all initial concentration points $\mathbf{x}'_i$.

7 Three-dimensional diffusion simulation

For an accurate simulation the three-dimensional doping profile has to be calibrated by the doping concentrations in the symmetry-plane of the two-dimensional profile. With this calibration the diffusion factor D (or more exact, the factor $4Dt$ where the diffusion factor is included) and the initial quantum of dopants are determined

The big advantage of this method is, the device can be optimized in this simulation state, without a rigorous device simulation. The device optimization will be explained, using Figures 4 and 5.

Elongating the drain finger effects only the borderland of the device. The punch-through characteristics of these areas will be improved. Whereas the possibility of impact-ionization at regions at the drain finger's tip at the wafer's surface will grow. Therefore we need a criterion, how much the finger can be elongated. This value is found in a graphical way:

- In Figure 4 the resulting surfaces of the *pn*-junctions is shown. The surface which surrounds the drain finger can also be seen approximately as an iso-surface of the boron concentration.

- The second surface is the phosphorus concentration, which produces the *pn*-junction where the wafer's surface meets the two-dimensional cut-plane.

- The two-dimensional simulation posted the device characteristics within the limits, with respect to punch-through and impact ionization.

- If the second iso-surface gets elongated (by an elongation of the drain finger) as long as it meets the first iso-surface, the two-dimensional behavior results also at the finger's tip, and impact ionization can not occur.

The optimal finger elongation results in 2 μm. The elongated surfaces can bee seen in Figure 5.

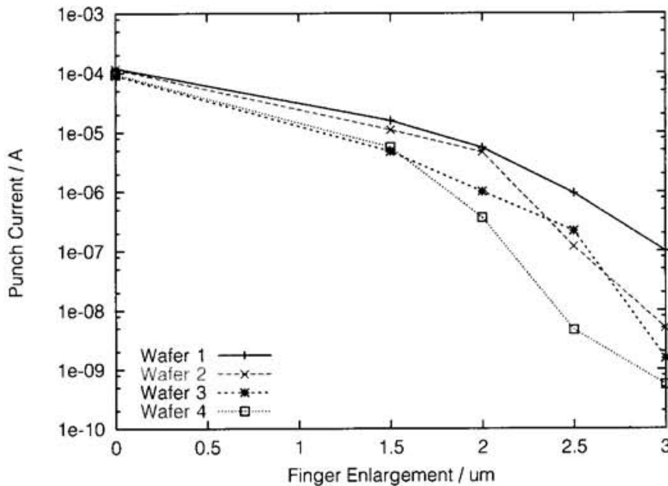

Fig. 6. Measured punch-current of some test examples depending on the finger elongation, at an supplied drain-substrate voltage of 90 V.

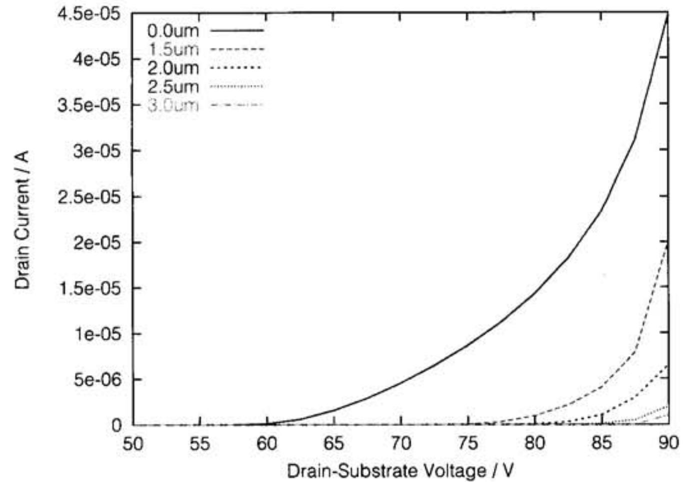

Fig. 7. Three-dimensional device simulations, different finger enlargement shown in different curves.

In Figure 6 the measured correlation between punch current and finger elongation at a constant drain substrate voltage of 90 V is shown, which verifies our considerations.

8 Three-dimensional device simulation

For the verification of these results, a fully three-dimensional device simulation of the finger was performed. The doping profile was also calculated by the discussed Green's function method. The device simulation was carried out with an advanced version of MINIMOS-NT [4], featured for three-dimensional simulations. For the approximation of the device characteristics the Shockley-Read-Hall recombination and the impact ionization models had to be included. The simulated drain current depending on the applied drain-substrate voltage for different finger elongations is shown in Figure 7. Because the PMOS works as a high side switch, the PTUB and SDNTUB contacts were at the same potential and biased against the substrate contact. It can be seen that the current characteristic is shifted to higher voltages by the elongation of the drain finger. The comparison between measurement and simulation is shown in Figure 8. The relatively high difference between simulation and measurement can be explained by an error in the approximation of the diffusion parameters of the two-dimensional profile, which has an significant effect on the punch voltage.

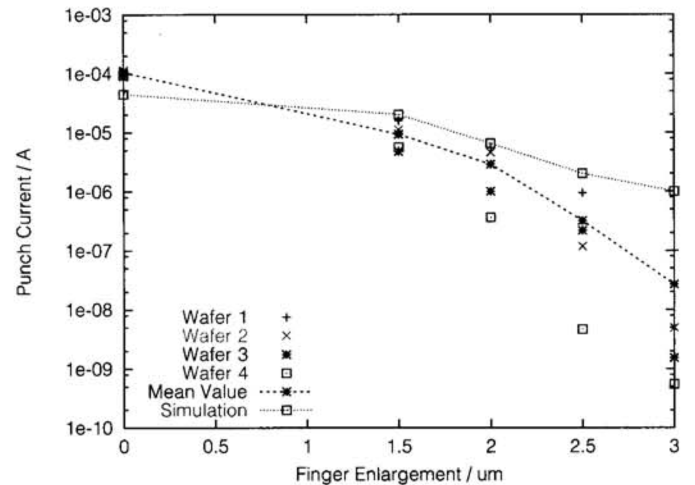

Fig. 8. Simulated punch-current depending on the finger elongation, with an supplied drain-substrate voltage of 90 V, the measured punch-currents are shown as points.

9 Conclusion

Efficient optimization of electric characteristics requires detailed information of the processes. Without the knowledge of the exact location of the punch-through point, the best device simulation often cannot give an answer. Without the special adaption of the diffusion calculation it would not have been possible to fully optimize the given high voltage device.

The authors acknowledge support from the "Christian Doppler Forschungsgesellschaft", Vienna, Austria.

References

1. `http://www.ise.ch/products/dessis`
2. A. Hössinger, *Simulation of Ion Implantation for ULSI Technology*, Dissertation, Technische Universität Wien, 2000, `http://www.iue.tuwien.ac.at/phd/hoessing`
3. H. Dirschmid, *Einführung in die mathematischen Methoden der theorischen Physik* (Vieweg, 1976)
4. T. Binder, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Hosina, R. Mlekus, V. Palakovski, M. Rottinger, G. Schrom, S. Selberherr, M. Stockinger, *MINIMOS-NT User's Guide* (Institut für Mikroelektronik, 1998)