High-Voltage Lateral Trench Gate SOI LDMOSFETs

J.M. Park, R. Klima, and S. Selberherr

Institute for Microelectronics, TU Wien
Gusshausstrasse 27–29, A-1040 Vienna, Austria

Abstract

We present a lateral trench gate SOI LDMOSFET which uses narrow trenches as channels. The lateral trench gate which allows the channel current to flow laterally on the trench side walls decreases its on-resistance, because it increases the current spreading area of the device. The specific on-resistance ($R_{\rm sp}$) strongly depends on the trench depth. The $R_{\rm sp}$ of the suggested devices as a function of the lateral trench depth and the space between the trenches is studied. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the influence of device parameters on the $R_{\rm sp}$ and breakdown voltage. The improvement in the current handling capability of the suggested device is about 8.3% compared to the conventional SOI LDMOSFET.

Keywords: High-voltage devices, SOI LDMOSFETs, lateral trench gate, simulation

I. INTRODUCTION

Smart power integrated circuits have become popular for automotive applications, consumer electronics, telecommunications, and industrial control. These ICs improve the reliability, reduce the volume and weight, and increase the efficiency of the system [1], [2]. Considerable effort has been spent on the development of smart power devices. SOI (Silicon on Insulator) lateral double diffused MOS transistors (LDMOSFETs) are increasingly used as output power devices in smart power applications. Advantages of SOI technology are the superior isolation, reduced parasitic capacitances and leakage currents, and the superior high temperature performance compared to the traditional junction isolation. These advantages allow monolithic integration of multiple power devices and low-voltage control circuitry on the same chip.
The conventional SOI LDMOSFET has the channel regions on the surface. The channel is obtained by a double diffusion process. It has been shown that by proper choice of n-drift doping and length, optimal on-resistance can be achieved for a given breakdown voltage requirement. The trench structure is used only for the isolation of power devices and low-voltage circuitry. New structures such as buried gate oxide devices [3], LUDMOSFETs [4], superjunction [5], and lateral trench gate [6] are proposed to improve the performance of the conventional lateral devices. Most of these structures are focused on the improvement of trade-off between the on-resistance and breakdown voltage.
We present a lateral trench gate SOI LDMOSFET which uses narrow trenches as channels. Contrary to the conventional vertical trench MOSFETs, the lateral trench gate is formed laterally on the side wall of a trench and the channel current flows to the lateral direction through the trench side walls. This gives an increased channel area compared to that of conventional SOI LDMOSFETs. Three-dimensional numerical simulations with MINIMOS-NT [7] have been performed to investigate the influence of device parameters on $R_{\rm sp}$ and breakdown voltage.

II. DEVICE STRUCTURES AND OPERATIONS

Fig. 1 and Fig. 2 show the schematic structures of a conventional LDMOSFET on SOI and a proposed lateral trench gate SOI LDMOSFET which are used for simulation of breakdown voltage and on-resistance, respectively. Generally, the breakdown voltage of the conventional SOI LDMOSFET is limited by the buried oxide thickness, SOI thickness, and drift layer length. Fig. 1 shows a cross-sectional view of a conventional n-channel SOI LDMOSFET designed for breakdown voltage of 100 V with an SOI thickness $t_{\rm soi}$ of 1.5 μm, and with a buried oxide thickness $t_{\rm ox}$ of 1.0 μm. The drift region of the device is doped according to the RESURF principle [8], [9] to achieve a maximum breakdown voltage. To obtain a better trade-off between the breakdown voltage and on-resistance a highly doped n^+ buffer is added at the drain. As shown in Fig. 2, the proposed lateral trench gate SOI LDMOSFET has a similar structure as that of a conventional SOI LDMOSFET except that it has a trench gate on the side wall. Together with the channel on the top of the SOI this gives an increased channel area, and an effective n-drift area (near the

gate edge) which contribute current conduction during on-state is increased. From Fig. 2 it is clear that the channel current flows on the side wall of the trench. With the increased channel area and the effective n-drift area the reduction of the channel resistance can be achieved. The width, space, and depth of the lateral trench gate are 0.4 μm, 1.1 μm and from 0.5 to 1.5 μm, respectively. Simulations are performed for the 100 V lateral trench gate SOI LDMOSFETs with an n-drift length $L_\mathrm{d} = 5.5$ μm and doping $N_\mathrm{D} = 1.0 \times 10^{16}$ cm^{-3}. The other structure parameters are the same as that in Fig. 1.

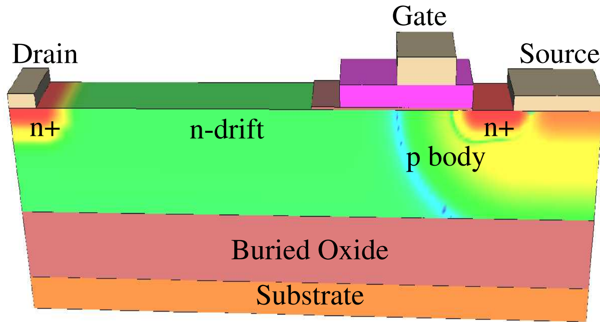

Fig. 1. Conventional LDMOSFET on SOI.

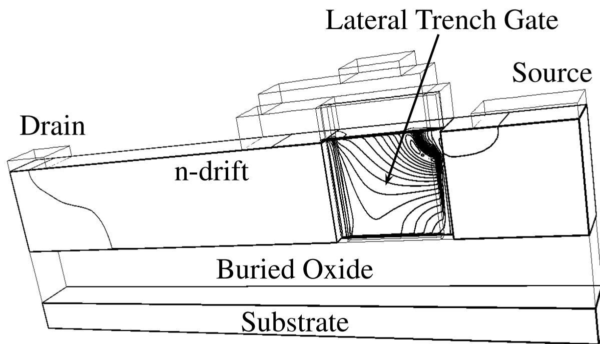

Fig. 2. Proposed lateral trench gate SOI LDMOSFET and current flow iso-lines at $V_\mathrm{GS} = 12$ V and $V_\mathrm{DS} = 2.0$ V.

III. SIMULATION RESULTS AND DISCUSSION

Optimum trade-off between breakdown voltage and R_sp has been the main issue of these devices. R_sp and breakdown voltage are inversely related to each other. Fig. 3 shows the potential distribution of the fully resurfed lateral trench gate SOI LDMOSFET at drain-source voltage V_DS = 110 V. It exhibits similar potential distribution as that of the conventional device, the lateral trench does not affect the RESURF condition. With the same breakdown voltage as the conventional device it helps to decrease the on-resistance by increasing the current spreading area at the channel region. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the breakdown voltage, R_sp, and self-heating effects as a function of the lateral trench depth, and the space between the trenches.

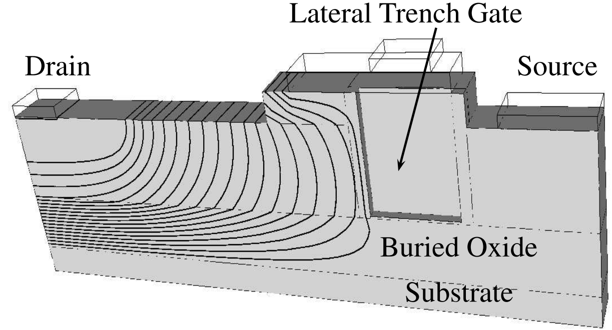

Fig. 3. Potential distribution of a lateral trench gate SOI LDMOSFET at $V_\mathrm{DS} = 110$ V.

A. OFF-STATE CHARACTERISTICS AND SELF-HEATING

Fig. 4 shows the electric field of the conventional SOI LDMOSFET at V_DS = 110 V, higher electric field can be seen at the drain and gate edge near the surface of the SOI. Fig. 5 shows the electric field of the lateral trench gate SOI LDMOSFET at V_DS = 110 V. Contrary to the conventional RESURF SOI LDMOSFETs a higher electric field can be seen at the drain edge and middle of the lateral trench gate. With the n$^+$ buffer at the drain the position of the electric field is moved toward extended drain edge (Fig. 6). At the gate the peak electric field moved from the surface to the middle of the bulk by the lateral trench gate, but it does not affect significantly the RESURF condition of the device. It helps to decrease the peak electric field near the gate edge on the top of the SOI.

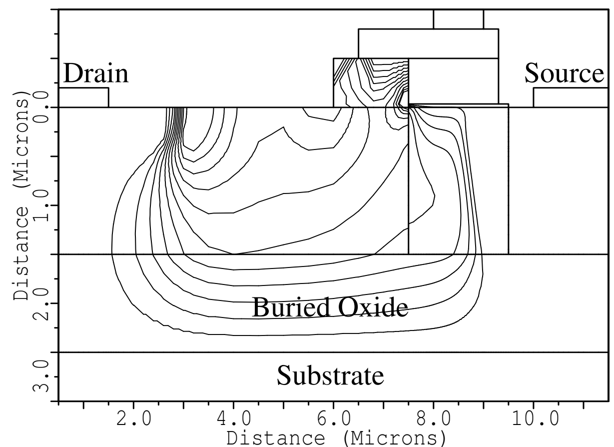

Fig. 4. Electric field of the conventional SOI LDMOSFET at V_DS = 110 V. A higher electric field can be seen at the drain and gate edge near the surface of the SOI.

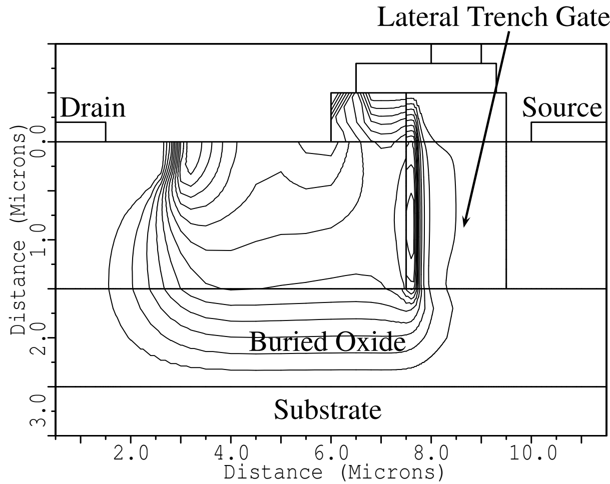

Fig. 5. Electric field of the lateral trench gate SOI LDMOSFET at $V_{\mathrm{DS}} = 110$ V. A higher electric field can be seen at the drain edge and middle of the lateral trench gate.

With the n-drift width of 5.5 μm, the maximum breakdown voltage of the lateral trench gate structure is 117 V with $N_{\mathrm{D}} = 1.0 \times 10^{16}$ cm^{-3}. The breakdown voltage of the conventional SOI LDMOSFET is 112 V with the same doping and structure parameters.

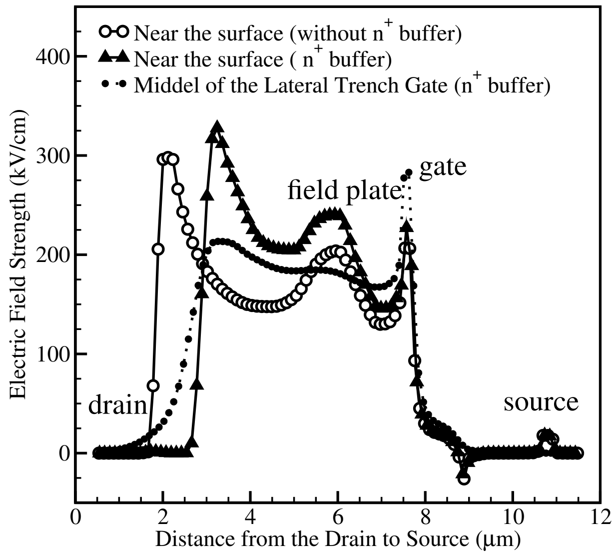

Fig. 6. Comparison of the electric field in the lateral trench gate SOI LDMOSFET along the surface of the SOI and along the middle of the lateral trench gate.

Fig. 7 shows the leakage currents of SOI LDMOSFETs versus drain voltage as a function of the lattice temperature up to 573 K. The leakage current increases nearly exponentially with increasing temperature [10], because the space charge generation rate follows the intrinsic carrier density n_i. The increase of breakdown voltage is caused by the reduction of the mean free path of the carriers due to lattice scattering, requiring higher field for the carriers to initiate impact ionization.

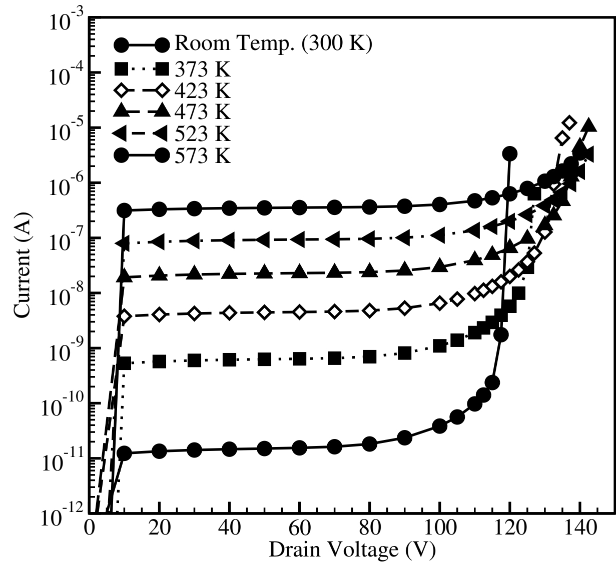

Fig. 7. Breakdown voltage versus lattice temperature of the lateral trench gate SOI LDMOSFET.

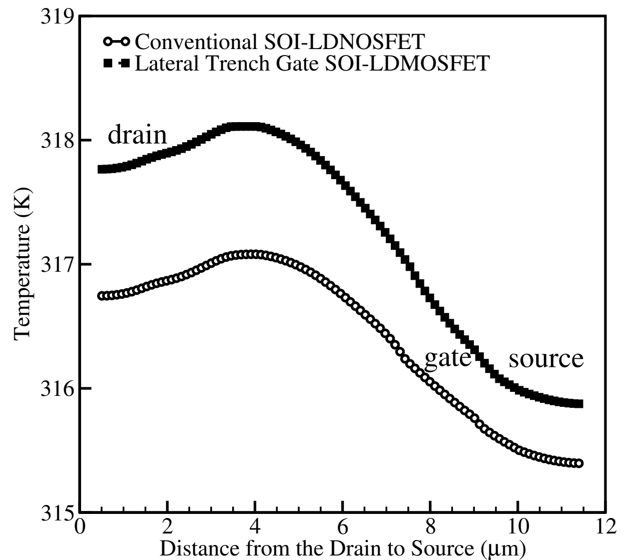

Fig. 8. Comparison of the temperature by self-heating between the conventional and lateral trench gate SOI LDMOSFET near the surface of the SOI.

The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI LDMOSFETs. In majority carrier devices such as MOSFETs, heat generation is mainly caused by Joule heating. It is proportional to the local resistances of the n-drift and channel region. But the channel resistance of the high-voltage devices (generally over 100 V) is not dominant in the on-resistance. Fig. 8 shows the temperature distributions near the SOI surface of the conventional and lateral trench gate SOI LDMOSFETs with an applied gate voltage $V_{\mathrm{GS}} = 12$ V and a drain-source

voltage $V_{\mathrm{DS}} = 2$ V. The bottom of the devices is assumed to be isothermal at 300 K. Because of the lower on-resistance (by increasing the current) of the lateral trench gate structure a higher temperature is obtained at the n-drift region of the lateral trench gate SOI LDMOSFET.

B. ON-STATE CHARACTERISTICS

Fig. 9 and Table 1 show the results of the on-state characteristics of a conventional and a lateral trench gate SOI LDMOSFET. From this figure it becomes clear that the lateral trench gate SOI LDMOSFET has enhanced current handling capability. The on-state characteristics strongly depend on the trench depth and weakly depend on the space between the trenches. The specific on-resistance rapidly decreases with increasing the trench depth, but it does not strongly depend on the space between the trenches. With a trench depth of 0.5 μm and space between the trenches of 0.5 μm the R_{sp} has similar value as that of conventional device. With a trench depth of 1.5 μm the R_{sp} of the device is 264 mΩ mm^{-2} at $V_{\mathrm{GS}} = 12$ V and $V_{\mathrm{DS}} = 0.5$ V. It is about 8.3% smaller than the corresponding R_{sp} value of a conventional SOI LDMOSFET (about 288 mΩ mm^{-2}).

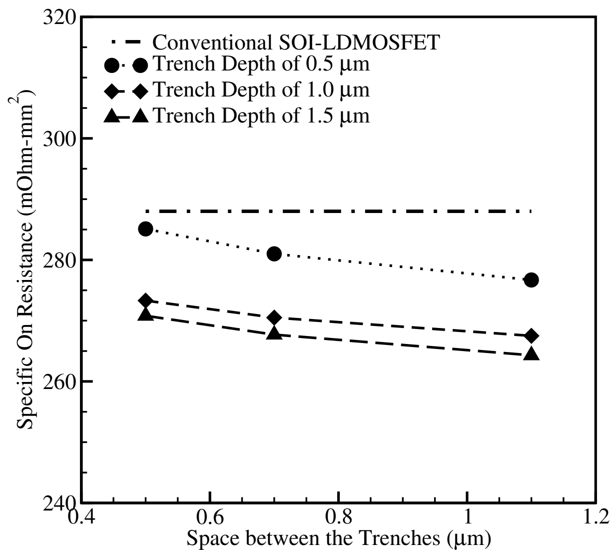

Fig. 9. Comparison the specific on-resistance among the conventional and lateral trench gate SOI LDMOSFETs at $V_{\mathrm{GS}} = 12$ V and $V_{\mathrm{DS}} = 0.5$ V.

Table 1. DC performance comparison between the conventional and the lateral trench gate SOI LDMOSFET.

	Conventional LDMOSFET on SOI	Lateral trench gate SOI LDMOSFET
N_{D}, cm^{-3}	1.0×10^{16}	1.0×10^{16}
L_{d}, μm	5.5	5.5
R_{sp}, mΩ mm^{-2}	288	264
BV, V	112	117

IV. CONCLUSIONS

A lateral trench gate LDMOSFET transistor on SOI is proposed. A lower specific on-resistance is obtained in the suggested structure compared to that of a conventional SOI LDMOSFET. With a lateral trench gate our three-dimensional simulations confirm that it is possible to get the best trade-off between the BV and R_{sp} of the LDMOSFET on SOI. The specific on-resistance strongly depends on the trench depth. It decreases with increasing the trench depth, but the space between the trenches dose not affect the on-resistance. Simulations are performed for the 100 V lateral trench gate SOI LDMOSFETs with an n-drift length $L_{\mathrm{d}} = 5.5$ μm and doping N_{D} = 1.0×10^{16} cm^{-3}. With a lateral trench depth of 1.5 μm a lower R_{sp} of 264 mΩ mm^{-2} is obtained.

REFERENCES

[1] B. Murari, F. Bertotti, and G. A. Vignola, *Smart Power ICs*, Springer-Verlag, 1996.

[2] A. Nakagawa, "Recent Advances in High Voltage SOI Technology for Motor Control and Automotive Application," in *Proc. of Intl. Bipolar/BiCMOS Circuits and Technology Meeting*, pp.69-72, 1996.

[3] T. Uesugi, M. Kodama, S. Kawaji, K. Nakashima, Y. Murase, E. Hayashi, Y. Mitsushima, and H. Tadano, "New 3-D Lateral Power MOSFETs with Ultra Low On-Resistance," in *Proc. of 10th Intl. Symp. Power Semiconductor Devices & ICs(ISPSD)*, pp.57-60, 1998.

[4] M. Zitouni, F. Morancho, P. Rossel, H. Tranduc, J. Buxo, and I. Pages, "A New Concept for the Lateral DMOS Transistor for Smart Power IC's," in *Proc. of 11th Intl. Symp. Power Semiconductor Devices & ICs(ISPSD)*, pp.73-76, 1999.

[5] T. Fujihira and Y. Miyasaka, "Simulated Superior Performances of Semiconductor Superjunction Devices", *Proc. of 10th Intl. Symp. Power Semiconductor Devices & ICs(ISPSD)*, 1998, pp. 423-426.

[6] Y. Kawaguchi, T. Sano, and A. Nakagawa, "20V and 8V Lateral Trench Gate Power MOSFETs with Record-Low On-resistance", *Proc. of Intl. Electron Devices Meeting(IEDM), Technical Digest*, 1999, pp. 197-200.

[7] Institute for Microelectronics, TU Wien, "MINIMOS-NT", 2001.

[8] A. W. Ludikhuize, "A Review of RESURF Technology," in *Proc. of 12th Intl. Symp. Power Semiconductor Devices & ICs(ISPSD)*, pp.11-18, 2000.

[9] E. Arnold, "Silicon-on-Insulator Devices for High Voltage and Power IC Applications," *J. Electrochem. Soc.*, Vol. 141, No. 7, pp.1983-1988, 1994.

[10] Y. K. Leung, Y. Suzuki, K. E. Goodson, and S. S. Wong, "Self-Heating Effect in Lateral DMOS on SOI," in *Proc. of 7th Intl. Symp. Power Semiconductor Devices & ICs(ISPSD)*, pp.138-140, 1995.

Jong Mun Park, Robert Klima, and Siegfried Selberherr
Institute for Microelectronics, TU Wien
Gusshausstrasse 27–29, A-1040 Vienna, Austria
Email: park@iue.tuwien.ac.at