Analysis of Gate Dielectric Stacks Using the Transmitting Boundary Method

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Gate stacks of high-κ dielectrics have been proposed to enable MOSFET effective oxide thickness scaling below 2 nm. Simulation of such devices requires the calculation of tunneling through non-triangular energy barriers. The tunneling current through an energy barrier of arbitrary shape is

$$J_\mathrm{g} = \frac{4\pi m_\mathrm{eff}\mathrm{q}}{h^3}\int_0^\infty TC(\mathcal{E}_\mathrm{t})\int_0^\infty \left[f_1(\mathcal{E}_\mathrm{t}+\mathcal{E}_\mathrm{l}) - f_2(\mathcal{E}_\mathrm{t}+\mathcal{E}_\mathrm{l}+\Delta\mathcal{E}_\mathrm{C})\right]\,\mathrm{d}\mathcal{E}_\mathrm{l}\,\mathrm{d}\mathcal{E}_\mathrm{t} \qquad (1)$$

where $TC(\mathcal{E}_\mathrm{t})$ is the transmission coefficient, $\mathcal{E}_\mathrm{l}$ and $\mathcal{E}_\mathrm{t}$ the longitudinal and transversal energy component, f_1 and f_2 the energy distribution functions in the gate and substrate, and $\Delta\mathcal{E}_\mathrm{C}$ the difference in the conduction band edges. The quantum-mechanical transmission coefficient can be derived using several techniques. While the WKB and Gundlach methods assume a triangular or trapezoidal barrier, the transfer-matrix method is based on a segmentation of an arbitrary-shaped energy barrier into a series of constant- or linear-potential segments as shown in Fig. 1. Alternatively, the quantum transmitting boundary method (QTBM) can be used, where open boundary conditions are introduced by [1]

$$\begin{aligned} \Psi_1 &= a_1 + b_1, & \Psi_0 &= a_1\exp(-ik_1\Delta) + b_1\exp(ik_1\Delta) \\ \Psi_n &= a_n + b_n, & \Psi_{n+1} &= a_n\exp(-ik_n\Delta) + b_n\exp(ik_n\Delta) \end{aligned} \qquad (2)$$

which allow Schrödinger's equation to be solved by standard techniques. The different numerical methods have been compared to study their applicability for the evaluation of high-κ dielectric stacks. Fig. 2 shows the transmission coefficient of a typical 2 nm stack, with the shape of the barrier and the squared wave function at an energy of 2.8 eV in the inset. The WKB and Gundlach methods, which approximate the barrier with a straight line, overestimate the transmission coefficient as compared to the transfer-matrix based methods, which show good agreement with the transmitting boundary method. The transfer-matrix based methods, however, cannot be used for thicker dielectrics as shown in Fig. 3 for a 3 nm SiO_2 gate oxide due to numerical instabilities at low energies (≈ 0.6 eV in this case). It was found that these methods become unstable due to rounding errors if the decay factor $\sum k_j\Delta$ exceeds a certain value ($\approx$20 in our simulations).

The transmitting boundary method, on the other hand, delivers accurate results and remains stable even for large stacks. It has therefore been implemented into the device simulator MINIMOS-NT and applied for the evaluation of gate dielectric stacks in a 50 nm 'well-tempered' MOSFET [2]. Retaining the effective gate oxide thickness of 2 nm we replaced the dielectric by a stack consisting of an underlying SiO_2 layer and a high-κ dielectric on top. The electron concentration in the stack (see Fig. 4) was taken into account in the Poisson equation. Using the material parameters listed in Fig. 5 the gate current was calculated at the bias point V_DS=0 V and V_GS=2 V for different thicknesses of the SiO_2 layer, see Fig. 6. Most of the materials yield even an increased gate current which can be explained by the trade-off between barrier height and barrier thickness. Only ZrO_2 and Al_2O_3 show considerably lower leakage than SiO_2 and may therefore be considered as viable high-κ dielectrics for future CMOS technologies.

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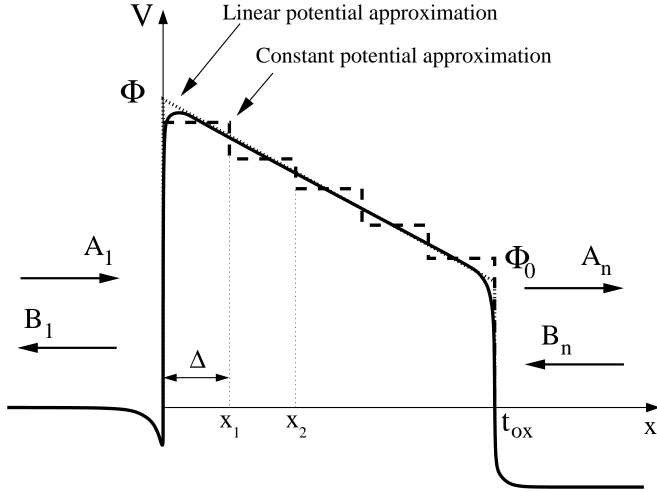

Figure 1: The energy barrier for the linear and constant potential transfer-matrix method.

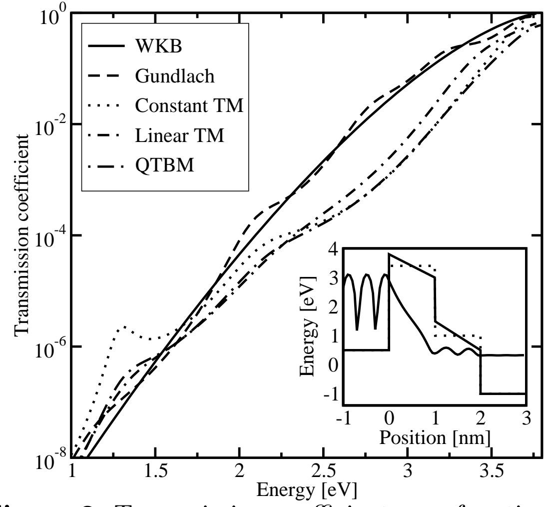

Figure 2: Transmission coefficient as a function of energy for a typical gate stack.

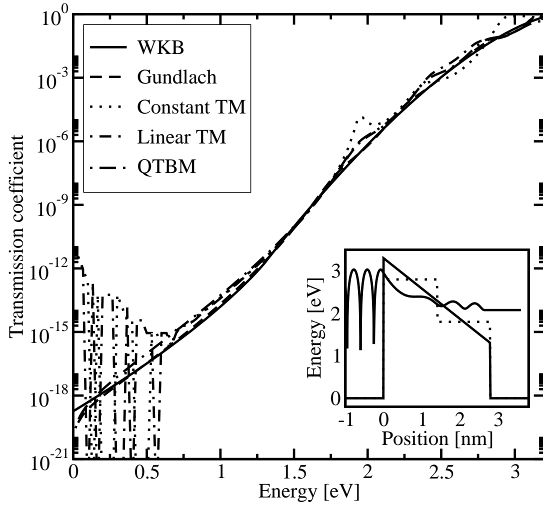

Figure 3: Transmission coefficient as a function of energy for a 3 nm thick layer of SiO_2.

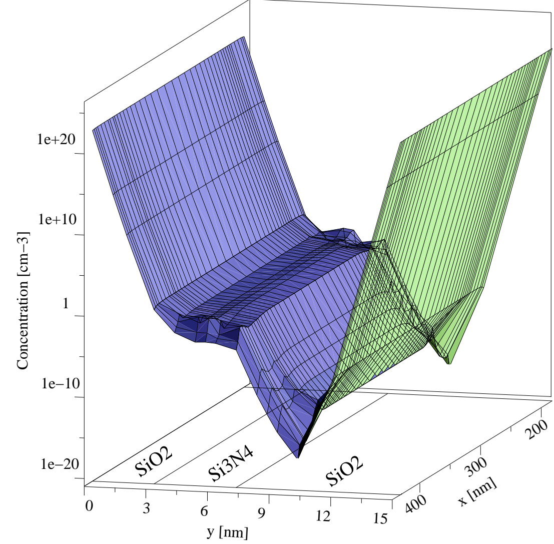

Figure 4: The electron concentration in a SiO_2-Si_3N_4-SiO_2 gate stack.

	κ [As/Vm]	Band gap [eV]	Band offset [eV]
Si	11.9	1.17	—
SiO_2	3.9	9.00	3.18
Si_3N_4	7.5	5.00	2.00
Ta_2O_5	25.0	4.40	1.40
TiO_2	40.0	3.50	1.10
Al_2O_3	7.9	5.60	3.50
ZrO_2	25.0	7.80	1.90
HfO_2	25.0	5.80	1.13
Y_2O_3	18.0	5.50	1.30

Figure 5: Material parameters of commonly used dielectrics, compared to silicon [3, 4].

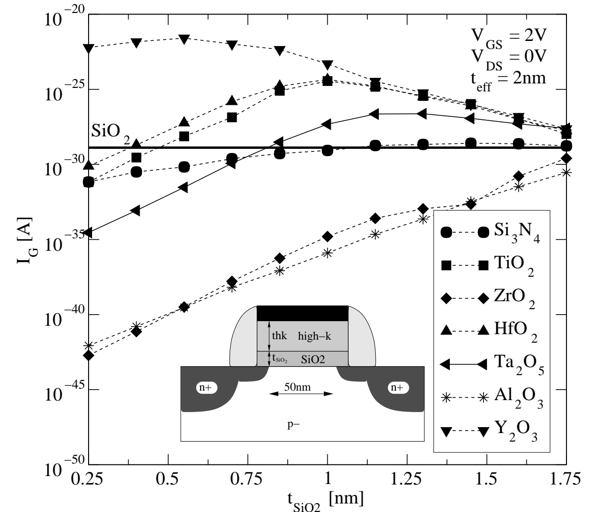

Figure 6: Gate current as a function of SiO_2 layer thickness at V_{DS}= 0 V and V_{GS}= 2 V.