2 LAX, B., and NEUSTADTER, T.: 'Transient response of a p–n junction', *J. Appl. Phys.*, 1954, **25**, pp. 1148–1154
3 LEVINSHTEIN, M.E., MNATSAKANOV, T.T., IVANOV, P.A., PALMOUR, J.W., RUMYANTSEV, S.L., SINGH, R., and YURKOV, S.N.: 'Paradoxes of carrier lifetime measurements in high-voltage SiC diodes', *IEEE Trans. Electron Devices*, 2001, **48**, pp. 1703–1710
4 KIMOTO, N.T., MIYAMOTO, N., and MATSUNAMI, H.: 'Performance limiting surface defects in SiC epitaxial p–n junction diodes', *IEEE Trans. Electron Devices*, 1999, **46**, pp. 471–477
5 GOSSIK, B.R.: 'About recovery characteristics of semiconductor rectifiers', *J. Appl. Phys.*, 1956, **27**, pp. 905–910
6 SCHLANGENOTTO, H., and GERLACH, W.: 'On the post-injection voltage decay of the p–s–n rectifiers at high injection levels', *Solid-State Electron.*, 1972, **15**, pp. 393–402
7 LEVINSHTEIN, M.E., RUMYANTSEV, S.L., and SHUR, M.S.: 'Properties of advanced semiconductor materials GaN, AlN, InN, BN, SiC, SiGe' (John Wiley & Sons Inc, New York, 2001)
8 IVANOV, P.A., LEVINSHTEIN, M.E., IRVIN, K.G., KORDINA, O., PALMOUR, J.W., RUMYANTSEV, S.L., and SINGH, R.: 'High hole lifetime (3.8 μs) in 4H-SiC diodes with 5.5 kV blocking voltage', *Electron. Lett.*, 1999, **35**, pp. 1382–1383
9 NOSOV, YU.R.: 'Physical foundations of the pulse semiconductor diode operation' ('Nauka' Publishing House, Moscow, 1968)
10 SCE, S.M.: 'Physics of semiconductor devices' (John Wiley & Sons Inc, New York, 1981)
11 ELASSER, M., CHEZZO, M., KRISHNAMURTHY, N., KRETCHMER, J., CLOCK, A.W., BROWN, D.M., and CHOW, T.P.: 'Switching characteristics of silicon carbide power pin diodes', *Solid-state Electron.*, 2000, **44**, pp. 317–323
12 STREL'CHUK, A.M., and SAVKINA, N.S.: 'Ideal 4H-SiC pn junction and its characteristic shunt', *Mater. Sci. Eng.*, 2001, **B80**, pp. 378–382

Energy transport gate current model accounting for non-Maxwellian energy distribution

A. Gehring, T. Grasser, H. Kosina and S. Selberherr

A new formulation to describe hot-electron tunnelling through dielectrics is presented. It is based on an expression for the electron energy distribution function which is characterised by its first three even moments. The model is simplified to make it applicable for energy-transport simulations, yielding a modified supply function in Tsu-Esaki's equation. Simulations show excellent agreement with Monte Carlo results.

The accurate prediction of gate oxide tunnelling currents is of increasing importance for today's miniaturised semiconductor devices. The high electric field in the channel of contemporary sub-100 nm MOSFETs however, forbids the use of models which are based on the local electric field alone: the shape of the electron energy distribution function (EED) has to be taken into account explicitly. This is problematic as the EED in the channel of a MOSFET significantly deviates from the Maxwellian shape. Transport models which are based on six moments of Boltzmann's equation have been successfully used to get information about the distribution of electrons in the channel [1, 2]; however, they are computationally demanding [3]. We therefore suggest a new model which is suitable for energy-transport simulations.

According to [4] the tunnelling current density through a dielectric layer can be written as

$$J_g = \frac{4\pi m_{ox} q}{h^3} \int_0^\infty TC(\mathcal{E}_t) N(\mathcal{E}_t)\, d\mathcal{E}_t \tag{1}$$

where $TC(\mathcal{E}_t)$ is the tunnelling probability and $N(\mathcal{E}_t)$ the supply function which is defined as

$$N(\mathcal{E}_t) = \int_0^\infty [f_1(\mathcal{E}_t + \mathcal{E}_l) - f_2(\mathcal{E}_t + \mathcal{E}_l + \Delta E_c)]\, d\mathcal{E}_l \tag{2}$$

Here, the total energy $\mathcal{E}$ is the sum of a longitudinal component $\mathcal{E}_l$ and a transversal component $\mathcal{E}_t$ which is perpendicular to the substrate-oxide interface. The electron energy distribution functions in the gate and substrate are denoted by f_1 and f_2, and the difference in the conduction band edges is $\Delta E_C = E_{C,1} - E_{C,2}$. For the case of a Fermi-Dirac distribution the gate current density evaluates as

$$J_g = \frac{4\pi m_{ox} q k_B T}{h^3} \int_0^\infty TC(\mathcal{E}_t) \ln\left[\frac{1 + \exp(\mathcal{E}_f - \mathcal{E}_t / k_B T)}{1 + \exp(\mathcal{E}_f' - \mathcal{E}_t / k_B T)}\right] d\mathcal{E}_l \tag{3}$$

where $\mathcal{E}_f$ and $\mathcal{E}_f'$ denote the Fermi energies at the semiconductor-oxide interfaces. This expression is frequently used in the literature and implemented in all common device simulators.

However, in the channel of a turned-on sub-quartermicron MOSFET, the assumption of a Fermi-Dirac distribution is not valid. Even for moderate drain bias, the EED shows a pronounced high energy tail as shown in Fig. 1 for a 500 nm MOSFET device biased at $V_{DS} = V_{GS} = 1$ V. Assuming a heated Maxwellian EED which only depends on the electron temperature leads to a completely wrong distribution of electrons.

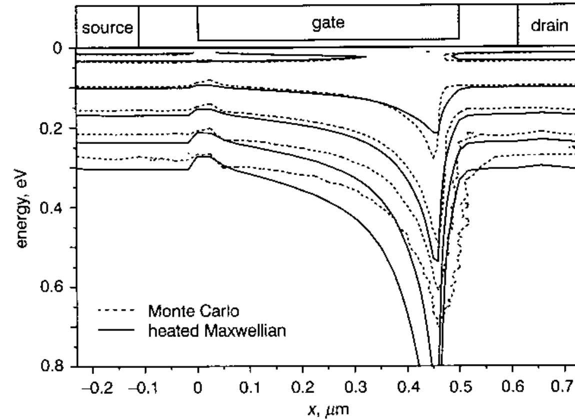

Fig. 1 *Contour lines of heated Maxwellian EED at semiconductor-oxide interface compared to results of Monte Carlo simulations*
Neighbouring lines differ by a factor of 10

We therefore propose to use a recently developed [2] expression for the EED. That allows us to rigorously account for the shape of the EED in the channel and in the poly gate. We follow the approach presented by Cassi and Riccò [5] who suggested using

$$f_1(\mathcal{E}_t) = A \exp\left[-\left(\frac{\mathcal{E}_t}{a}\right)^b\right] \tag{4}$$

to describe the EED in the channel. With this expression and the assumption of a Fermi-Dirac EED in the poly gate, the supply function (2) becomes

$$N(\mathcal{E}_t) = A_1 \frac{a}{b} \Gamma_i\left[\frac{1}{b}, \left(\frac{\mathcal{E}_t}{a}\right)^b\right] - A_2 k_B T_D \ln\left[1 + \exp\left(-\frac{\mathcal{E}_t + \Delta E_c}{k_B T_L}\right)\right] \tag{5}$$

where $\Gamma_i(\alpha, \beta)$ denotes the incomplete gamma function. The values of A_1 and A_2 can be determined from the local carrier concentration, while the values of a and b can be found from the electron temperature T_n and the electron kurtosis β_n using a six moments transport model [2]. This method, however, is computationally expensive and may not be feasible for everyday TCAD applications. We therefore approximate the kurtosis β_n by an expression obtained from bulk silicon where a fixed relationship between β_n, T_n and the lattice temperature T_L exists:

$$\beta_{bulk}(T_n) = \frac{T_L^2}{T_n^2} + 2\frac{\tau_\beta}{\tau_\epsilon}\frac{\mu_S}{\mu_n}\left(1 - \frac{T_L}{T_n}\right) \tag{6}$$

In this expression τ_β, τ_ϵ, μ_S and μ_n are the kurtosis relaxation time, the energy relaxation time, the energy flux mobility, and the electron mobility, respectively. We used a fit to Monte Carlo data for homogeneously doped bulk silicon for τ_β/τ_ϵ [2]. Thus, the self-consistent approach can be used within the energy-transport model. As the influence of the band structure was found to be negligible we restrict ourselves to the parabolic case where we find [6]

$$T_n = \frac{2}{3}\frac{\Gamma(5/2b)}{\Gamma(3/2b)}\frac{a}{k_B} \quad (7)$$

$$\beta_n = \frac{3}{5}\frac{\Gamma(3/2b)\Gamma(7/2b)}{\Gamma(5/2b)^2} \quad (8)$$

Expression (7) can be easily inverted to find $a(T_n)$ whereas the inversion of (8) to find $b(T_n)$ at $\beta_n(b) = \beta_{bulk}(T_n)$ cannot be given in a closed form. We therefore used the fit expression $b(T_n) = 1 + b_0 z^{b_1} + b_2 z^{b_3}$ with $z = 1 - T_L/T_n$ and the parameters $b_0 = 38.82$, $b_1 = 101.11$, $b_2 = 3.40$, and $b_3 = 12.93$. Using $a(T_n)$ and $b(T_n)$ the Monte Carlo EED can be reproduced without knowledge of β_n as shown in Fig. 2.

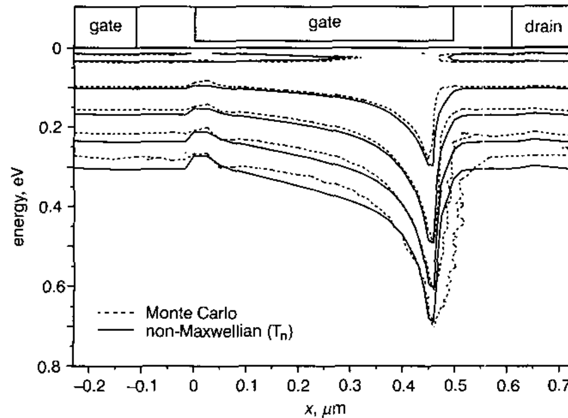

Fig. 2 *Contour lines of non-Maxwellian EED at semiconductor-oxide interface using local parameters $a(T_n)$ and $b(T_n)$ compared to results of Monte Carlo simulations*

Neighbouring lines differ by a factor of 10

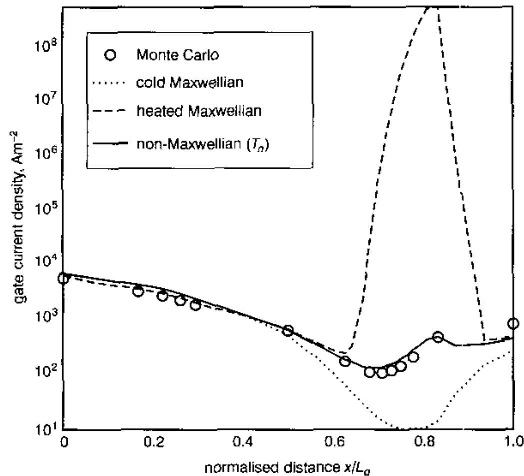

Fig. 3 *Gate current density along channel of MOSFET with 90 nm gate length and 2 nm oxide thickness. Comparison of heated and cold Maxwellian approximation with new model and Monte Carlo results*

Fig. 3 shows the resulting gate current density applying the WKB approximation to evaluate the tunnelling coefficient for a 90 nm MOSFET device with 2 nm oxide thickness and Monte Carlo results for comparison. Our model yields excellent agreement, while the heated Maxwellian approximation substantially overestimates the gate current density especially near the drain region. Instead of the heated Maxwellian EED it may even be better to use a cold Maxwellian EED in that regime. The resulting gate current is shown in Fig. 4 for a 500 nm EEPROM device with an oxide thickness of 4 nm. For low gate voltages the electron temperature is high and the heated Maxwellian approximation massively overestimates the total gate current. As the gate voltage increases, the peak electric field in the channel is reduced. Hence, the high energy tail is suppressed and the models deliver similar results. The new model correctly reproduces the Monte Carlo results. It is thus well suited for the implementation in device simulators solving the energy-transport model.

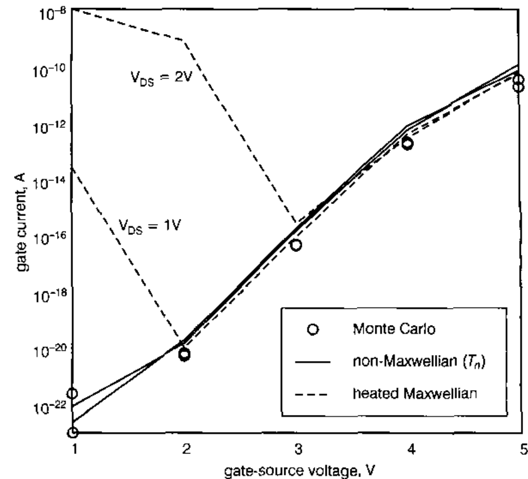

Fig. 4 *Gate current of 500 nm MOSFET with 4 nm oxide thickness. Comparison of heated Maxwellian approximation with new model and Monte Carlo results*

© IEE 2003
16 January 2003
Electronics Letters Online No: 20030440
DOI: 10.1049/el:20030440

A. Gehring, T. Grasser, H. Kosina and S. Selberherr (*Institute for Microelectronics, TU Vienna, Gusshausstrasse 27–29, A-1040 Vienna, Austria*)

References

1 GRASSER, T., KOSINA, H., GRITSCH, M., and SELBERHERR, S.: 'Using six moments of Boltzmann's transport equation for device simulation', *J. Appl. Phys.*, 2001, **90**, (5), pp. 2389–2396
2 GRASSER, T., KOSINA, H., HEITZINGER, C., and SELBERHERR, S.: 'Characterization of the hot electron distribution function using six moments', *J. Appl. Phys.*, 2002, **91**, (6), pp. 3869–3879
3 GEHRING, A., GRASSER, T., KOSINA, H., and SELBERHERR, S.: 'Simulation of hot-electron oxide tunnelling current based on a non-Maxwellian electron energy distribution function', *J. Appl. Phys.*, 2002, **92**, (10), pp. 6019–6027
4 TSU, R., and ESAKI, L.: 'Tunnelling in a finite superlattice', *Appl. Phys. Lett.*, 1973, **22**, (11), pp. 562–564
5 CASSI, D., and RICCÒ, B.: 'An analytical model of the energy distribution of hot electrons', *IEEE Trans. Electron Devices*, 1990, **37**, (6), pp. 1514–1521
6 GRASSER, T., KOSINA, H., and SELBERHERR, S.: 'Influence of the distribution function shape and the band structure on impact ionization modeling', *J. Appl. Phys.*, 2001, **90**, (12), pp. 6165–6171

$HfO_2/HfSi_xO_y$ high-K gate stack with very low leakage current for low-power poly-Si gated CMOS application

C.W. Yang, Y.K. Fang, S.F. Chen, M.F. Wang, T.H. Hou, Y.M. Lin, L.G. Yao, S.C. Chen and M.S. Liang

Poly-Si gated NMOSFETs, with $HfO_2/HfSi_xO_y$ gate stacks for CMOS low-power application are reported for the first time. Compared to an SiO_2 control sample, the $HfO_2/HfSi_xO_y$ stack with equivalent oxide thickness of about 18 Å exhibits four-orders of magnitude reduction in gate leakage at $V_g = 1$ V. Additionally, negligible hysteresis and comparable subthreshold swing are observed, indicating good interface quality and bulk film properties. Furthermore, the stack-caused inherent transconductance degradation is small; almost 66% of the normalised peak transconductance with respect to SiO_2 can be reached.