Evaluation of ZrO_2 Gate Dielectrics for Advanced CMOS Devices

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Abstract

We discuss modeling issues of ZrO_2 insulating layers fabricated by metal-organic chemical vapor deposition (MOCVD). Tunneling through such layers cannot be described within the established Tsu-Esaki model due to the presence of a strong trap-assisted tunneling component. Trap energy levels and concentrations can be extracted from the time constants of the measured trap charging and decharging processes. A trap concentration of 4.5×10^{18} cm^{-3} with a trap energy level of 1.3 eV below the ZrO_2 conduction band edge was found for the considered layer. The parameters are used to simulate a 50 nm 'well-tempered' MOSFET and the influence of the high-κ dielectric on the threshold voltage was studied. Two counteracting effects are found: while the fringing fields from the drain contact reduce the threshold voltage, the presence of traps in the dielectric can lead to a strong increase of the threshold voltage.

1. Introduction

Gate dielectric stacks of high-κ dielectrics have been proposed to enable the reduction of MOSFET effective oxide thicknesses below 2 nm which is necessary to allow further device scaling. Several materials have been suggested to act as alternative dielectrics, such as Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, or ZrO_2. Apart from thermodynamic stability, interface quality, and reliability, the dielectric permittivity and the barrier height are of utmost importance as they influence the gate current density through the layer [1]. Unfortunately, alternative dielectrics show a pronounced tradeoff between the permittivity and the barrier height. Simulations have shown that ZrO_2 promises good performance as compared to other materials [2]. In this paper the performance of ZrO_2 dielectric layers is studied by simulations based on static and transient measurements of ZrO_2 layers. Section 2 describes layer formation while Sections 3 and 4 are dedicated to the static and transient measurements. In Section 5 a 'well-tempered' MOSFET is studied by means of device simulation using the parameters of the investigated layers, and Section 6 presents conclusions.

2. Device Preparation

ZrO_2 pMOS capacitors have been fabricated by MOCVD on p-type (100) silicon wafers with an acceptor doping of 1.5e18 cm^{-3} and Al gate electrodes. A horizontal hot-wall reactor equipped with a bubbler system for metal-organic precursor delivery was employed, see Fig. 1. Zr(tfacac)4 was selected as precursor substance. It shows advanced stability towards hydrolysis compared to other possible precursor materials such as Zr(Ot-Bu)4 and has sufficient volatility for delivery at moderate bubbler temperatures. The already present Zr-O bonds in the precursor molecule also promote the formation of high quality thin films. The silicon substrates were subjected to a modified RCA-clean immediately prior to deposition including an HF dip to remove the native oxide and passivate the substrate surface. During the thin film deposition oxygen was supplied in addition to the argon carrier gas flow to support the decomposition of the precursor to zirconium oxide. All depositions were performed at a temperature of 450°C. Gas flow rates were optimized in regard to the chemical composition of the product. Atmospheres of forming gas (10% hydrogen in nitrogen) and diluted oxygen (20% oxygen, 80% nitrogen) were employed as exemplary reducing (forming gas) and oxidizing (diluted oxygen) conditions in post-deposition annealing at 650°C [3].

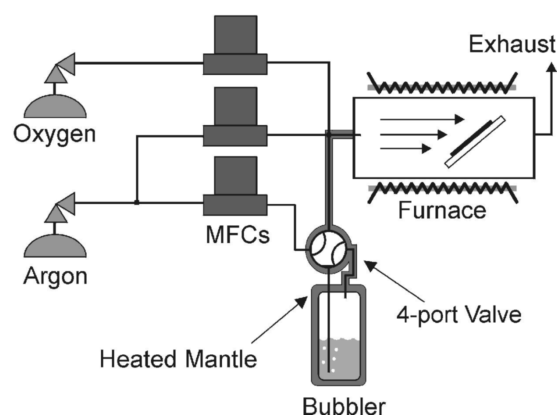

Figure 1. MOCVD deposition scheme

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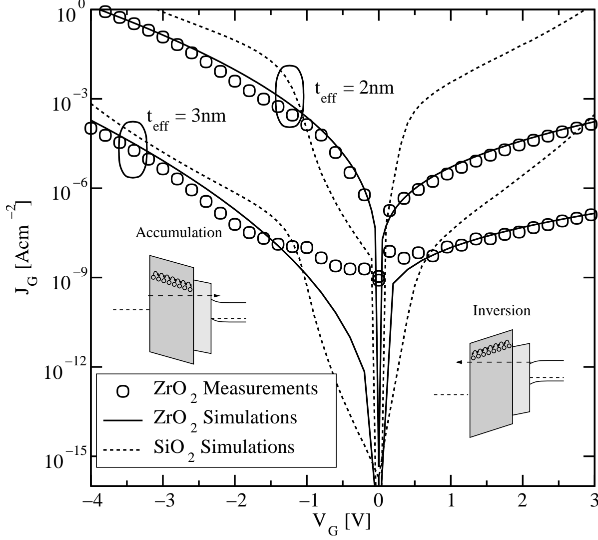

Figure 2. Static gate current measurements of the ZrO_2 layers compared with simulations.

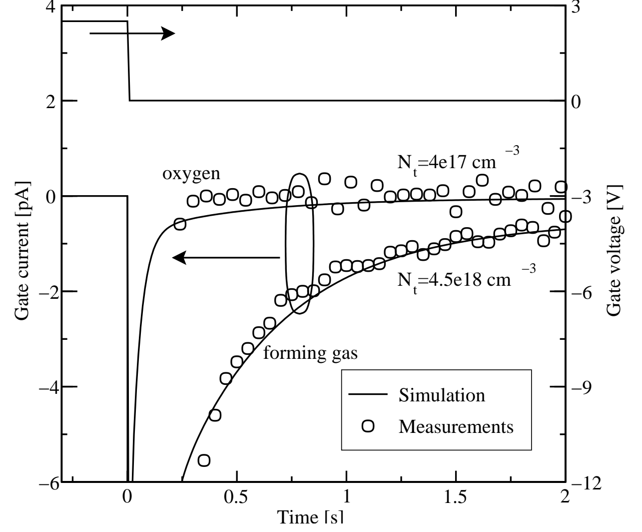

Figure 3. Transient gate current of the dielectrics annealed under reducing and oxidizing conditions.

The overall thicknesses of the dielectric layers has been evaluated by spectroscopic ellipsometry. Employing a relative permittivity of the high-κ material itself of κ=18, which has been found for thicker films, the comparison of optical measurements and the results of C-V characterization implicates the presence of an interfacial layer with a permittivity in the range of 4 to 8. Table 1 summarizes the results of an evaluation of the thicknesses of the high-κ films and interfacial layers. Also given is the effective oxide thickness $t_{\mathrm{eff}} = t_{\mathrm{int}}\kappa_{\mathrm{s}}/\kappa_{\mathrm{int}} + t_{\mathrm{hk}}\kappa_{\mathrm{s}}/\kappa_{\mathrm{hk}}$ where t_{int} and t_{hk} are the thicknesses of the interface and the high-κ layer, and κ_{int}, κ_{s}, and κ_{hk} the permittivities of the interface layer, silicon dioxide, and the high-κ dielectric.

Table 1. Layer thicknesses of the deposited layers in nm.

t_{phys}	t_{int}	t_{hk}	t_{eff}
6.9	0.75 – 2.0	6.15 – 4.9	2.0
12.7	0.3 – 1.0	12.4 – 11.7	3.0

3. Modeling of Static Tunneling

The band diagram of ZrO_2 dielectrics deposited on silicon shows a two-step energy barrier due to the presence of a thin layer of Zr-silicate at the interface between ZrO_2 and silicon. We assume a band gap of the ZrO_2- and Zr-silicate layer of 5.7 eV and 4.5 eV, respectively, with a conduction band offset of 1.5 eV for ZrO_2 and 0.8 eV for the Zr-silicate [4]. For the calculation of tunneling current through the layer we used the the general-purpose device simulator MINIMOS-NT and applied the Tsu-Esaki method, for which the tunnel current density is

$$J = \frac{4\pi m_{\mathrm{ox}} q \mathrm{k_B} T}{h^3} \int_{\mathcal{E}_{\mathrm{min}}}^{\infty} TC(\mathcal{E}) N(\mathcal{E}) d\mathcal{E} \qquad (1)$$

where m_{ox} is the effective electron mass in the oxide, $\mathcal{E}_{\mathrm{min}}$ the lower of the two conduction band edges next to the oxide, $TC(\mathcal{E})$ the transmission coefficient, and $N(\mathcal{E})$ the supply function which is calculated using Fermi-Dirac statistics. The transmission coefficient $TC(\mathcal{E})$ can be calculated using several methods, such as the transfer-matrix or transmitting-boundary method. However, since the transfer-matrix method showed numerical instabilities we employed the transmitting-boundary method as described in [**?**].

Fig. 2 shows the measured gate current for the two dielectric layers, with the approximate shape of the energy barrier shown in the insets. As reference, the figure also shows the gate current for a 2 nm and a 3 nm SiO_2 layer (dotted lines). As expected, the measured current density is lower than for the SiO_2 counterparts. However, the tunnel current predicted by the Tsu-Esaki model for the ZrO_2 layer could not reproduce the measurements as it yielded tunneling currents orders of magnitude lower than the measurements. We explain this failure of the Tsu-Esaki model by the presence of strong trap-assisted tunneling due to a high trap concentration in the dielectric layer. By assuming a simple Frenkel-Poole like conduction through the oxide layer

$$J = A F_{\mathrm{ox}} \exp\left(\frac{B\sqrt{F_{\mathrm{ox}}} - \mathrm{q}\Phi_{\mathrm{t}}}{\mathrm{k_B} T}\right) \qquad (2)$$

where F_{ox} is the electric field in the oxide and A and B were used as fitting parameters, the measurements could be reproduced (full lines). However, the values of A and B differ for positive and negative gate bias. That indicates that different conduction processes occur for accumulation and inversion. Note that in previous studies [5] tunneling through ZrO_2 layers fabricated by magnetron sputtering could be reproduced without considering trap-assisted tunneling.

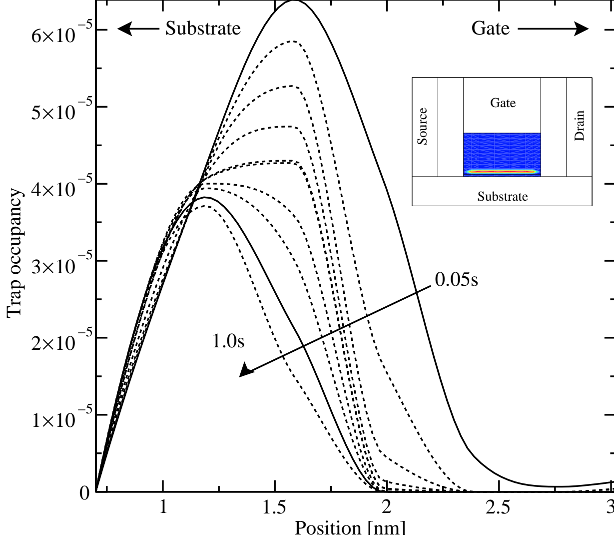

Figure 4. Decay of the trap occupancy in the gate dielectric after removing a gate bias of 2.5 V

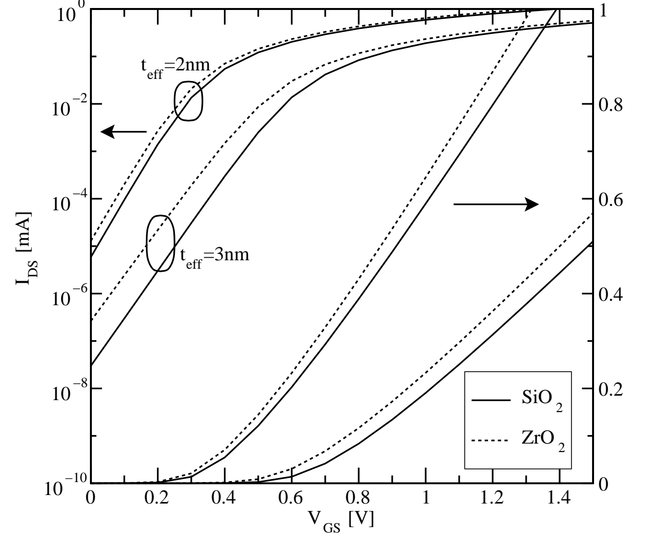

Figure 5. Transfer characteristics of the 'well-tempered' MOSFET with SiO_2 and ZrO_2 dielectrics at V_{DS}=1.2V.

4. Modeling of Transient Tunneling

To clarify the trap energy level and concentration, the step response of the MOS capacitors has been measured as shown in Fig. 3 for the 12.7 nm ZrO_2 layer annealed in reducing conditions (forming gas) and the 6.9 nm layer annealed under oxidizing conditions. The gate voltage is turned off after being fixed at a value of 2.5 V and the resulting gate current is measured over time. The transient gate current exceeds the static gate current by orders of magnitude and decays very slowly. This behavior can be explained assuming slow states in the dielectric layer [6].

To account for this transient trap-assisted tunneling we use a model that has been presented in [7] and was implemented in MINIMOS-NT. Based on the rate equation for the concentration of occupied traps at position z and time t in the dielectric layer

$$\frac{df_{\mathrm{T}}(z,t)}{dt} = (1-f_{\mathrm{T}}(z,t))\tau_{\mathrm{c}}^{-1}(z) - f_{\mathrm{T}}(z,t)\tau_{\mathrm{e}}^{-1}(z), \quad (3)$$

the trap occupancy follows an exponential decay

$$f_{\mathrm{T}}(z,t) = \frac{\tau_{\mathrm{m}}(z)}{\tau_{\mathrm{c}}(z)} + \left(f_{\mathrm{T}}(z,0) - \frac{\tau_{\mathrm{m}}(z)}{\tau_{\mathrm{c}}(z)}\right)\exp\left(-\frac{t}{\tau_{\mathrm{m}}(z)}\right).$$

In these equations $f_{\mathrm{T}}(z,t)$ is the trap occupancy function at position z and time t, $\tau_{\mathrm{m}}^{-1} = \tau_{\mathrm{c}}^{-1} + \tau_{\mathrm{e}}^{-1}$, and $\tau_{\mathrm{c}}(z)$ and $\tau_{\mathrm{e}}(z)$ are the time constants for capture and emission processes. They are calculated assuming inelastic phonon-assisted tunneling processes [8]. The free parameters of the model are the trap concentration, the trap energy level below the dielectric conduction band edge, the Huang-Rhys factor of the traps S, and the phonon energy $\hbar\omega$. Once the occupancy function is known, the transient tunnel current through one of the interfaces is

$$J(t) = q\int_0^{t_{\mathrm{ox}}} N_{\mathrm{t}}(z)\left(\tau_{\mathrm{c}}(z)^{-1} - f_{\mathrm{T}}(z,t)\tau_{\mathrm{m}}(z)^{-1}\right)\,\mathrm{d}z.$$

The trap charge of occupied traps is calculated as the product of the local trap concentration $N_{\mathrm{t}}(z)$, the trap occupancy $f_{\mathrm{T}}(z,t)$ and the trap charge state. The trap concentration was assumed to be constant in the dielectric layer. Only electron tunneling has been assumed, and the trap charge was self-consistently taken into account in the Poisson equation. Using this model, a trap energy level of 1.3 eV below the ZrO_2 conduction band edge, a trap concentration of $4.5\times10^{18}\,\mathrm{cm}^{-3}$ and an energy loss of 1.5 eV have been found. For the dielectric layer annealed under oxidizing conditions the trap concentration was reduced to 4e17 cm^{-3} to fit the measurements.

The model allows to study the location of occupied traps in the dielectric. Under inversion condition, traps near the substrate side of the dielectric layer are occupied while traps near the gate are empty. Fig. 4 shows that the trap occupancy has a Gaussian shape and shows a linear decay over time when the gate voltage is switched off.

5. Device Simulation

To predict the performance of devices based on ZrO_2 dielectrics a well-tempered MOSFET as described in [9] with an effective channel length of 50 nm has been simulated. Effective gate oxide thicknesses of 2 nm and 3 nm SiO_2 and respective ZrO_2 layers have been considered. Fig. 5 show the transfer characteristics for a drain-source voltage of V_{DS}=1.2 V on a linear and logarithmic scale for the different oxide thicknesses and dielectrics. It can be seen that the ZrO_2 layer leads to considerably reduced threshold voltages. This reduction in the threshold voltage can be explained by the fringing fields from the drain contact which reduce the drain-source barrier, an effect which is especially pronounced for thicker layers. Fig. 6 depicts the conduction band edge in the channel for different gate-

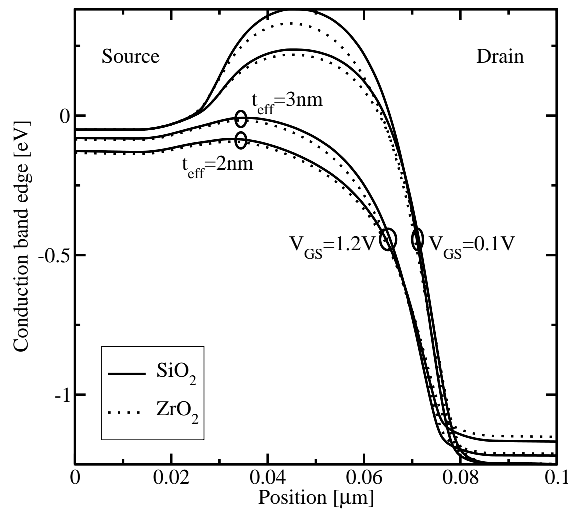

Figure 6. Well-tempered MOSFET conduction band edge along the channel for SiO_2 and ZrO_2 dielectrics

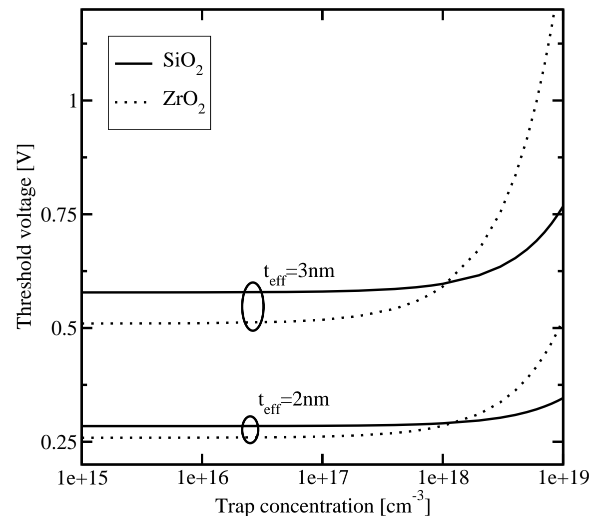

Figure 7. Influence of the dielectric trap concentration on the MOSFET threshold voltage

source voltages. It can be seen that the barrier is slightly lower for the ZrO_2 layer at V_{GS}=1.2 V, while there is a heavy barrier reduction for V_{GS}=0.1 V.

An additional topic of interest for high-κ dielectrics is the influence of trapped charges in the high-κ layer on the threshold voltage of the device. We used MINIMOS-NT to study this effect and defined the threshold voltage at a drain-source current of 10 µA. The trap concentration in the ZrO_2 layer was increased from $10^{15}\,\mathrm{cm}^{-3}$ to $10^{19}\,\mathrm{cm}^{-3}$, with full trap occupancy in the dielectric layer. It can be seen in Fig. 7 that the threshold voltage strongly increases with rising trap concentration. This effect is therefore contradictory to the increase of the threshold voltage due to fringing fields described above.

6. Conclusions

The tunneling current through ZrO_2 layers deposited by MOCVD is mainly determined by trap-assisted tunneling which can be explained by a Frenkel-Poole tunneling model. The trap energy level and concentration can be estimated by measuring the step response of the MOS capacitors. The performance of a 'well-tempered' MOSFET using ZrO_2 dielectrics was studied by means of device simulation. It was found that there exist two controversial effects influencing the threshold voltage of the device. On the one hand, the high-κ dielectric leads to a reduced threshold voltage especially for thicker layers. This effect is due to fringing fields from the drain contact. On the other hand, occupied traps in the dielectric layer increase the threshold voltage of the device. So, for low trap concentrations, the threshold voltage for the high-κ device is lower than for the SiO_2 counterpart, while it is higher for high trap concentrations. This effect must be taken into account when modeling advanced MOS devices.

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