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Feature Scale Simulation of Advanced Etching Processes

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INTRODUCTION AND MOTIVATION

Etching of trenches and the deposition of thin layers are fundamental for the production of memory cells, power MOSFETs, and backend stacks. For the purposes of feature scale topography simulation, there are three basic geometric operations: deposition of layers, etching of trenches, and CMP (chemical mechanical planarization). The deposition of layers was simulated in [1, 2]. CMP is a straightforward operation on the feature scale level. Hence in this paper we present simulations for etching processes including advanced effects like microtrenching.

SIMULATION APPROACH AND RESULTS

The simulations were performed using the topography simulator ELSA (enhanced level set applications) which is based on a level set algorithm for describing moving boundaries [1, 2, 3]. For simulating etching of materials with different properties with respect to the etchant, a multi region level set algorithm was developed. This extension enables the description of complicated geometries. Examples are masks on the wafer, etch stop layers, or selective etching. In these regions the incoming fluxes are translated to the etching speed according to the different material properties.

The ion angular distribution function (IADF) entering the simulation domain and the location of the ion sources are determined by the plasma and this information enters the feature scale simulation as physical boundary condition. The ions at the wafer surface are reflected in a specular manner in addition to a cosine law around the angle of the reflection.

The experiments performed during development of a RAM process were performed in a LAM 9600 reactor (cf. Figure 1). The etchant was chlorine and thus $Cl^{+}{}_{(g)} + S \rightarrow Cl_{(s)}$, $Si_{(s)} + 4Cl_{(s)} \rightarrow SiCl_{4(g)} + 4S$ (S denotes a surface site) was used as the dominating reaction path [4, 5]. The corresponding simulation is shown in Figure 2.

Figure 3 shows a situation where microtrenching occurs. In this case the reflections at the side walls affect the development of small trenches at the bottom, whose shape is resolved accurately in the simulation.

CONCLUSION

For different process conditions the etching of trenches into Silicon is simulated depending on the physical transport phenomena that occur on the reactor scale level, most notably the ion angular distribution function. Accurate agreement was found for a RAM process and backend stacks of a 100nm CMOS process.

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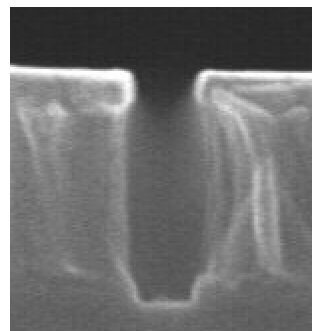

Figure 1

SEM image.

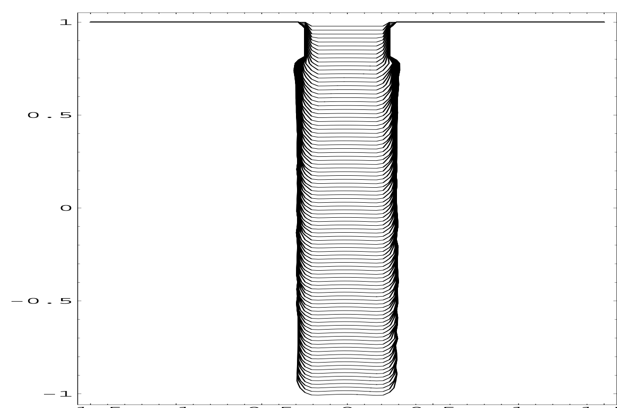

Figure 2

Simulation result.

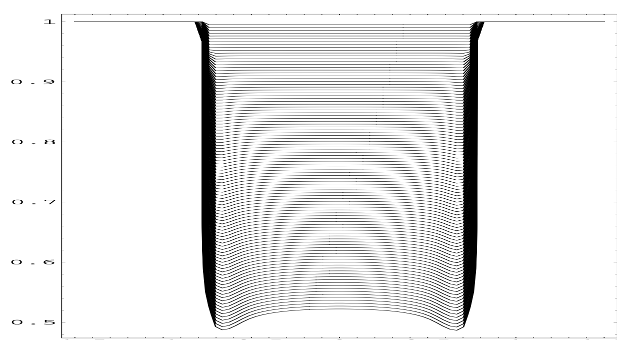

Figure 3

Microtrenching.