Analysis of High Speed Heterostructure Devices

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Abstract— **We present a review of industrial heterostructure devices based on SiGe/Si and III-V compound semiconductors analyzed by means of numerical simulation. The work includes a comparison of device simulators and current transport models to be used, and addresses critical modeling issues. Results from two-dimensional hydrodynamic analyses of Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs) with Minimos-NT are presented in good agreement with measured data. The examples are chosen to demonstrate technologically relevant issues which can be addressed by device simulation.**

I. Introduction

Communication and information systems are subject to rapid development, where semiconductor heterostructure devices, such as Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs), are among the fastest and most advanced high-frequency devices [1]. They meet well the requirements for low power consumption, medium-scale integration, low cost in large quantities, and high-speed operation capabilities in circuits in the very high frequency range (recently beyond 500 GHz [2]) and for data rates higher than 100 Gbit/s for long range communication.

SiGe HBTs progressively replace III-V devices for their typical applications, such as low noise amplifiers and frequency dividers up to 99 GHz[3], and are considered essential for 40 Gb/s optical communication systems. Transit frequencies, f_T, of 350 GHz [4], maximum oscillation frequencies, f_{max}, of 285 GHz, and ring oscillator delays of 4.2 ps [5] have been reported. Fig. 1 shows the rapid progress of peak-f_T of SiGe HBTs over the last couple of years. The devices are fully compatible with existing state-of-the-art 0.13 μm CMOS technology [5], [6]. Digital application-specific integrated circuits (ASICs) are combined with SiGe HBT circuits in the so-called SiGe BiCMOS technology and are in volume production.

GaAs HBTs are popular devices due to their use for power amplifiers in modern cellular phone handsets. Their major advantages are the very low off-state power consumption (a few μW) and the high current amplification for low battery-driven voltage of typically 3 V. Major contributions come from RF Microdevices [7], based on the long experience of TRW Inc. [8]. Further contributions come from United Monolithic Semiconductors (UMS) [9], [10] and WIN Semiconductor [11].

InP HBTs bear a number of advantages over the GaAs material system for many applications [12]. They are most interesting for oscillator applications because of the low phase noise properties. Due to a combination of high speed and high breakdown voltages they are suitable for high-speed digital applications up to at least 100 Gbit/s for long distance communication. The principle reasons for their application include the high current amplification at low current levels, which normally is addressed as low-power capability, and the ultimate speed available in emitter-coupled logic (ECL) circuits. Fig. 2 shows the record peak-f_T of InP HBTs over the last couple of years.

The most prominent HEMT on GaAs is currently the AlGaAs/InGaAs pseudomorphic HEMT (PHEMT), which combines outstanding breakdown voltages and high-speed performance. The focus has moved from research to industrial production of these devices. Major contributions come from Triquint, TRW, and UMS [13], [14], [15]. Although being challenged by SiGe HBTs, GaAs PHEMTs still deliver remarkable performance for low-noise applications in receiver circuits up to 100 GHz [16].

Narrow bandgap materials such as InGaAs lattice-matched to InP have pushed the cut-off frequencies beyond 400 GHz for sub-100 nm gate length HEMTs. InAlAs/InGaAs HEMTs have been the fastest three-terminal devices for the last decade, as can be seen in Fig. 3.

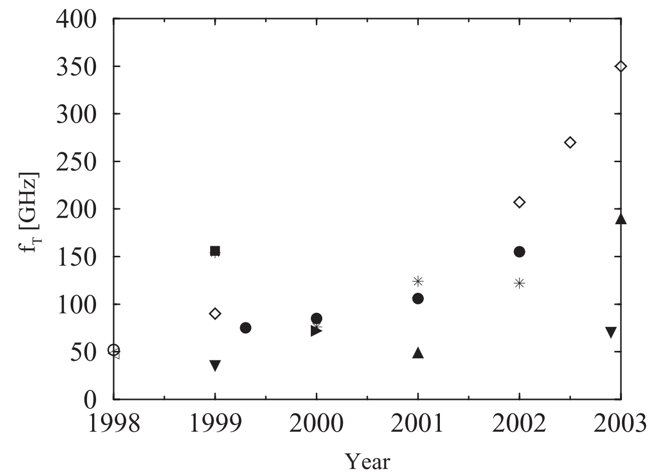

Fig. 1. Current gain cutoff frequency f_T of SiGe HBTs over time.

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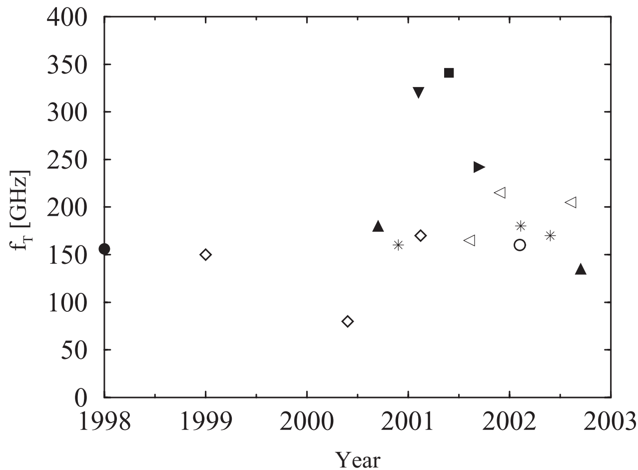

Fig. 2. Current gain cutoff frequency f_T of InP HBTs over time.

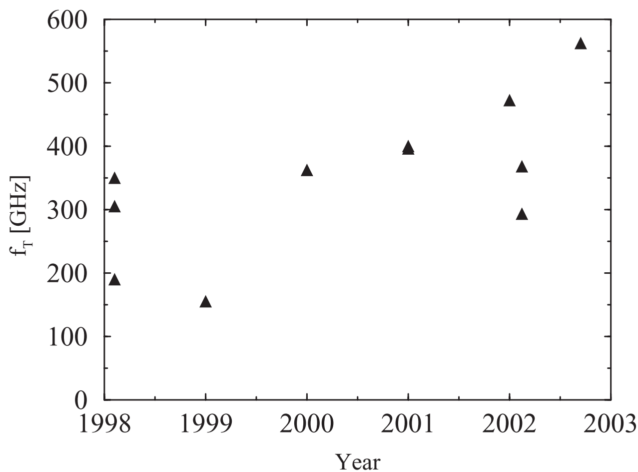

Fig. 3. Current gain cutoff frequency f_T of InAlAs/InGaAs/InP HEMTs over time.

To cope with explosive development costs and strong competition in the semiconductor industry, Technology Computer-Aided Design (TCAD) methodologies are extensively used in development and production. Several questions during device fabrication, such as performance optimization and process control, can be addressed by simulation. The choice of a given simulation tool or a combination of tools depends to a large extent on the complexity of the particular task, on the desired accuracy of the problem solution, and on the available human, computer, and time resources.

Optimization of geometry, doping, materials, and material composition profiles targets at high power, high breakdown voltage, high speed (high f_T, f_{max}), low leakage, low noise, and low power consumption. This is a challenging task that can be significantly supported by device simulation.

The paper gives a short review of state-of-the-art device simulators, including the three-dimensional device simulator Minimos-NT, discusses critical modeling issues regarding the simulation of advanced SiGe and III-V semiconductor devices, and concludes with particular simulation results of such devices obtained with the same simulation tool, model set, and set of model parameters. We demonstrate by examples from industrial vendors how a well-calibrated tool can address technologically important issues.

II. Critical Modeling Issues for Heterostructure Devices

There are several problems which are specific for the modeling and simulation of heterostructure devices.

A generic device simulator must not only be capable to account for various semiconductor materials but also for different complex geometrical structures and material sequences in multiple dimensions. The physical properties of SiGe and III-V compounds must be modeled for wide ranges of material compositions, temperatures, doping concentrations, etc. The model parameters have to be verified against several independent HEMT and HBT technologies to obtain a concise set used for all simulations. Reviewing simulation of HBTs and submicron HFETs with gate-lengths down to 100 nm used for millimeter-wave devices, solutions of energy transport equations are necessary to account for non-local effects, such as velocity overshoot.

Modeling of strained SiGe is not a trivial task, since special attention has to be focused on the stress-induced change of the bandgap as a function of germanium content [17]. This effect must be separated from doping-induced bandgap narrowing which in turn depends on the semiconductor material composition, the doping concentration, and the lattice temperature [18]. As the minority carrier mobility is of considerable importance for bipolar transistors a distinction between majority and minority electron mobilities is required [18].

Heterointerface modeling is a key issue for devices which include abrupt junctions. Thermionic emission and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces.

Another critical issue for recessed HFETs and for III-V HBTs is the description of the semiconductor/insulator interfaces, especially with respect to the treatment of the interfaces during the manufacturing process. Fermi-level pinning prevails for typical barrier materials such as AlGaAs or InAlAs and for ledge materials such as InGaP. Active surface states can influence significantly the current gain in bipolar devices [19].

All the important generation/recombination effects, such as Shockley-Read-Hall recombination, surface recombination, direct recombination, Auger recombination, band-to-band tunneling processes, and impact ionization must be taken into account. III-V semiconductors and SiGe are known to have a reduced heat conduc-

tivity in comparison with silicon [1]. Thus self-heating effects must be accounted for considering the substrate thermal conductivity [20].

Advanced device simulation allows a precise physics-based extraction of small-signal parameters [1]. Measured bias-dependent S-parameters serve as a valuable source of information when compared at different bias points to simulated S-parameters from a device simulator. This procedure reflects the full RF information contained in the S-parameters and allows process control beyond the comparison of DC quantities.

A physics-based large-signal extraction is critical due to the typical problems of compact large-signal models. These are: the accurate treatment of parasitic elements, e.g. inductances for multi-finger devices; the thermal problem, which is generically three-dimensional; and frequency dispersion due to fast traps in III-V semiconductors.

III. Heterostructure Device Simulators

The continuously increasing computational power of computer systems allows the use of TCAD tools on a very large scale. Several commercial device simulators (such as APSYS [21], ATLAS [22], BIPOLE3 [23], DESSIS [24], G-PISCES [25], and MEDICI [26]), company-developed simulators (like FIELDAY [27] and NEMO [28]), and university-developed simulators (such as DEVICE [29], FLOODS [30], GALENE [31], MINIMOS 6 [32], nextnano3 [33], PISCES [34], and PROSA [35]) have been successfully employed for device engineering applications. These simulators differ considerably in dimensionality (one, quasi-two, two, quasi-three, or three), in choice of carrier transport model (drift-diffusion, energy-transport, or Monte Carlo (MC) statistical solution of the Boltzmann transport equation), and in the capability of including electrothermal effects. The drift-diffusion transport model [36] is by now the most popular model used for device simulation. With down-scaling of the feature sizes, non-local effects become more pronounced and must be accounted for by applying an energy-transport model or a hydrodynamic transport model [37]. During the last two decades, Monte Carlo methods for solving the Boltzmann transport equation have been developed [38], [39] and applied for device simulation [40], [41], [42]. However, reduction of computational time is still an issue, and therefore MC device simulation is still not feasible for industrial application on daily basis. An approach to preserve accuracy at lower computational cost is to calibrate lower order transport parameters to MC simulation data.

Quantum mechanical effects gain increased importance with the scaling of the feature size. These effects are often neglected in device simulation or only accounted for by simple analytical models for quantum corrections [43], [44], since solving the Schrödinger or the Wigner equation [45] is extremely expensive in terms of computational resources.

Most device simulators focus on silicon devices, and the model parameters for SiGe are often simply inherited from the parameters for silicon. The database available for properties of III-V semiconductors has been limited for a long time due to the large number of materials and material compositions. Moreover, a thorough approach of modeling has been lacking. The quality of the physical models can be questioned, since modeling of the properties of AlGaAs, InGaAs, InAlAs is often restricted to slight modifications of the GaAs material properties. Physical parameters for InGaP and other phosphides are required for advanced device modeling, together with new material systems, such as the GaN or the GaSb systems, which have entered the III-V world with impressive device results. A severe problem is the limited feedback from statistically-based technological process development to device simulator development. Therefore published application examples will also be mentioned here in the course of the discussion.

Critical issues concerning simulation of heterostructures, such as interface modeling at heterojunctions, silicon/poly-silicon interfaces for SiGe devices and insulator surfaces for III-V devices are frequently not considered. The importance of high-energy and high-field effects, such as carrier energy relaxation, impact ionization, and self-heating, is sometimes underestimated.

The two-dimensional device simulator PISCES [34] developed at Stanford University incorporates modeling capabilities for Si, GaAs, and InP-based devices. One of its versions, PISCES-HB, includes harmonic balance for large-signal simulation. It has been applied to LDMOS devices [46] and to MESFETs [47]. Another version, G-PISCES from Gateway Modeling [25], has been extended by a full set of III-V models. Examples of MESFETs, HEMTs, and HBTs for several material systems, e.g. InAlAs/InGaAs, AlGaAs/InGaAs, AlGaAs/GaAs, and InGaP/GaAs, are demonstrated. However, in comparison with the original version of PISCES, this simulator lacks an energy-transport model which is necessary to model high-field effects. G-PISCES also demonstrated the simulation of AlGaN/GaN HEMTs [48].

The device simulator MEDICI from Synopsys [26], which is also based on PISCES, offers simulation capabilities for SiGe/Si HBTs and AlGaAs/InGaAs/GaAs HEMTs. It has been used for the simulation of AlGaAs/GaAs HBTs [49] and for the evaluation of properties of GaN HBTs [50]. Advantages of this simulator are hydrodynamic simulation capabilities and the rigorous approach to generation/recombination processes. In addition, it includes a module which considers anisotropic material properties in SiGe. In a recent version, an interface model including carrier tunneling is included in the III-V simulation module.

The two- and three-dimensional device simulator DESSIS from ISE [24] has demonstrated a rigorous approach to semiconductor physics including extensive trap modeling and a variety of mobility models. The capabilities to model Si and SiC are extended by a heterojunction framework to III-V materials [51]. Interface tunneling is included in a thermionic field emission model. The density-gradient method is used to model quantum effects in heterostructure devices [52].

At the quantum level a one-dimensional Schrödinger-Poisson solver, NEMO [28], based on non-equilibrium Green's functions is offered for sub-0.1 μm SiGe structures. POSES [25] from Gateway Modeling is another Schrödinger-Poisson solver proposed for process control by charge analysis in HEMTs. In the program SIMBA a link between a one-dimensional Schrödinger solver and a two-dimensional Poisson solver is demonstrated. SIMBA also provides drift-diffusion transport simulation of GaN HEMTs [53]. Recently the three-dimensional version of SIMBA has been used for thermal optimization of GaN HEMT layouts [54].

Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated by several simulators, including BIPOLE3 from BIPSIM, [23] which features good models for poly-silicon. A similar approach which couples a full hydrodynamic transport model with a Schrödinger solver has been developed at the University of Leeds [55], [56]. This with regard to computation time effective approach has been verified against MC simulations for devices with gate-lengths down to 50 nm [55]. Fast Blaze [22] from Silvaco is a commercial tool based on the code from Leeds. Simulations of S-parameters of AlGaAs/GaAs and pseudomorphic AlGaAs/InGaAs/GaAs HEMTs have been presented.

A software interface between the device model and the compact Root large-signal model within the Microwave Design System (MDS and ADS) has been offered by Agilent. Fast Blaze can be combined with the Advanced Design System (ADS) and has an interface with the microwave circuit simulator. An extraction with subsequent multitone excitation calculations has been presented in [57].

The two- and three-dimensional simulator ATLAS [22] from Silvaco has also claimed the simulation of AlGaAs/GaAs and AlGaAs/InGaAs/GaAs PHEMTs. Simulations of SiGe HBTs have also been announced, based on the simulator PROSA, developed at the University of Ilmenau [35]. However, the latter lacks heterointerface modeling. Several good optimization results for SiGe HBTs have been achieved with another university-developed simulator, SCORPIO [58].

We tried to address most of the critical modeling issues for heterostructure devices in the three-dimensional device simulator Minimos-NT [59], which we used for preparing the following examples.

IV. Selected Results of Industrially Relevant Devices

It is well known that GaAs-HBTs with an InGaP ledge have an improved reliability [60]. Power amplifiers with InGaP/GaAs HBTs are part of many cellular phones today. Two-dimensional device simulation allows the analysis of experimental data in cases which cannot be explained by simple analytical assumptions. This proved to be especially useful for explaining and avoiding device degradation which occurs as a result of electrothermal stress aging. The impact of the ledge thickness and the negative surface charges existing at the ledge/nitride interface, was studied for a one-finger $3{\times}30\ \mu\text{m}^2$ InGaP/GaAs HBT with respect to reliability [61]. We found a surface charge density of $\rho_{\text{surf}} = 10^{12}\ \text{cm}^{-2}$ appropriate to get good agreement with the measured Gummel plots at $V_{\text{CB}} = 0$ V. Based on these investigations it is possible to explain the base current degradation (see Fig. 4) of a strongly stressed device by a decrease in the effective negative surface charge density along the interface from $10^{12}\ \text{cm}^{-2}$ to $4{\times}10^{11}\ \text{cm}^{-2}$ due to compensation mechanisms [62]. Fig. 5 shows simulation result for the electron current density at $V_{\text{BE}} = 1.2$ V.

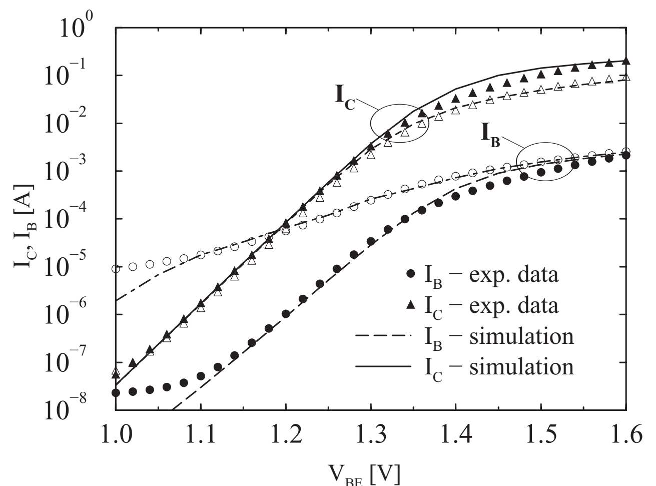

Fig. 4. Comparison of measurements (symbols) and simulations (lines) before (filled) and after (open) HBT aging

Once the possible reason for device degradation is known, it is natural to search for solutions. Some ways to avoid degradation were analyzed, assuming the worst case when the negative surface charges at the ledge/nitride interface of a device with 40 nm ledge thickness are completely compensated due to stress. A possible solution is to avoid the electron leakage path in the ledge by means of electrically isolated base contacts, e.g. by introducing a nitride spacer between the ledge and the base metals.

The simulation analysis shows that the depth of such a spacer is of importance. On the one hand, there is

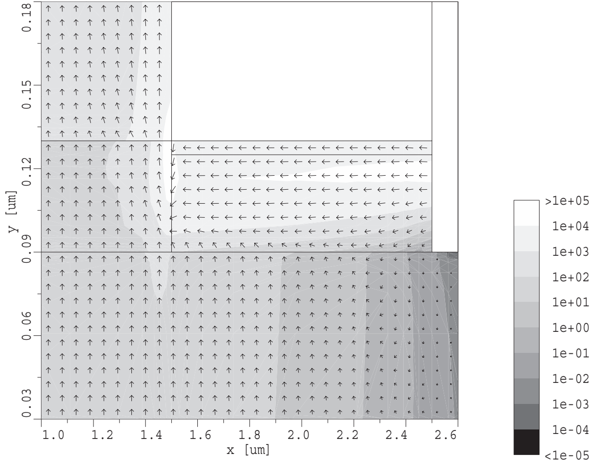

Fig. 5. Electron current density [A/cm^2] at $V_{BE} = 1.2$ V: Simulation with a surface charge density of $4{\times}10^{11}$ cm^{-2}.

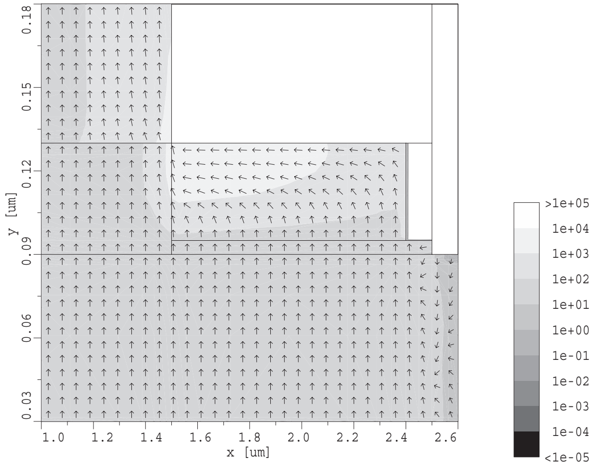

Fig. 6. Simulated electron current density [A/cm^2] at V_{BE} = 1.2 V with a spacer between ledge and base contact.

the constraint not to exceed the ledge thickness in order to avoid surface recombination in the base. On the other hand, the spacer has to have a sufficient depth to prevent the electron current. Fig. 6 shows the electron current density at $V_{BE} = V_{CE} = 1.2$ V in a device with a distance of 10 nm between the spacer and the base layer. As can be seen in Fig. 6 a current path still exists under the spacer, if the surface charges are compensated. Unfortunately it is technologically challenging to control the exact spacer depth which has to be about 95% of the ledge thickness in order to solve the reliability problem.

Fig. 7 shows the simulated forward Gummel plots for 40 nm ledge devices with 35 nm deep spacers on the base contact side or on the emitter side of the ledge, respectively. In addition, simulation results for a device with 20 nm ledge thickness are included for comparison in Fig. 7. Measured data for a non-stressed device

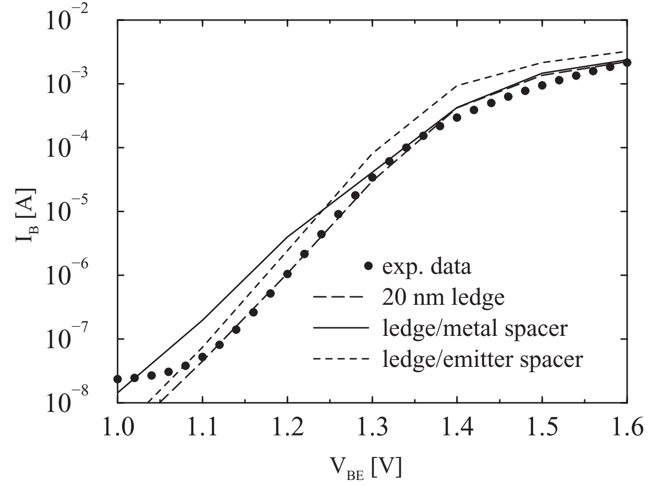

Fig. 7. Base current I_B in a stressed device using spacer between the ledge and the base contact, between the ledge and the emitter, and device with a thinner ledge. Comparison with measured data for non-stressed device.

(symbols) is included as a reference. Note that the device with the 20 nm ledge not only has better device characteristics, but is also easier to manufacture.

For HFET performance the very critical issues are process control and inverse modeling of geometrical structures. Various examples for high-power AlGaAs/InGaAs/GaAs and high-speed InAlAs/InGaAs/InP HEMTs are demonstrated in [63].

Two factors contribute to the gate currents in pseudomorphic GaAs HEMTs: thermionic field emission effects and impact ionization are analyzed in detail in [64], [65]. For high-speed InAlAs/InGaAs HEMTs, the precise evaluation of low voltage or low power capabilities is useful for development of high-speed optical data transmission beyond 40 Gbit/s. The comparison of several lattice matched and metamorphic technologies gave consistent simulation parameters also for this material system [66]. Fig. 8 shows simulation and measurements for two different substrate temperatures for a composite channel $In_{0.52}Al_{0.48}As$/ $In_{0.66}Ga_{0.34}As$/$In_{0.53}Ga_{0.47}As$/InP HEMT for l_g = 150 nm. High field effects such as impact ionization are considered. This allows the analysis of both, optimized speed and limited gate current, when scaling δ-doping and gate-to-channel separation for the requirements of 80 Gbit/s operation.

The methodology for characterization and optimization of SiGe HBTs involves process calibration, device calibration employing two-dimensional device simulation, and automated Technology Computer Aided Design (TCAD) optimization. The investigated 12×0.4 μm^2 SiGe HBT structure is obtained by process simulation with DIOS [24], which reflects real device fabrication as accurately as possible.

All important physical effects, such as surface recom-

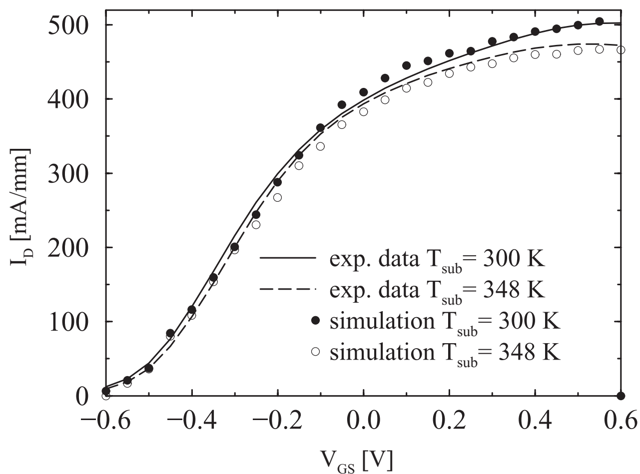

Fig. 8. Simulated and measured transfer characteristics of a composite channel InAlAs/InGaAs/InP HEMT with $l_g = 150$ nm as a function of temperature at $V_{DS} = 0.75$ V.

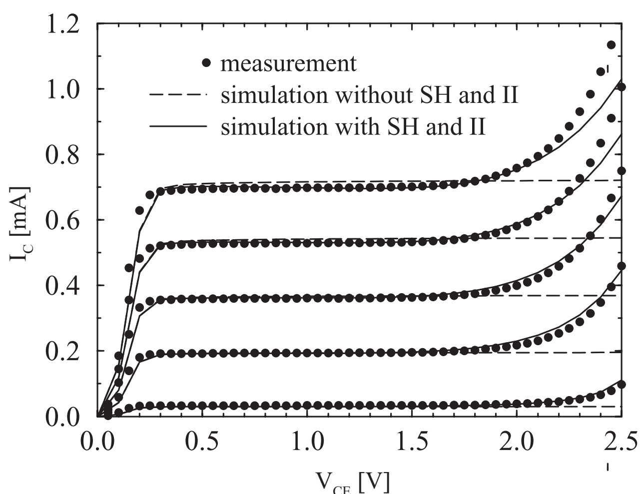

Fig. 9. SiGe HBT output characteristics: Simulation with and without self-heating (SH) and impact ionization (II) compared to measurement data. I_B is stepped by 0.4 μA from 0.1 μA to 1.7 μA.

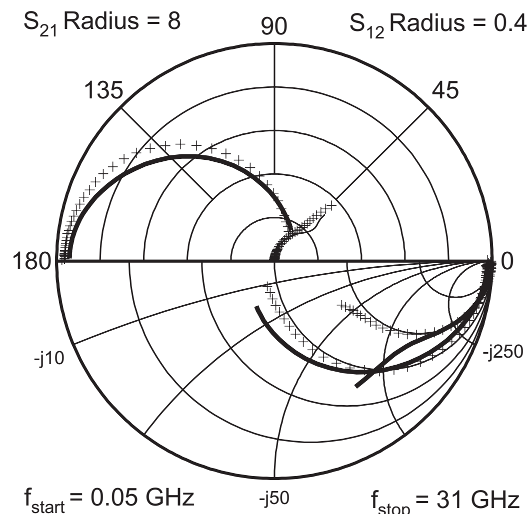

Fig. 10. Simulated (–) and measured (+) S-parameters in a combined Smith-polar chart from 50 MHz to 31 GHz at $V_{CE} = 1$ V and $J_C = 76$ kA/cm^2.

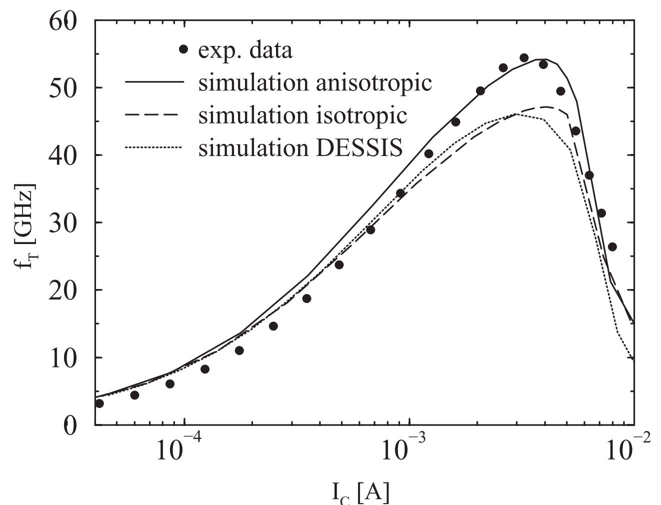

Fig. 11. Cut-off frequency f_T versus collector current I_C at $V_{CE} = 1$ V.

bination, generation due to impact ionization, and self-heating, are properly modeled and accounted for in the simulation in order to get good agreement with measured forward and output characteristics (Fig. 9) using a concise set of models and parameters. Simulation without including self-heating effects cannot reproduce the experimental data, especially at high power levels.

Since advanced SiGe techniques exhibit competitive performance of high frequency devices in markets that were prior the domain of other materials, small-signal analysis by means of simulation of these devices becomes more important. Fig. 10 shows a comparison between measured and simulated S-parameters in the frequency range between 50 MHz and 31 GHz at V_{CE} =1 V and current density $J_C = 76\,\text{kA/cm}^2$. We calculated the matched gain g_m and the short-circuit current gain h_{21} in order to extract f_T and f_{max}. Fig. 11 compares f_T vs. I_C from simulation and measurement. It shows also the effect of an anisotropic electron mobility. In addition, results obtained by a commercial device simulator (DESSIS [24]) using default models and parameters are included for comparison.

Using the model for the InP/InGaAs/InGaAsP/InP HBT given in [1], the following study is performed. In this device, the $In_{0.53}Ga_{0.47}As$ base layer is replaced by $GaAs_{0.49}Sb_{0.51}$ which is also lattice-matched to the InP substrate, and the InGaAsP launcher is removed. Fig. 12 compares the simulated forward Gummel plots of the conventional InP/InGaAs/InGaAsP/InP DHBT (Dev. 1) and the novel InP/GaAsSb/InP

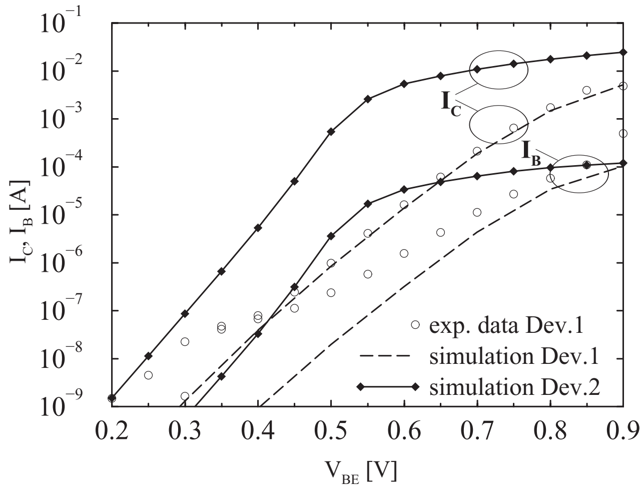

Fig. 12. Forward Gummel plot of 1×8 μm^2 InP/GaAsSb/InP DHBT in comparison to a conventional InP/InGaAs/InGaAsP/InP design.

DHBT (Dev. 2). Measured data for the conventional device are included as a reference.

V. Conclusion

A brief overview of the state-of-the-art of simulation tools for heterostructure RF-devices has been given. We have presented experiments and simulations of GaAs HBTs, SiGe HBTs, InP HBTs, and InP HEMTs. Good agreement was achieved both with experimental DC-results and with high-frequency data. With an increasing number of stable and reliable heterostructure technologies available, a meaningful comparison between simulation results and statistically analyzed data is possible and delivers on the one hand side model verification, and on the other hand side valuable process information.

Acknowledgment

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