CAPACITANCES IN THE BACKEND OF A **100***nm CMOS PROCESS AND THEIR PREDICTIVE SIMULATION*

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ABSTRACT

One of the challenging issues for semiconductor circuit design is how to overcome RC delays in the interconnect layers. To reduce the overall dielectric constant, it is important to develop a low-k barrier/etch stop film that can prevent the metal lines, usually made of aluminum, from interacting with other materials in multi-level interconnect schemes. An additional requirement for a barrier/etch stop film is high etch selectivity with respect to the ILD (inter-layer dielectric). Silicon nitride has been generally accepted as a first generation barrier. However, its k-value is high and when used in conjunction with a lower k dielectric, the overall k-value of the stack is significantly impacted. Here voids may serve a beneficial purpose, where they can lower the overall capacitance.

In this paper the simulation of backend and interconnect capacitance is considered. The backend stack is built up using topography simulation of deposition, etching, and CMP (chemical mechanical planarization) processes in different metal lines. We present results for a 100nm CMOS process. We show that the influence of void formation between interconnect lines strongly impacts the whole interconnect stack performance. Our tool for the topography simulations is called ELSA (enhanced level set applications) whose outputs are used by the capacitance extraction tool called RAPHAEL. The results of RAPHAEL are made available to the circuit designer in turn and are used in SPICE.

INTRODUCTION

Interconnects are becoming more important with shrinking technologies. The capacitance and resistance of interconnect lines are the important factors for calculating the timing delays due to metal lines, which contribute more and more to the overall delays.

For proper modeling the capacitances one has to know the metal profile, e.g., bottom and top CD (critical dimensions) and metal slope, the profile of the deposited layer with and without CMP, and the profile of the void, if any is formed. Generally these three profiles depend heavily on deposition process conditions, on metal thickness and line-to-line spacing, and less strongly on metal width.

Most resistance and capacitance extraction (RCX) tools assume rectangular metal profiles, either planar or conformal dielectrics, and have very simplistic void models. Even if the metal slope is modeled, it is mostly assumed constant and independent of space. While these ideal assumptions may be sufficient for older technologies, they are insufficient for today's technologies like the example from a 100nm CMOS process, where interconnects have a large number of special features which are nowhere close to ideal. Voids in ILD materials may serve a beneficial purpose. They lower the overall capacitance of a given metal layer and thus this approach is economically advantageous compared to using low-k materials. The impact of the voids on metal capacitance, especially for small features, is tremendous.

We present the results from a rigorous simulation approach. In order to provide predictive simulations of the overall capacitance, the shapes and positions of the voids must be simulated accurately. Here topography simulations serve as the input to the following extraction of the capacitance. The extracted capacitance for the specific technology at hand is then made accessible to the circuit designer.

FEATURE SCALE SIMULATION

In this section we present a brief description about the feature scale simulation which is implemented in the simulator ELSA [1]. Starting from a plain substrate topography simulation can be divided into three main tasks: etching trenches, depositing thin films, and CMP. These three tasks are carried out in order to build up the geometry of backend stacks. An example of the stacks to be considered in the following is shown in **Fig. 1**.

In principal, feature scale simulations consist of three steps. The first one is the simulation of the transport of particles in the boundary layer above the wafer by radiosity. The second one is determining the chemical reactions taking place at the wafer surface through the fluxes of particles found in the first step. The last step changes the surface according to the previous steps. This tracking is performed using the level set method [2].

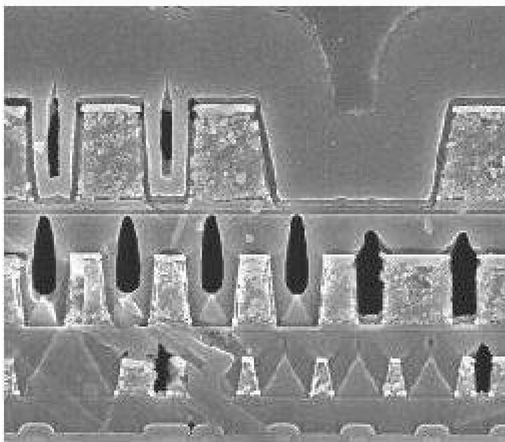

Figure 1: SEM image of a whole backend stack comprised of three Al metals and a Ti-nitride local interconnect.

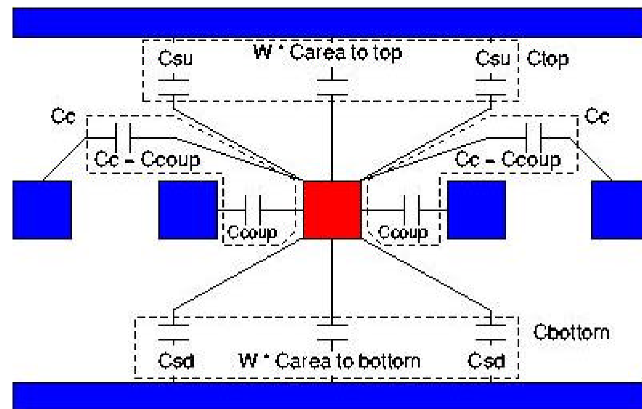

Figure 2: Two-dimensional schematics of a signal line (middle) surrounded by grounded lines and planes.

BACKEND SIMULATION

The coordinates generated by the topography simulator are then fed into a field solver, in our case RAPHAEL [3], which builds the structure, calculates electric fields and charge densities, and solves for various capacitances.

ELSA generally reports a large number of coordinates for describing ILD and void coordinates depending on the resolution required. Since this number of surface elements determines the number of RAPHAEL grid points, a significant reduction is necessary. Otherwise simulation times would be orders of magnitude larger than those for equivalent simplified structures. Hence we use a surface coarsening algorithm for reworking the output and reducing the number of points supplied to the field solver [4,5]. For this application simulation time is an important factor, since thousands of simulations are necessary for characterizing a technology.

CAPACITANCE TYPES

In order to model capacitances, we assume that a signal line is at high voltage and surrounded by two lines on the left, two lines on the right, a plane underneath, and a plane above. The surrounding lines and planes are assumed to be at ground voltage. For example, an M2 signal line could be surrounded by M2 grounded lines above the M1 plane and underneath the M3 plane. This skeleton is shown in **Fig. 2**.

There is a coupling capacitance to an adjacent line (C_{coup}), a coupling capacitance to a next to adjacent line (which usually is very small), a capacitance to the top plate (C_{top}), and a capacitance to the bottom plate (C_{bot}). The top capacitance is further split into a top area capacitance (C_{areat}) and a top side wall capacitance (C_{su}). Similarly the bottom capacitance is split into a bottom area capacitance (C_{areab}) and a bottom side wall capacitance (C_{sd}). The bottom (top) capacitance equals width W times bottom (top) area capacitance plus twice bottom (top) side wall capacitance.

CAPACITANCE MODELS

Capacitance simulations are performed as a function of three variables: First, they depend on metal combination, e.g., M4 above M2, or M3 above M1 and underneath M5. For a six layer technology the combinations can be above a hundred. Second, they depend on line-to-line spacing. Simulations start from the minimum allowed spacing (e.g., 0.14µm) and end in the range of a few microns (e.g., 6µm). Generally initial spacing increments are fine to capture any strong dependence of capacitance on spacing, and final increments are coarse to capture capacitance saturation. Third, capacitance simulations depend on line width. Simulations start from the minimum allowed width to approximately 60 times the minimum width. Since the dependence on the width is well behaved, only a few intermediate widths are usually needed. Once the set of metal combinations, spaces, and widths is finalized, the field solver simulations are started. In each case technology coordinates are read from the topography simulator and a set of capacitances is calculated and stored in a database. After all simulations are performed, one has accumulated a large range of capacitance parameters for different combinations of metals, spaces, and widths. All capacitances are reported per unit length, e.g., fF/µm.

EXAMPLES AND SIMULATION RESULTS

A SEM image of a typical backend stack is shown in **Fig. 1**. The films deposited are nitride and silicon dioxide films [6,7,8] and the interconnect lines are made of aluminum. The backend stacks considered are part of a 100nm CMOS process.

We applied ELSA to the following challenging example. Here we have M3 lines, i.e., top metal in this case, above the M2 plane. M3 lines are at 0.50µm width, and at a line-to-line spacing which varies between 0.45µm and 1.9µm. The upper part of **Fig. 3** shows the RAPHAEL structure constructed from ELSA coordinates at minimum spacing. Notice that at minimum spacing the metal lines are vertical and voids are maximum in size.

Next we build the structure at 1.5µm spacing. The middle part of **Fig. 3** shows the corresponding RAPHAEL structure again built from ELSA simulation results. Notice that in this case, however, metal lines have a slope, which duplicates the real process geometry. Voids are quite small in this case. Finally we build the structure at 1.9µm spacing. The lower part of **Fig. 3** shows the resulting RAPHAEL structure. Metals have slopes here as well, but voids do not longer exist.

The middle line capacitance was simulated for the above three structures and compared to CBCM (charge based capacitance measurement). The results are shown in **Fig. 4**. We observe very good agreement with an error of less than 5%.

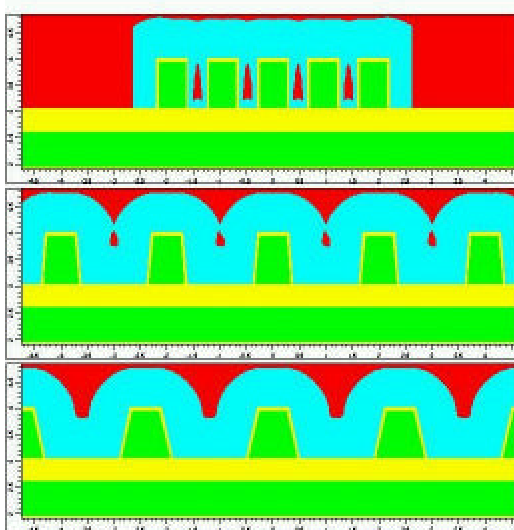

Figure 3: M3 lines (0.5mm top width) above M2 plane at 0.45mm, 1.5mm, and 1.9mm line-to-line spacings for the upper, middle, and lower part, respectively.

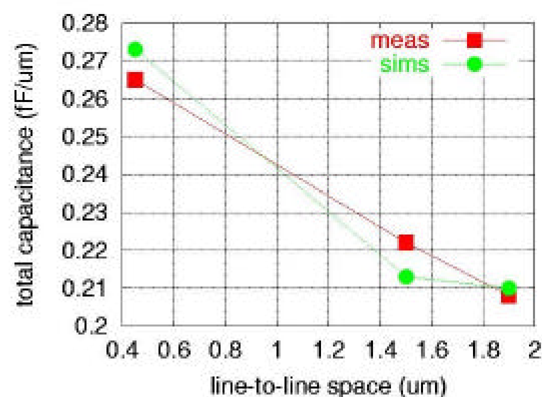

Figure 4: Comparing the M3 middle line capacitances as a function of line-to-line spacing between simulation and measurement.

CONCLUSION

The topography simulator ELSA and the RCX tool RAPHAEL, together with a few auxiliary tools, were combined to provide simulations of capacitances, and thus timings, in backend stacks. This simulation flow starts ab initio with silicon surfaces and takes into account etching, deposition, and CMP steps. From these the complex structures of interconnect lines are built resulting in many combinations depending on metal combination, line-to-line spacing, and line width. The interconnect structures serve as input to the field solver whose capacitance simulations are stored in a database. The circuit designer accesses the results of this simulation flow and uses them in SPICE.

The shape and position of voids in nitride films occurring in backend manufacturing process were simulated accurately. Void formation has a significant influence on the capacitances and hence a rigorous simulation approach like the one presented is indispensable for today's technologies. Furthermore using voids in a controlled and reproducible manner can be an economically advantageous substitute for low-k materials.

The simulations show very good agreement with CBCMs (charge based capacitance measurements). These simulations were used during the development of a 100nm CMOS process and proved to be of great help for circuit design.

REFERENCES

1. Sheikholeslami A., Heitzinger C., Puchner H., Badrieh F., and Selberherr S., "Simulation of Void Formation in Interconnect Lines". In Proc. of SPIE –The International Society for Optical Engineering, VLSI Circuits and Systems, Gran Canaria, Spain, May 19-21, 2003, p. 445-452.
2. Sethian J., "Level Set Methods and Fast Marching Methods". Cambridge University Press, Cambridge, 1999.
3. Avant! Corporation, TCAD Business Unit, Fremont, "Raphael, Interconnect Analysis Program, Version 2000.2, Reference Manual". CA, USA, July 2000.
4. Heitzinger C., Sheikholeslami A., Puchner H., and Selberherr S., "Predictive Simulation of Void Formation During the Deposition of Silicon Nitride and Silicon Dioxide Films". In Proc. of the 203rd Meeting of the Electrical Society, Paris, France, May 26- June 2, 2003, p. 356-365.
5. Heitzinger C., Fugger J., Haeberlen O., and Selberherr S., "Simulation and Inverse Modelling of TEOS Deposition Processes Using a Fast Level Set Method". In Proc. of Simulation of Semiconductor Processes and Devices, Kobe, Japan, September, 2002, p. 191-194.
6. Smith D., Wacker B., Ready S., Chen C., and Alimonda A., "Mechanism of SiN_xH_y Deposition from NH_3-SiH_4 Plasma". J. Appl. Phys., 87(3):1060-1069, Feb. 2000.
7. Schumicki G. and Seegebrecht P., "Prozesstechnologie". Springer, 1991.
8. Raupp G., Shemansky F., and Cale T., "Kinetics and Mechanism of Silicon Dioxide Deposition Through Thermal Pyrolysis of Tetraethoxysilane". J. Vac. Sci. Technol. B, 10(6):2422-2430, Nov. 1992.