Silicon Carbide Accumulation-Mode Laterally Diffused MOSFET

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Abstract

We present a new accumulation-mode structure for silicon carbide laterally diffused MOSFET. Key parameters that alter the device performance have been optimized using the device simulator MINIMOS-NT. The relationship between blocking and driving capability of the structure has been analyzed. Excellent I-V characteristics with significant improvement on the reduction of the gate bias voltage has been achieved. A blocking voltage of $1460\,\mathrm{V}$ *with a small leakage current, a considerably lower specific on resistance of* $93\,\mathrm{m}\Omega\cdot\mathrm{cm}^2$ *and a fairly large advantage on electrical performance and device reliability were achieved.*

1. Introduction

Silicon carbide (SiC) based devices are expected to offer superior performance compared to silicon devices due to their excellent electrical and thermal properties [1]. SiC is the only semiconductor material besides Si on which a thermal oxide can be grown, enabling MOS devices such as Double Diffused MOSFETs (DMOS) [2], Lateral RESURF MOSFET [3], Insulated Gate Bipolar Transistors (IGBT) [4], and MOS Gated Bipolar Transistors (MGT) [5]. Due to the lack of material development and design, most SiC MOSFETs suffer from surface problems such as step-bunching and non-uniform doping density [6]. This leads to poor inversion layer electron mobility and oxide reliability, which degrades the on-state performance and breakdown voltage. To minimize these problems accumulation-mode MOSFETs (ACCUFET) have been demonstrated recently for vertical DMOS transistors [7]. In this work we propose a new design of an accumulation-mode LDMOSFET (Laterally Diffused MOSFET). Key parameters that alter the overall device performance have been optimized using the general-purpose device simulator MINIMOS-NT [8]. The relationship between blocking and driving capability of the structure has been analyzed. Excellent I-V characteristics were obtained with good current saturation and gate control. The work also demonstrates a simulation based comparison of the proposed structure with the standard inversion-mode LDMOSFET.

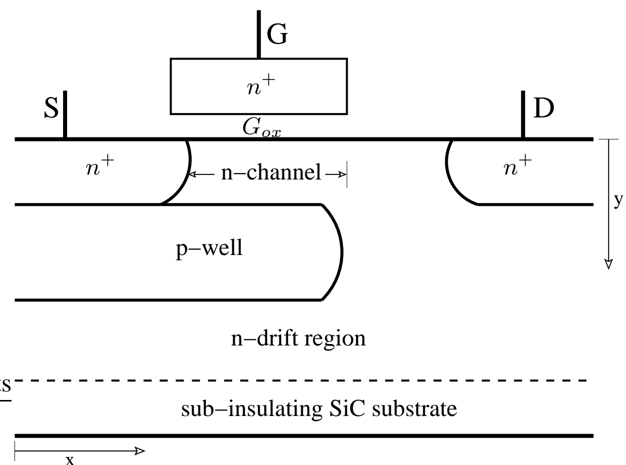

Figure 1. Schematics of the proposed SiC accumulation-mode LDMOSFET.

2. Device Structure and Operation

A schematic cross section of the proposed SiC accumulation-mode LDMOSFET is shown in Fig. 1. The principal difference between this structure and the conventional inversion-layer structure is the presence of a thin n-channel region (accumulation-layer) below the gate oxide using a buried p-well region formed by the ion-implantation. The thickness, length, and n- doping of this accumulation-layer is carefully chosen so that it is completely depleted by the built-in potential of the p/n junction. This causes a potential barrier between the n+ source and the n-drift regions, resulting in a normally-off device with the entire drain voltage supported by the p/n-drift region. Thus it can support high forward blocking voltages at zero gate bias with low leakage currents. When a positive gate bias is applied, an accumulation channel of electrons at the SiO_2-SiC interface is created and hence, a low resistance path for the electron current flow from the source to the drain can be achieved. This structure utilizes the buried p-well region as a shield to the influence of a high SiC bulk electric filed on the gate oxide. The structure also offers the possibility of moving the channel away from the oxide interface, thereby removing the effect of interface quality on the channel mobility.

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3. Device Analysis and Optimization

The choice of appropriate physical models is fundamental for any comparative study that involves numerical simulation. Among the SiC polytypes commercially available, for this work 6H-SiC is preferred owing to its higher inversion layer electron mobility and breakdown field strength [9] . We have utilized published material data from [10]. A model that takes into account the mobility degradation due to surface scattering has been incorporated with [11] and implemented in our simulator MINIMOS-NT:

$$\mu_{n,p}^{\mathrm{low}} = \mu_{n,p}^{\mathrm{min}} + \frac{\mu_{n,p}^{\mathrm{T_0}} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\mu}} - \mu_{n,p}^{\mathrm{min}} \cdot (1 - M(y))}{1 + M(y) \cdot \left(\frac{N_{\mathrm{D}}+N_{\mathrm{A}}}{N_{\mathrm{n,p}}^{\mu}}\right)^{\gamma_{\mathrm{n,p}}^{\mu}}} \tag{1}$$

$$M(y) = \frac{2 \cdot \exp\left(-\left(\frac{y}{y^{\mathrm{ref}}}\right)^2\right)}{1 + \exp\left(-2 \cdot \left(\frac{y}{y^{\mathrm{ref}}}\right)^2\right)} \tag{2}$$

where the function $M(y)$ depends on the surface distance y, and the parameter y^{ref} describes a critical length ($50\,\mathrm{nm}$ is taken for this analysis) .

At a high electric field the drift velocity $v_{n,p}$ of the carriers saturates due to increasing optical phonon scattering and finally reaches the saturation velocity $v_{n,p}^{\mathrm{sat}}$, leading to the field dependent mobility as described by [12]

$$\mu_{n,p} = \frac{\mu_{n,p}^{\mathrm{low}}}{\left[1 + \left(\frac{\mu_{n,p}^{\mathrm{low}} \cdot E_{\parallel}}{v_{n,p}^{\mathrm{sat}}}\right)^{\beta_{n,p}^{\mathrm{sat}}}\right]^{\frac{1}{\beta_{n,p}^{\mathrm{sat}}}}}. \tag{3}$$

We take the component of the electric field parallel to the electron motion as driving force. The temperature dependence of $v_{n,p}^{\mathrm{sat}}$ has been modeled by

$$v_{n,p}^{\mathrm{sat}} = v_0^{\mathrm{sat}} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\mathrm{sat}}} \tag{4}$$

and

$$\beta_{n,p}^{\mathrm{sat}} = \beta_0^{\mathrm{sat}} \cdot \left(\frac{T}{T_0}\right)^{\sigma_{n,p}^{sat}}. \tag{5}$$

Other MINIMOS-NT models that account for incomplete ionization, Auger recombination, Shockley-Read-Hall recombination, and impact ionization have been employed. The latter has been modeled according to [13], where the dependence of the impact ionization rate on the electric field and temperature is given by

$$\alpha_{n,p} = a_{n,p}\gamma_a \exp\left(-\frac{b_{n,p}\gamma_a}{E_{\parallel}}\right) \tag{6}$$

$$\gamma_a = \frac{\tanh\left(h\omega_{\mathrm{op}}/2kT_0\right)}{\tanh\left(h\omega_{\mathrm{op}}/2kT\right)} \tag{7}$$

α_n and α_p are the impact ionization coefficients for electrons and holes, respectively. The factor γ_a as a function of the optical phonon energy $h\omega_{\mathrm{op}}$ expresses the temperature dependence of the phonon gas against which the carriers are accelerated.

Table 1. MINIMOS-NT parameters used for simulating 6H-SiC.

species	$\mu_{n,p}^{T_0}$ [cm²/Vs]	$\mu_{n,p}^{\mathrm{min}}$ [cm²/Vs]	$N_{n,p}^{\mu}$ [cm^{-3}]	$\gamma_{n,p}^{\mu}$
n	415	0.0	1.1×10^{18}	0.59
p	99	6.8	2.1×10^{19}	0.31
$\delta_{n,p}^{\mu}$	$v_0^{T_0}$ [cm/s]	β_0^{sat}	$\delta_{n,p}^{\mathrm{sat}}$	$\sigma_{n,p}^{\mathrm{sat}}$
-1.8	1.9×10^{7}	1.7	-1	1.25
a_n [cm $^{-1}$]	b_n [V/cm]	a_p [cm $^{-1}$]	b_p [V/cm]	$h\omega_{\mathrm{op}}$ [meV]
1.66×10^{6}	1.27×10^{7}	5.18×10^{6}	1.4×10^{7}	106

For the device optimization six parameters that alter the device performance have been investigated: The doping concentration of the n-drift region; the depth and the concentration of the implanted p-well; the doping concentration and the thickness of the n-channel (accumulation-layer); and the gate oxide overlap length. The p-well region has a Gaussian profile buried between 0.3 and 1.0 μm, which has to be optimized because it determines the thickness of the accumulation-layer region which in turn affects the gate oxide field, breakdown voltage, and on-resistance.

For the desired breakdown voltage of $1500\,\mathrm{V}$, the proposed structure is optimized to have a $33\,\mu\mathrm{m}$ cell pitch, a $10\,\mu\mathrm{m}$ thick n-drift region doped at $5.0\times10^{15}\,\mathrm{cm}^{-3}$ and an n+ polysilicon gate electrode with a $50\,\mathrm{nm}$ thick gate oxide. When the buried p-well depth is larger, the built in potential is unable to fully deplete the n-channel which causes high leakage currents. Therefore, its depth and implanted peak concentration of $0.5\,\mu\mathrm{m}$ (between $0.3 - 0.8\,\mu\mathrm{m}$) and $1.0\times10^{18}\,\mathrm{cm}^{-3}$ respectively was found to give the optimum accumulation layer thickness at which the criterion for the device optimization (figure of merit, FOM) [14] can be satisfied.

$$\left.\frac{V_{\mathrm{B}}^2}{R_{\mathrm{on,sp}}}\right|_{\mathrm{opt}} = \mu_n \epsilon_s \left(\frac{2E_{\mathrm{c}}}{3}\right)^3 \tag{8}$$

where V_{B} is the breakdown voltage, $R_{\mathrm{on,sp}}$ is the specific on resistance, E_{c} is the critical electric field, μ_n is electron mobility parallel to the c axis and ϵ_s is the SiC dielectric constant.

Values of the accumulation layer thickness, length and concentration of $0.3\,\mu\mathrm{m}$, $4\,\mu\mathrm{m}$ and $5.0\times10^{15}\,\mathrm{cm}^{-3}$, respectively, have been established to achieve the desired on- and off-state characteristics. At these optimum values and room temperature, a specific on-resistance of $93.2\,\mathrm{m}\Omega\cdot\mathrm{cm}^2$ and a breakdown voltage of $1460\,\mathrm{V}$ with the corresponding small leakage current was achieved. The effect of the accumulation layer thickness on the maximum operating voltage, specific on-resistance and crite-

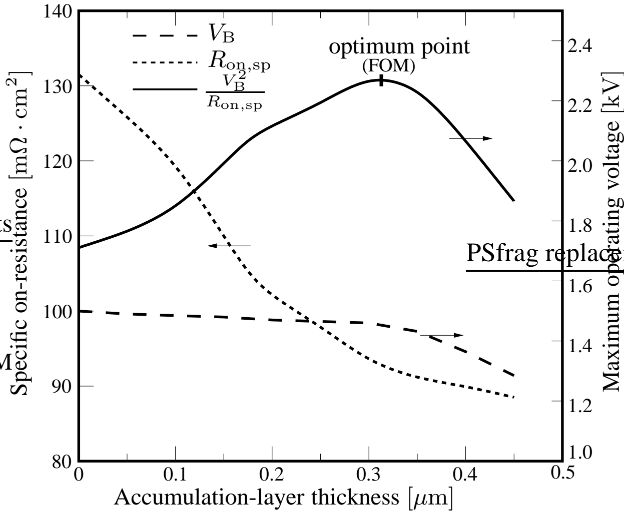

Figure 2. Effect of the accumulation layer thickness on maximum operating voltage and specific on-resistance.

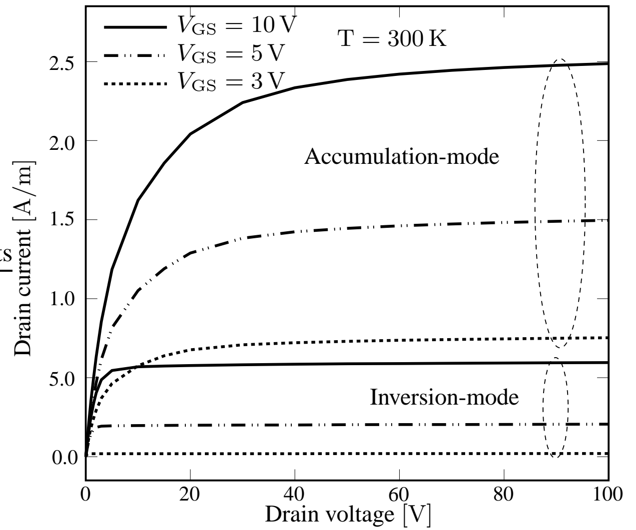

Figure 3. Comparison of output characteristics.

rion for the device optimization obtained by simulation is illustrated in Fig. 2.

The gate oxide overlap was varied from 4 to 7 μm, and its influence on the surface field and operating voltage was analyzed. According to Gauss' law the field in the oxide is approximately 2.5 times higher than the peak field in the SiC bulk. Therefore, the oxide breakdown must not take place before the avalanche breakdown occurs in the SiC bulk. Simulation predicted that a gate oxide overlap length of 6 μm is optimal.

4. Result and Discussion

The proposed accumulation-mode LDMOSFET shows a fairly large advantage in terms of electrical performance compared to its standard inversion-mode LDMOSFET counter part. Excellent I-V characteristics were obtained with good current saturation and gate control as depicted in Fig. 3. One of the important areas of improvement for the SiC MOSFET device is the decrease in its conduction losses which is governed by its specific on-resistance. This on-resistance depends on the channel resistance of the device. An estimate of the on-resistance contribution indicates that 90% of the on-resistance is due to the large channel resistance, owing to the low inversion layer mobility. The proposed structure is able to minimize this resistance and improve the mobility. A simulated accumulation layer mobility of 120 cm^2/Vs compared to the 18 cm^2/Vs for the inversion-layer was observed, which is in a good agreement with the experiment result extracted at a different temperature [9]. Significant improvement on the reduction of the gate bias voltage (a logic level gate bias of 5 V) has been achieved to obtain good on-state conduction as shown in Fig. 4.

The device is normally off with a threshold voltage of only 1 V compared to that of 3 V for the inversion-mode structure. In addition to moving the channel away from the oxide interface and removing the effect of interface quality on the channel mobility, the proposed structure offers the possibility of serving as a shield to the influence of high SiC bulk electric filed on the gate oxide. The peak surface electric field at the maximum operating voltage has been kept below 1.5 MV/cm as depicted in Fig. 5. That is equivalent to the oxide field of 3.75 MV/cm, and considerably lower than the practical limit of the electric field strength in the oxide. Therfore, the proposed structure improves the reliability of the device while utilizing the high breakdown electric field strength of SiC.

A breakdown voltage of 1460 V with a leakage current comparable to that of standard inversion-mode LDMOSFET was achieved as shown in Fig. 6. The off-state leakage current caused by the built-in potential of the p/n junction is ten orders of magnitude less than the on-state current for the same structure, but two order of magnitude greater than the inversion-mode structure. This can

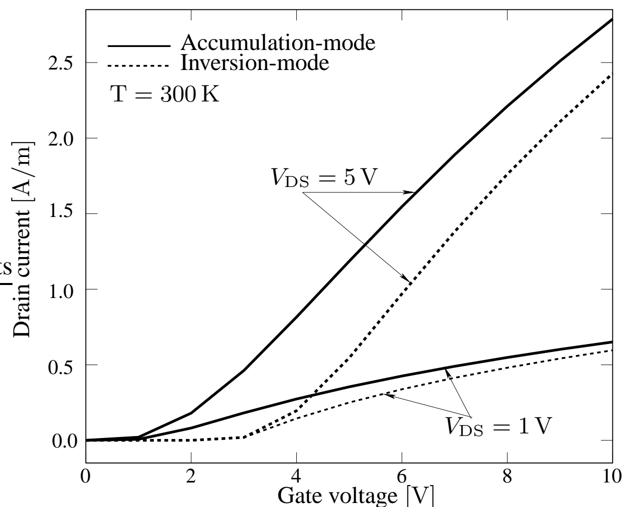

Figure 4. Comparison of transfer characteristics.

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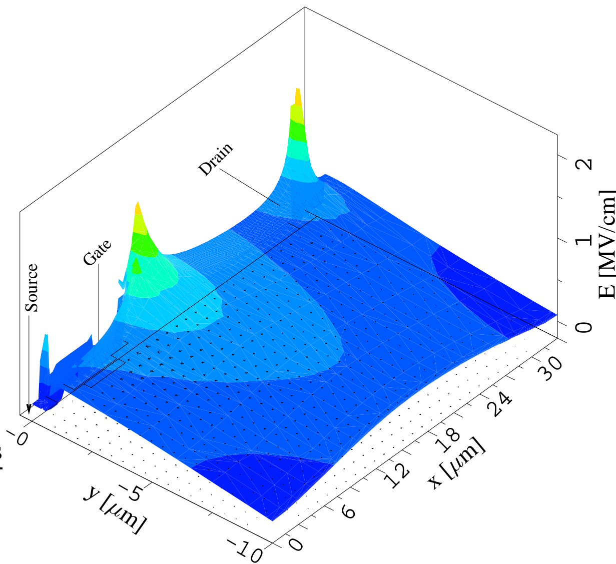

Figure 5. Electric field profile at 1400 V.

effectively be suppressed by calibrating parameters which enable a fully depleted accumulation-layer. High temperature causes an increase in the leakage current due to the reduced on-resistance and increased intrinsic carrier concentration.

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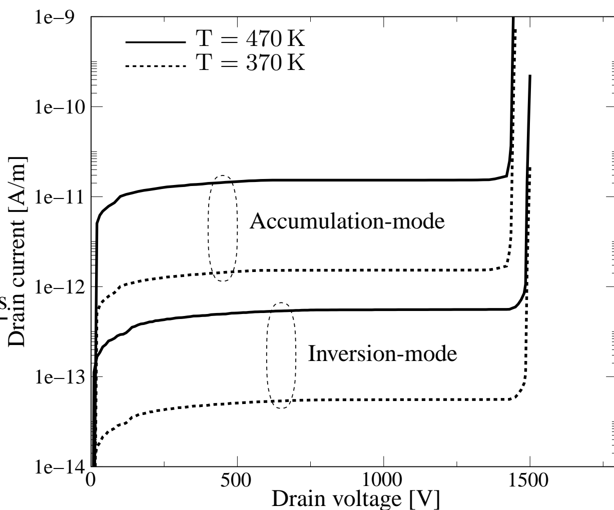

Figure 6. Comparison of off-state characteristics.

5. Conclusion

A new accumulation-mode structure for a silicon carbide laterally diffused MOSFET that minimizes problems caused by lack of material development and design has been proposed, optimized, and analyzed. Improvement on the reduction of the gate bias voltage has been achieved to obtain good on-state conduction. The device exhibits a blocking voltage of 1460 V and a specific on-resistance of 93.2 mΩ·cm^2 at an oxide field of 3.75 MV/cm which is considerably lower than the practical limit of the oxide breakdown field.

6. Acknowledgment

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