Rigorous Modeling of High-Speed Semiconductor Devices

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Abstract— **We present the state-of-the-art in simulation for industrial heterostructure devices based on SiGe/Si and III-V compound semiconductors. The work includes a detailed comparison of device simulators and current transport models to be used, and addresses critical modeling issues. Results from two-dimensional hydrodynamic analyses of Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs) with Minimos-NT are presented in good agreement with measured data. The examples are chosen to demonstrate technologically important issues which can be addressed and solved by device simulation.**

I. INTRODUCTION

Communication and information systems are subject to rapid and highly sophisticated changes. In this development semiconductor heterostructure devices, such as Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs), are among the fastest and most advanced high-frequency devices. They meet well the requirements for low power consumption, medium-integration, low cost in large quantities, and high-speed operation capabilities in circuits in the very high frequency range (recently beyond 500 GHz [1]) and for data rates higher than 100 Gbit/s for long range communication.

To cope with explosive development costs and strong competition in the semiconductor industry today, Technology Computer-Aided Design (TCAD) methodologies are extensively used in development and production. Several questions during device fabrication, such as performance optimization and process control, can be addressed by simulation. The choice of a given simulation tool or a combination of tools depends to a large extent on the complexity of the particular task, on the desired accuracy of the problem solution, and on the available human, computer, and time resources.

Optimization of geometry, doping, materials, and material composition profiles targets at high power, high breakdown voltage, high speed (high f_T, f_{max}), low leakage, low noise, and low power consumption. This is a challenging task that can be significantly supported by device simulation.

The paper gives a review of state-of-the-art device simulators, including the three-dimensional device simulator Minimos-NT, discusses critical modeling issues regarding the simulation of advanced SiGe and III-V semiconductor devices, and concludes with particular simulation results of such devices obtained with the same simulation tool, model set, and set of model parameters. We demonstrate by examples from industrial vendors how a well-calibrated tool can address technologically important issues, such as process variation or reliability.

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II. HETEROSTRUCTURE DEVICE SIMULATORS

The continously increasing computational power of computer systems allows the use of TCAD tools on a very large scale. Several commercial device simulators, e.g. [2]-[7], company-developed simulators, e.g. [8], [9], and University developed simulators, e.g. [10]-[16] have been successfully employed for device engineering applications. However, most of them were focused on silicon devices. These simulators differ considerably in dimensionality (one-, /quasi-/two-, or /quasi-/three-dimensional), in choice of carrier transport model (drift-diffusion, energy-transport, or Monte Carlo statistical solution of the Boltzmann equation), and in the capability of including electrothermal effects. The drift-diffusion transport model [17] is by now the most popular model used for device simulation. With down-scaling feature sizes, non-local effects become more pronounced and must be accounted for by applying an energy-transport or hydrodynamic transport model [18]. During the last two decades Monte Carlo methods for solving the Boltzmann transport equation have been developed [19], [20] and applied for device simulation [21]-[23]. However, reduction of computational time is still an issue and, therefore, Monte Carlo device simulation is still not feasible for industrial application on daily basis. An approach to preserve accuracy at lower computational cost is to calibrate lower order transport parameters to Monte Carlo simulation data.

In addition, quantum mechanical effects are often neglected or accounted for only by simple models for quantum corrections [24], [25], as solving the Schrödinger or the Wigner equation is extremely expensive in terms of computational resources.

A common drawback is the limited feedback from technological state-of-the-art process development to simulator development. The quality of the physical models can be questioned as the model parameters for SiGe are often simply inherited from parameters for Silicon. Modeling of the properties of AlGaAs, InGaAs, InAlAs was restricted to slight modifications of the GaAs material properties. Additional materials, such as InGaP and other InP-based materials are required for advanced device modeling, together with new material systems, such as the GaN or the GaSb systems, which have entered the III-V world with impressive device results.

Critical issues concerning simulation of heterostructures are frequently not considered, such as interface modeling at heterojunctions, silicon/poly-silicon interfaces for SiGe devices and insulator surfaces for III-V devices. Hydrodynamic and high-field effects, such as carrier energy relaxation, impact ionization, and self-heating effects, are often ignored.

The two-dimensional device simulator PISCES [10], developed at Stanford University, incorporates modeling capabilities for Si, GaAs, and InP based devices. One of its versions,

PISCES-HB, includes harmonic balance for large signal simulation. Another version G-PISCES from Gateway Modeling [6] has been extended by a full set of III-V models. Examples of MESFETs, HEMTs, and HBTs for several material systems, e.g. InAlAs/InGaAs, AlGaAs/InGaAs, AlGaAs/GaAs, and InGaP/GaAs HBTs are demonstrated. A disadvantage of this simulator is the lack of appropriate energy transport or hydrodynamic transport models, necessary to model high-field effects, in comparison to the original version of PISCES.

The device simulator MEDICI from Synopsis [7], which is also based on PISCES, offers simulation capabilities for SiGe/Si HBTs and AlGaAs/InGaAs/GaAs HEMTs. Advantages of this simulator are hydrodynamic simulation capabilities and the rigorous approach to generation/recombination processes. In addition, it includes a module treating anisotropic material properties. In the newest version, a hetero-interface model was included. Next to modeling of III-V materials this simulator has some weakness in the capabilities of mixed-mode device/circuit simulation. However, it has been successfully used for the simulation of AlGaAs/GaAs HBTs [26].

At the quantum level, among others, a one-dimensional Schrödinger-Poisson solver NEMO [9], based on non-equilibrium Green's functions, is offered for sub-0.1 μm SiGe structures. POSES [6] from Gateway Modeling is another Schrödinger-Poisson solver proposed for charge analysis in HEMT devices for process control.

The two- and three-dimensional device simulator DESSIS from ISE [5] has demonstrated a rigorous approach to semiconductor physics modeling. Various critical issues, such as extensive trap modeling, are solved. Some steps in direction of interface and III-V modeling have been reported [27].

Quasi-two-dimensional approaches using a simplified one-dimensional current equation are demonstrated, among others, by BIPOLE3 from BIPSIM [4] which additionally features good models for poly-silicon.

In the program SIMBA [28] a link between a one-dimensional Schrödinger solver and a two-dimensional Poisson solver is demonstrated. SIMBA also provides drift-diffusion transport simulations of GaN HEMTs.

Using a one-dimensional current equation quasi-two-dimensional approaches are demonstrated in several publications by the University of Leeds [29]. This computation time effective approach has also been verified against Monte Carlo simulation for some examples for gate-lengths down to 50 nm [30].

A similar quasi-two-dimensional tool is Fast Blaze from Silvaco, also based on code from Leeds, which together with the two-dimensional tool ATLAS [3] has claimed the simulation of AlGaAs/GaAs and pseudomorphic AlGaAs/InGaAs/GaAs HEMTs. Simulations of SiGe HBTs have also been announced, based on a simulator originally developed at the University of Ilmenau, PROSA [16]. However, in the latter no material interfaces are considered.

Several good optimization results for SiGe HBTs were achieved with another University developed simulator, SCORPIO [31].

Table I summarizes features of device simulators discussed in this paper.

TABLE I
COMPARISON OF DIFFERENT DEVICE SIMULATORS,
(DD) DRIFT-DIFFUSION MODEL, (ET) ENERGY TRANSPORT MODEL,
(HD) HYDRODYNAMIC MODEL, (TE) THERMIONIC EMISSION,
(TFE) THERMIONIC FIELD EMISSION.

Simulator	Dimension	Model	Features
POSES	1D		Schrödinger-Poisson solver
NEMO	1D		Schrödinger-Poisson solver
BIPOLE3	quasi-2D	DD	poly-silicon
Leeds	quasi-2D	HD	Schrödinger equation, thermal model
Fast Blaze	quasi-2D	HD	
ATLAS	2D	DD,ET	TE heterojunction model
APSYS	2D	HD	optical, interfaces
Jungemann	2D	DD,HD,MC	rigorous transport modeling
PISCES	2D	DD,ET	III-V models, poly-silicon
PISCES-HB	2D	DD	harmonic balance
G-PISCES	2D	DD	full set III-V models
MEDICI	2D	DD,HD	anisotropic properties, TFE model
SIMBA	2D,3D	DD	Schrödinger equation
FIELDAY	2D,3D	DD	electrothermal
Minimos-NT	2D,3D	DD,HD	(see Section III)
DESSIS	2D,3D	DD,HD	trap modeling, TFE model

III. CRITICAL ISSUES OF MODELING HETEROSTRUCTURE DEVICES

This section discusses critical modeling issues for heterostructure devices. We have addressed these issues in our three-dimensional device simulator Minimos-NT [32], which can deal with different complex structures and materials, such as SiGe and various III-V binary and ternary compounds, with arbitrary material composition profiles in a wide temperature range.

The models are based on experimental or Monte Carlo simulation data and employ analytical functional forms which cover the whole material composition range. The model parameters are checked against several independent HEMT and HBT technologies to obtain a concise set used for all simulations. Reviewing simulation of HBTs and submicron HFETs with gate-lengths down to 100 nm used for mm-wave devices, solutions of energy transport equations are necessary to account for non-local effects, such as velocity overshoot. A model for carrier temperature dependent energy relaxation times [33] has been developed as well as a model for lattice temperature dependent saturation velocities [34].

Heterointerface modeling is a key issue for devices which include abrupt junctions. Thermionic emission and field emission effects critically determine the current transport parallel and perpendicular to the heterointerfaces. Another critical issue for recessed HFETs and for III-V HBTs is the description of the semiconductor/insulator interface. Fermi-level pinning prevails especially for typical barrier materials such as AlGaAs or InAlAs, for ledge materials such as InGaP, and insulators such as SiN.

Modeling of strained SiGe is not a trivial task, since special attention has to be focused on the stress-dependent change of the

bandgap due to Ge content [35]. This effect must be separated from dopant-dependent bandgap narrowing which for itself depends on the semiconductor material composition, the doping concentration, and the lattice temperature [36].

As the minority carrier mobility is of considerable importance for bipolar transistors, an analytical low field mobility model which distinguishes between majority and minority electron mobilities has been developed [36] using Monte Carlo simulation data for electrons in Si and SiGe. Monte Carlo simulation which accounts for alloy scattering and splitting of the anisotropic conduction band valleys due to strain in combination with an accurate ionized impurity scattering model [37] allowed us to obtain results for SiGe for the complete range of donor and acceptor concentrations and Ge contents x. The good agreement of the model with the measured and the Monte Carlo simulation data, both for in-plane and perpendicular to the surface directions, is illustrated in Fig. 1.
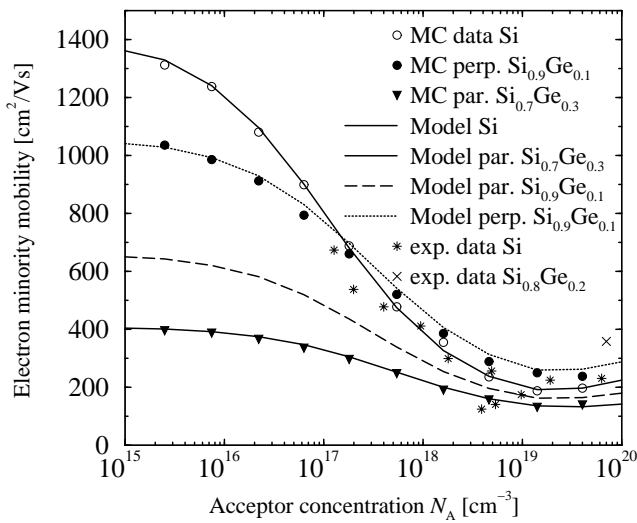
Fig. 1. Minority electron mobility in $Si_{1-x}Ge_x$ as a function of N_A and x: The model gives good agreement with measurements and Monte Carlo simulation data both for in-plane and perpendicular to the surface directions.

All the important physical effects, such as bandgap narrowing, anisotropic electron minority mobility in strained SiGe, Shockley-Read-Hall recombination, surface and Auger recombination, and impact ionization are taken into account. III-V materials and SiGe are known to have a reduced heat conductivity in comparison to Silicon [38]. Self-heating effects are accounted for by solving the lattice heat flow equation self-consistently with the energy transport equations. Examples are given in the next section for both HEMT and HBT devices.

Advanced device simulation allows a precise physics-based extraction of small-signal parameters [39], [40]. Measured bias dependent S-parameters serve as a valuable source of information when compared at different bias points to simulated S-parameters from a device simulator, such as Minimos-NT. This procedure reflects the full RF-information contained in the S-parameters and allows process control beyond the comparison of DC-quantities.

IV. SELECTED RESULTS OF INDUSTRIALLY RELEVANT DEVICES

It is well known that GaAs-HBTs with an InGaP ledge have an improved reliability [41]. Power amplifiers with InGaP/GaAs HBTs are part of many cellular phones today. Two-dimensional device simulation allows the analysis of experimental data in cases which cannot be explained by simple analytical assumptions. This proved to be especially useful for explaining and avoiding device degradation which occurs as a result of electrothermal stress aging. The impact of the ledge thickness and the negative surface charges existing at the ledge/nitride interface, was studied for a one-finger $3 \times 30~\mu m^2$ InGaP/GaAs HBT with respect to reliability [42]. We found a surface charge density of $\rho_{surf} = 10^{12}~cm^{-2}$ to be sufficient to get good agreement with the measured Gummel plots at $V_{CB} = 0$ V. Simulation results for the electron current density at $V_{BE} = 1.2$ V without and with a surface charge density of $10^{12}~cm^{-2}$, respectively, are shown in Fig. 2 and Fig. 3. Based on these investigations it is possible to explain the base current degradation (see Fig. 4) of a strongly stressed device by a decrease in the effective negative surface charge density along the interface from $10^{12}~cm^{-2}$ to $4 \times 10^{11}~cm^{-2}$ due to compensation mechanisms [43].
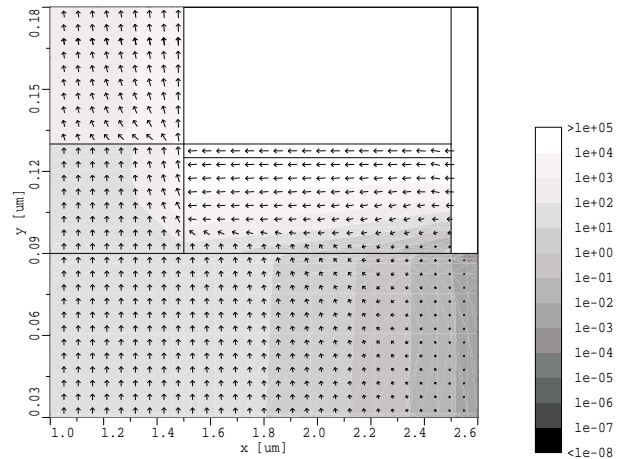

Fig. 2. Electron current density [A/cm^2] at $V_{BE} = 1.2$ V: Simulation without surface charges.
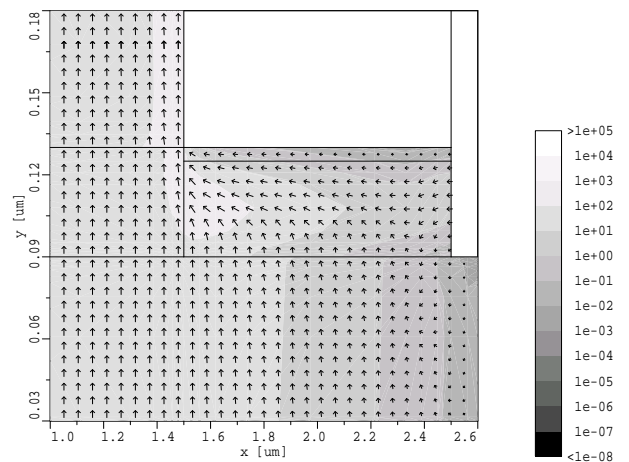

Fig. 3. Electron current density [A/cm^2] at $V_{BE} = 1.2$ V: Simulation with a surface charge density of $10^{12}~cm^{-2}$.
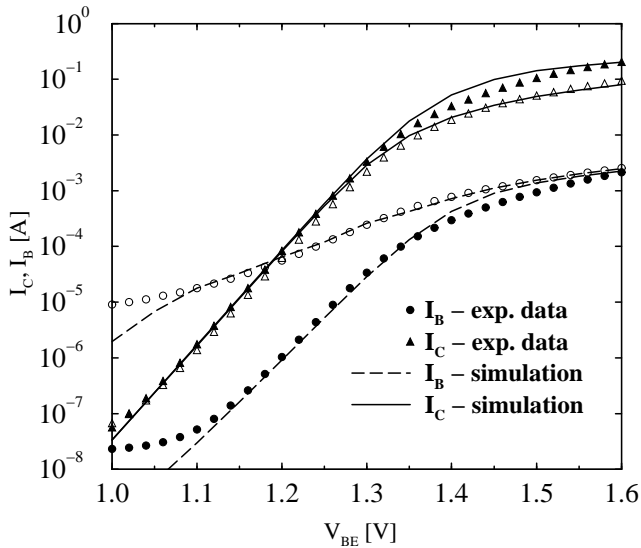
Fig. 4. Comparison of measurements (symbols) and simulations (lines) before (filled) and after (open) HBT aging

For HFET performance the very critical issues are process control and inverse modeling of geometrical structures. Various examples for high-power AlGaAs/InGaAs/GaAs and high-speed InAlAs/InGaAs/InP HEMTs are demonstrated in [44].

Two factors contribute to the gate currents in pseudomorphic GaAs HEMTs: thermionic field emission (TFE) effects and impact ionization are analyzed in detail in [45], [46]. For high-speed InAlAs/InGaAs HEMTs, the precise evaluation of low voltage or low power capabilities is useful for development of high-speed optical data transmission beyond 40 Gbit/s. The comparison of several lattice matched and metamorphic technologies gave consistent simulation parameters also for this material system [47]. Fig. 5 shows simulation and measurements for two different substrate temperatures for a composite channel $In_{0.52}Al_{0.48}As/ In_{0.66}Ga_{0.34}As/In_{0.53}Ga_{0.47}As/InP$ HEMT for $l_g = 150$ nm. High field effects such as impact ionization are considered. This allows the analysis of both, optimized speed and limited gate current, when scaling δ-doping and gate-to-channel separation for the requirements of 80 Gbit/s operation.
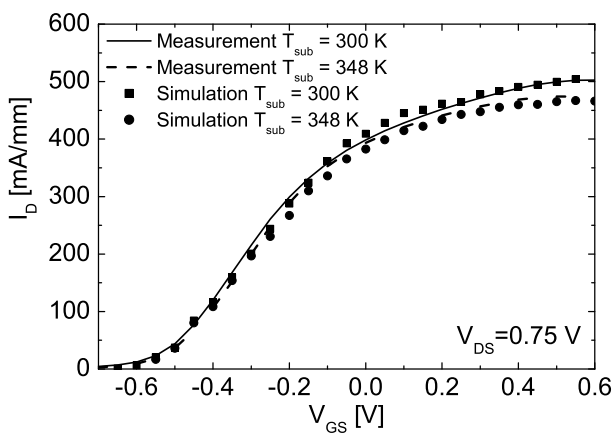

Fig. 5. Transfer characteristics of a composite channel InAlAs/InGaAs/InP HEMT with $l_g = 150$ nm for two different temperatures

The investigated 12×0.4 μm^2 SiGe HBT device structure is obtained by process simulation with DIOS [5] which reflects real device fabrication as accurately as possible. The implant profiles as well as the annealing steps are calibrated to one-dimensional SIMS profiles. To save computational resources the simulation domain covers only one half of the real device which is symmetric and the collector-sinker is not included in the structure (see Fig. 6).
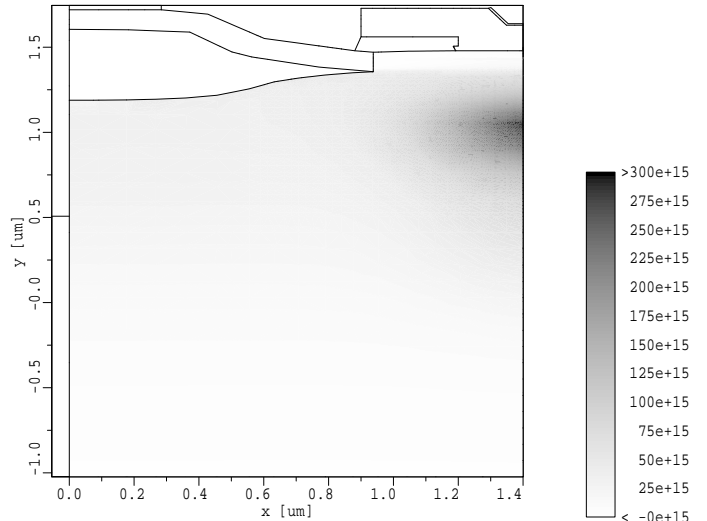

Fig. 6. Simulated device structure and Phosphorus collector implant [cm^{-3}].

All important physical effects, such as surface recombination, generation due to impact ionization, and self-heating, are properly modeled and accounted for in the simulation in order to get good agreement with measured forward (Fig. 7) and output characteristics (Fig. 8) using a concise set of models and parameters. In contrast, simulation without including self-heating effects cannot reproduce the experimental data, especially at high power levels.

The contribution of doping-dependent bandgap narrowing to the conduction band (here about 80% and 20% for donor and acceptor doping, respectively), the concentration of traps in the Shockley-Read-Hall recombination model, the velocity recombination for holes in the poly-silicon contact model [48] used at the emitter contact, and the substrate thermal resistance are the only fitting parameters used in the simulation.

A closer look at the increasing collector current I_C at high collector-to-emitter voltages V_{CE} and constant base current I_B stepped by 0.4 μA from 0.1 μA to 1.7 μA reveals the interplay between self-heating and impact ionization. While impact ionization leads to a strong increase of I_C, self-heating decreases it. In fact, both I_C and I_B increase due to self-heating at a given bias condition. As the change is relatively higher for I_B, in order to maintain it at the same level, V_{BE} and, therefore, I_C decrease.

Since advanced SiGe techniques exhibit competitive performance of high frequency devices in markets that were prior the domain of other materials, small-signal analysis by means of simulation of these devices becomes more important. Fig. 9 shows a comparison between measured and simulated S-parameters in the frequency range between 50 MHz and 31 GHz at $V_{CE} = 1$ V and current density $J_C = 76$ kA/cm^2.
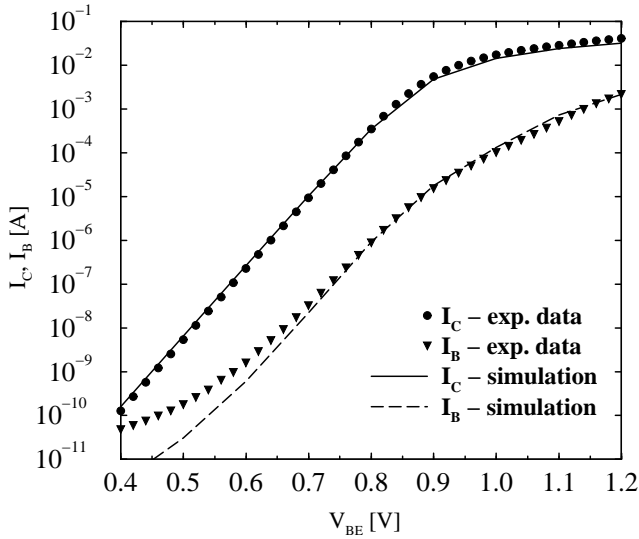
Fig. 7. Forward Gummel plots at V_{CB} = 0 V: Comparison between measurement data and simulation at room temperature. The bandgap is one of the crucial modeling parameters.
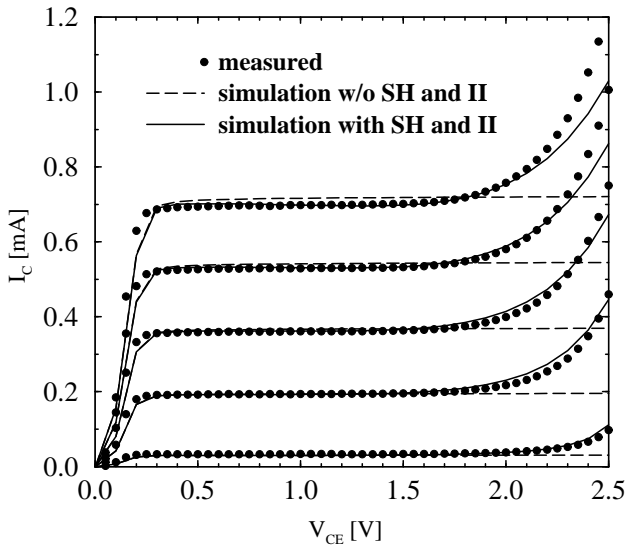

Fig. 8. Output characteristics: Simulation with and without self-heating (SH) and impact ionization (II) compared to measurement data. I_B is stepped by 0.4 μA from 0.1 μA to 1.7 μA.

We calculated the matched gain g_m and the short-circuit current gain h_{21} in order to extract the figures of merit f_T (short-circuit cut-off frequency) and f_{max} (maximum oscillation frequency) found at the unity gain point. Fig. 10 and Fig. 11 show the comparison of our results and the corresponding measurement data. While the measurement data ends at 31 GHz the simulation could be extended to frequencies beyond this intersection. The peak of the f_T-curve in Fig. 10 corresponds exactly to the frequency at the respective intersection in Fig. 11. Fig. 10 shows also the effect of an anisotropic electron mobility. In addition, results obtained by a commercial device simulator (DESSIS [5]) using default models and parameters are included for comparison.
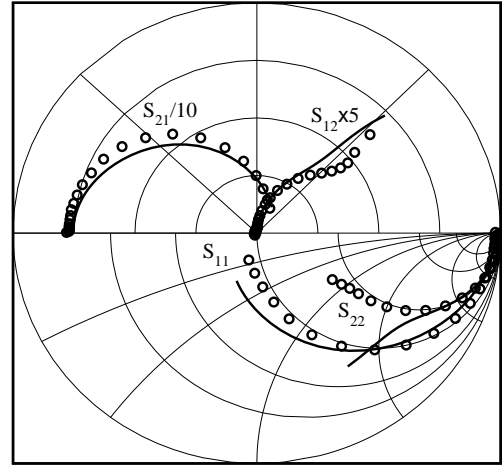

Fig. 9. S-parameters in a combined Smith chart (radius = 1) from 50 MHz to 31 GHz at V_{CE} = 1 V and current density J_C = 76 kA/cm^2 (measurements with circles).
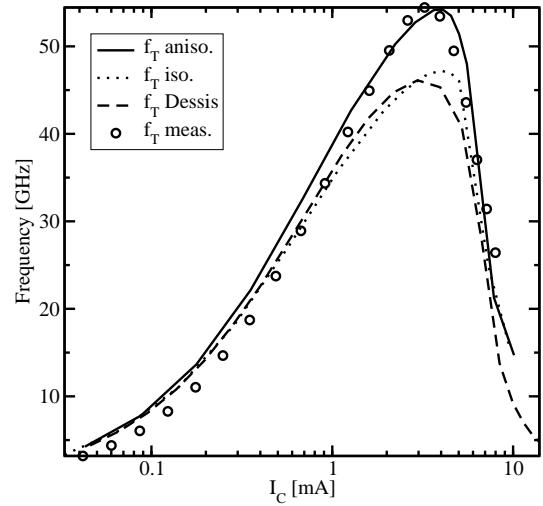

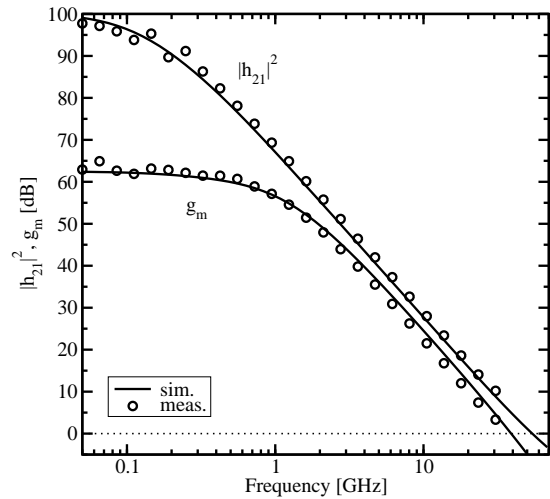Fig. 10. Cut-off frequency f_T versus collector current I_C at V_{CE} = 1 V.

Fig. 11. Short-circuit current gain h_{21} and matched gain g_m vs. frequency at V_{CE} = 1 V and current density J_C = 76 kA/cm^2.

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V. Conclusion

A brief overview of the state-of-the-art of simulation tools for heterostructure RF-devices has been given. We have presented experiments and simulations of SiGe and GaAs HBTs. Good agreement was achieved both with experimental DC-results (forward and output characteristics) and with high-frequency data. With an increasing number of stable and reliable heterostructure technologies available, a meaningful comparison between simulation results and statistically analyzed data is possible and delivers on the one hand side model verification, and on the other hand side valuable process information.

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