Optimization of Electrothermal Material Parameters using Inverse Modeling

Rainer Minixhofer*, Stefan Holzer°, Clemens Heitzinger†, Johannes Fellner*,
Tibor Grasser°, and Siegfried Selberherr†
*austriamicrosystems AG, A-8141 Unterpremstätten
°Christian Doppler Laboratory for TCAD in Microelectronics
at the Institute for Microelectronics
†Institute for Microelectronics, TU Vienna, A-1040 Vienna, Austria
Rainer.Minixhofer@austriamicrosystems.com

Abstract

A method for determining higher order thermal coefficients for electrical and thermal properties of metallic interconnect materials used in semiconductor fabrication is presented. By applying inverse modeling on transient electrothermal three-dimensional finite element simulations the measurements of resistance over time of Polysilicon fuse structures can be matched. This method is intended to be applied to the optimization of Polysilicon fuses for reliability and speed.

1. Introduction

For deep-submicron semiconductor process technology nodes, the use of Polysilicon fuses, as one-time-programmable devices providing memories up to several kilobits, offers a cheap, efficient, and area-saving alternative to small non-volatile memories for System-on-a-Chip solutions. Approaches to increase this memory densities by using 3-state fuses of layered materials are also reported [8]. Another important application is the use in simple field programmable gate arrays or for trimming CMOS circuits for specific analog performance [9]. Furthermore, the fuses are used to provide variable elements as trimmable resistor or capacitor arrays [6]. Finally the fuses may act as the classical protective elements for improved protection and replacement of critical components before actual failures [11]. Programming is done by sending a broad current pulse through the fuse, resulting in open-circuit the Polysilicon film after transition to a second-breakdown state. The transition occurs when parts of the Polysilicon layer reach the Silicon melting point, and the molten Silicon is transported from the negative end through drift of ions in the applied field [4]. Fuses implemented in deep submicron technologies become more and more attractive in terms of power and area consumption, and hybrid approaches using other materials are getting less important [7]. Nevertheless, going to smaller ground rules below 350 nm, implies decreasing supply voltages to 1.5 V and below [10]. This constraint requires a careful optimization of the fuse layout, ensuring an efficient and reliable programming mechanism [3] and minimizing the necessary power consumption of the fusing process. As the fusing process takes place in a short time interval (between a couple of nanoseconds up to the microsecond range), direct thermal measurements of this process are quite hard to obtain. Previously carried out work [12] already shed some light on the physics behind the fusing mechanism, but the optimization of the fuse structure for reliable and fast fusing was only possible via expensive experimental work by using test chips.

This work focuses on gaining better insight into the materials characteristics used in the structure, to enable a layout optimization through simulation. Since the electrical and thermal properties of Polysilicon are a complex function of Polysilicon film doping, grain size, and grain morphology [5], the average electrical and thermal properties as a function of temperature were obtained by experimentally measuring the transient resistivity response of the fuse through Joule self-heating, and subsequent inverse modeling this measured data, to fit the observed behavior. The electro-thermal self-heating simulations were done using the Smart-Analysis-Package (SAP) for three-dimensional interconnect simulation [1] in combination with SIESTA, a TCAD optimization framework combining gradient based and genetic optimizers [2]. This approach enabled the optimization of the fuse layout of such devices by significantly saving costs normally spent in design and production of layout test chips. Furthermore, a better insight into the transient electro thermal effects occurring in the first couple of microseconds was gained.

2. Experiment

The fuse devices were fabricated in an industry-standard deep submicron polycided gate CMOS process. On a specialized test chip multiple different layout variations were placed to find the optimum layout for fast and reliable fusing. A more complicated example of a fuse structure is shown in Fig. 3. The first experiments were done with rectangular pulses. Nevertheless, through the steep slope of the fuse terminal voltage the initial time regime of the fuse heating is not well resolved. Further-

0-7803-7999/03/$17.00©2003 IEEE

more, the initial transient behavior of the measurement circuit yields high errors in the measured current data. To overcome these problems a voltage ramp was applied and the resulting fusing resistance was calculated by assuming ohmic behavior. The Polysilicon layer in the fuse is doped to solid solubility, and therefore its conductivity may considered to be approximately ohmic. Since all materials in the fuse except the Polysilicon layer are metallic, this assumption shall give a reasonable estimate for the fuse resistivity. The devices were stressed with different triangular voltage ramps for a few microseconds. A pulse generator was used to define the length of the pulse. As the generator has a typical output impedance of 50 Ω and the resistor of the Polysilicon fuse is lower than that, the source has to be buffered by an operational amplifier with a high slew rate to get a stable voltage. To avoid an additional voltage drop on a shunt resistor a current probe was used. In addition, the voltage on the fuse was monitored by an oscilloscope to calculate the right resistor value. The measurement principle can be seen in Fig. 1.

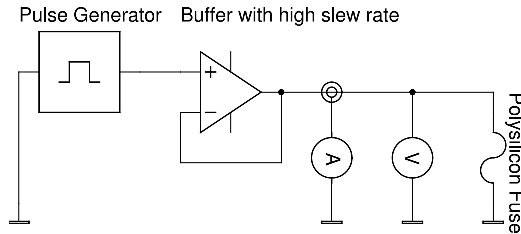

Figure 1. Schematic of the Polysilicon fuse measurement

The resulting measurement data for three different source voltages as a function of time are shown in Fig. 2.

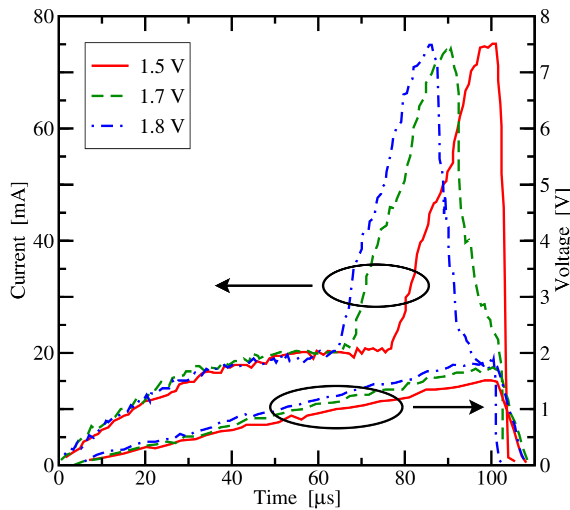

Figure 2. Measured current through fuse and voltage at the fuse terminals as a function of time

The resistance difference between the three voltages is because of self heating of the whole structure (including the contact barrier layers) in the first microsecond of the applied pulse. The negative temperature coefficient of the resistance in all three curves is through the combined Joule self-heating of the Polysilicon/Polycide layer sandwich (see Fig. 3). The high noise in the data during the first 10μs is because of the low voltage level in this time regime and the resulting low signal-to-noise ratio.

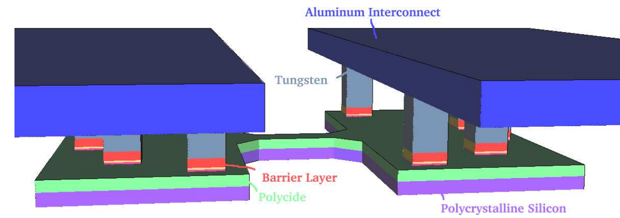

Figure 3. Fuse device structure showing the variety of included materials

3. Simulation and Inverse Modeling

3.1. Mathematical Models

For the numerical calculation of Joule self-heating effects two partial differential equations have to be solved. Poisson's equation

$$\mathrm{div}(\gamma_{\mathrm{E}}\,\mathrm{grad}\,\varphi) = 0 \tag{1}$$

gives the electric potential φ where γ_{E} denotes the electric conductivity. The power loss density p is obtained by computing $p = \gamma_{\mathrm{E}}(\mathrm{grad}\,\varphi)^2$. The heat conduction equation

$$c_{\mathrm{p}}\,\rho_{\mathrm{m}}\,\frac{\partial T}{\partial t} - \mathrm{div}(\gamma_{\mathrm{T}}\mathrm{grad}\,T) = -p \tag{2}$$

is solved to obtain the temperature distribution where γ_{T} represents the thermal conductivity, c_{p} the specific heat, and ρ_{m} the mass density. The temperature dependence of the conductivities is modeled with

$$\gamma(T) = \frac{\gamma_0}{1 + \alpha(T - T_0) + \beta(T - T0)^2} \tag{3}$$

where γ_0 is the thermal or electrical conductivity at the temperature T_0, α and β are the linear and quadratic temperature coefficients of the specified materials.

3.2. Simulation Setup

The layout of the fuse was transformed into a three-dimensional representation of the device using a detailed process description of the interconnect forming deposition and etch steps. With the well known electrical conductivity of the interconnect and barrier layers the structural setup was checked by calculating the overall resistance of the structure excluding self-heating effects. The Polysilicon conductivity was matched to the observed overall resistance and the resulting value was compared to independently measured sheet resistances of the polycrystalline

layer in fabrication, resulting in an excellent agreement between the ohmic simulation and the measurements. The subsequent transient simulations were set up including the thermal coefficients of the electrical conductivity, the thermal conductivity, and the heat capacity of all layers in the structure. The starting values of these parameters were taken from literature data.

3.3. Inverse Modeling

The simulation framework SIESTA provides a wide range of optimizers that can be chosen to fit best for the current problems. Reference data for this optimization are measurements of the resistance calculated from Fig. 2. At start time SIESTA provides the initial values of the free parameters for the three-dimensional interconnect simulator STAP of the SAP package, as introduced in [1]. The output of the simulation is parsed by SIESTA in order to compare it with the reference data. It produces a score value that indicates how good these two data sets match. This value is submitted to the optimizer which generates corresponding to the score value the next n-tuple of free parameters to improve the next score value that will be evaluated after the next simulation run with the currently produced values.

The optimizer mainly used in SIESTA is a genetic optimizer that relies on the theory of evolutionary computation and generic algorithms described in [2]. The population of the n-tuples of free parameters are chosen randomly with respect to a Gaussian normal distribution where a lot of distribution and generation parameters can be configured and tuned for special kinds of problems. Furthermore, the simulation of the population can be distributed on a computer cluster to significantly decrease the optimization time.

Wide interval ranges of free parameters can result in convergence problems because of non-physical parameter values which would cause negative resistance or negative doping. To avoid this, the simulation framework SIESTA provides a kind of divergence detection where SIESTA is signaled when the simulator has problems to converge. This feature allows the user to expand the intervals of the free parameters in a larger range as before.

4. Results and Discussion

The simulation framework SIESTA has to fit the thermal parameters of the electrical and thermal conductivities in order to minimize the difference between the reference and the simulation. To check the consistency of the setup, all thermal and electrical parameters were used for the automated simulation run, resulting in a total of 10 parameters. The resulting best fit to the measured reference data is given in Table 1. The electrical and thermal conductivities $\gamma_{0,\mathrm{E}}$ and $\gamma_{0,\mathrm{T}}$ as well as the linear temperature coefficient of the thermal conductivity α_T for Polysilicon are in excellent agreement compared to data reported in [5]. The electrical conductivity of the Polysilicon/Tungsten Silicide sandwich as a function of temperature is comparable to data measured electrically by external heating of the layers.

Table 1. Parameters of electrical and thermal conductivity for materials used in the fuse structure

	Poly Si	WSi_2
$\gamma_{0,\mathrm{E}}$ $[1/\mu\Omega\mathrm{m}]$	0.12	1.25
α_E [1/K]	9.1×10^{-4}	8.9×10^{-4}
β_E $[1/\mathrm{K}^2]$	7.9×10^{-7}	8.1×10^{-7}
$\gamma_{0,\mathrm{T}}$ [W/Km]	45.4	119.4
α_T [1/K]	2×10^{-2}	2.98×10^{-2}

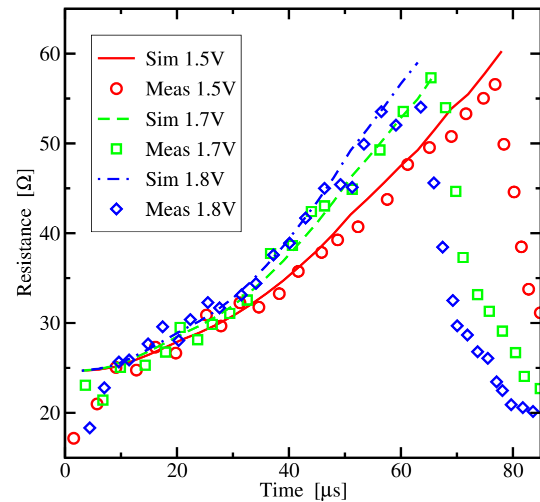

Figure 4. Comparison of measured and simulated resistance as a function of time

The optimized parameter set results in resistance characteristics as shown in Fig. 4 where an excellent match with the measurements is obtained. The strong increase of the resistance as a function of time because of self heating can be clearly seen. In addition, after a certain critical temperature is reached the resistance drops dramatically and the ohmic approximation looses its validity. To generalize this result to other fuse geometries this critical temperature has to be extracted. As expected, the critical temperatures of all the three samples are inside of a small interval about 1150 K (cf. Fig. 6). This value is much smaller as the single crystal Silicon melting point of 1414 °C and the Tungsten Silicide (WSi_2 phase) melting point of 2015 °C [14]. The maximum temperature of the Polysilicon fuse is observed in the center of the Tungsten Silicide layer as shown in Fig. 6.

Several mechanisms for this low critical temperature are possible. First, the disordered region between the Tungsten Silicide and the Silicon may have a stoichiometry closer to the eutectic point of the Tungsten-Silicide system and therefore a lower melting point. But since the lowest eutectic temperature of the W-Si system is 1389 °C [14], this is not likely for pure alloys. Second, the high doping concentration of the Polysilicon layer reduces the melting temperature as reported for Silicon glasses with

high Boron and Phosphorus contents. And finally, the assumption that all materials show Ohmic behavior over the full temperature range between 300 and 1200 K does not hold for higher temperatures.

The intended target for getting the possibility to optimize fuse layouts for better performance is not affected since it is obvious from Fig. 5 that the melting begins always at approximately the same temperature. Therefore the method should be applicable for other geometries as well. The agreement between experiment and simulation is excellent and provides a reliable base for carrying out predictive simulations of the transient temperature distribution during the initial heating phase of the fusing.

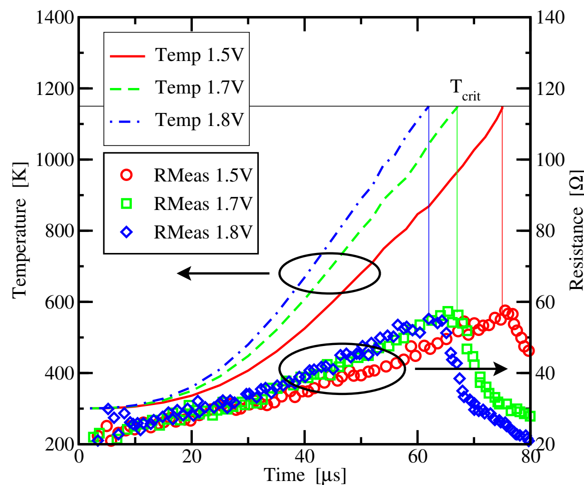

Figure 5. Comparison of the simulated temperature and measured resistance showing the extracted critical temperature

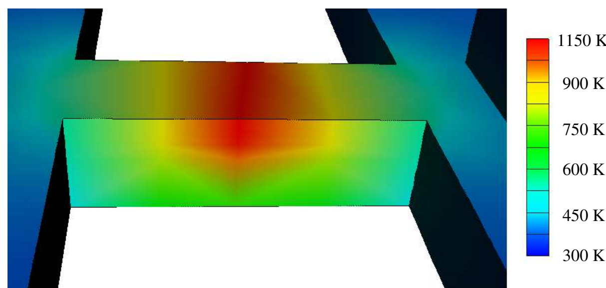

Figure 6. Temperature distribution in the interconnect structure at 65 μs and 1.7 V

5. Conclusion

We have presented a method for obtaining important material parameters by inverse modeling using finite element simulations of complex interconnect structures. This method is capable of describing the electrical behavior of interconnect materials over a significant temperature interval. Furthermore it uses the transient thermal self-heating effect to separate different materials and their electrical and thermal properties. Nevertheless, the exact conduction mechanism inside the Polysilicon layer is still not well reflected in this analysis. In further work the impact of the grain boundary barriers and their behavior at high temperature has to be addressed by implementing a more accurate model like the model of Mandurah [13]. It was demonstrated that the method is consistent and gives an excellent match to experimental results. With the extracted critical temperature, where the material looses its ohmic properties, the geometry can be optimized in terms of reliability and speed.

[1] R. Sabelka, "A Finite Element Simulator for Three-Dimensional Analysis of Interconnect Structures", *Microelectronics Journal*, Vol.32, No.2, 2001, pp. 163-171.

[2] C. Heitzinger, S. Selberherr, "An Extensible TCAD Optimization Framework Combining Gradient Based and Genetic Optimizers", *Microelectronics Journal*, Vol.33, No.1-2, 2002, pp. 61-68.

[3] D.W. Greve, "Programming Mechanism of Polysilicon Fuse Links", *Int. Electron Devices Meeting*, IEDM'81 1981, pp. 70-73.

[4] D.W. Greve, "Programming Mechanism of Polysilicon Resistor Fuses", *IEEE Trans. Electron Devices*, Vol.ED-29, No.4, 1982, pp. 719-724.

[5] A.D. McConnel, S. Uma, K.E. Goodson, "Thermal Conductivity of Doped Polysilicon Layers", *Proc. of the Int. Conference on Heat Transfer and Transport Phenomena in Microscal*, G.P. Celata et al., eds., Begell House, New York, 2000, pp. 413-419.

[6] D.J. Nickel, "Element Trimming Fusible Link", *IBM Technical Disclosure Bulletin*, Vol.26, No.8, Jan 1984, p. 4415.

[7] Y. Fukuda, S. Kohda, K. Masuda, Y. Kitano,"A New Fusible-Type Programmable Element Composed of Aluminum and Polysilicon", *IEEE Trans. Electron Devices*, Vol.ED-33, No.2, 1986, pp. 250-253.

[8] J. Doyle,"A Thick Polysilicon Three-State Fuse", *Motorola Technical Developments*, Vol.3, Mar 1983, pp. 31-32.

[9] O. Kim,"CMOS trimming circuit based on polysilicon fusing", *Electronic Letters*, Vol.34, No.4, 19. Feb 1998, pp. 355-356.

[10] A. Kalnitsky, I. Saadat, A. Bergemont, P. Francis,"$CoSi_2$ integrated fuses on poly silicon for low voltage 0.18μm CMOS applications", *Int. Electron Devices Meeting*, 5-8 Dec. 1999, pp. 765-768.

[11] J.R. Lloyd, M.R. Polcari,"Polysilicon Fuse", *IBM Technical Disclosure Bulletin*, Vol.24, No.7A, Dec 1981, p. 3442.

[12] S. Das, S.K. Lahiri,"Transient Response of Polysilicon Fuse-Links for Programmable Memories and Circuits", *Semiconductor Devices (Proc. SPIE Vol.2733)* 11-16 Dec. 1995; New Delhi, India, pp. 232-234.

[13] M.M. Mandurah, K.C. Saraswat,"A Model for Conduction in Polycrystalline Silicon-Part I: Theory", *IEEE Trans. Electron Devices*, Vol.ED-28, No.10, Oct 1981, pp. 1163-1171.

[14] C. Vahlas, P.-Y. Chevalier and E. Blanquet,*CALPHAD*, Vol. 13, 1989, pp. 273-292.