A Method for Generating Structurally Aligned High Quality Grids and its Application to the Simulation of a Trench Gate MOSFET

Clemens Heitzinger, Alireza Sheikholeslami,
Jong-Mun Park, and Siegfried Selberherr
Institute for Microelectronics, TU Vienna, A-1040 Vienna, Austria
Heitzinger@iue.tuwien.ac.at

Abstract

The error of the numeric approximation of the semiconductor device equations particularly depends on the grid used for the discretization. Since the most interesting regions of the device are generally straightforward to identify, the method of choice is to use structurally aligned grids. Here we present an algorithm for generating structurally aligned grids including anisotropy and for producing grids whose resolution varies over several orders of magnitude. Furthermore the areas with increased resolution and the corresponding resolutions can be defined in a flexible manner and criteria on grid quality can be enforced.

The grid generation algorithm was applied to sample structures which highlight the features of this method. Furthermore we generated grids for the simulation of a high voltage trench gate MOSFET. In order to resolve the junction regions accurately, four regions were defined where the grid was grown in several directions with varying resolutions. Finally device simulations performed by MINIMOS NT show current voltage characteristics and the threshold voltage.

1. Introduction

Generating structurally aligned grids is a crucial prerequisite for the accurate simulation of the electric behavior of semiconductor devices. The quality of the numeric approximation of the solution of the device equations by the finite element or the finite volume method particularly depends on the underlying mesh. In addition to aligning the meshes with the structures, it is desirable to be able to enforce quality criteria like the Delaunay criterion or the minimum angle criterion [1].

Here we present a new method to generate structurally aligned triangulations, including anisotropy if desired. The principal idea is to obtain a suitable, not connected set of edges by advancing a front through the simulation domain by a level set algorithm in the first step. In the second step these edges are used as the input for a specialized grid generator that enforces the quality criteria. Although a technique based on the level set method has been used for generating structurally aligned grids [2], that method cannot generate anisotropic grids and no condition concerning the quality of the grid, e.g., minimum angles or the Delaunay criterion, can be guaranteed. However, with our approach we can successfully carry out device simulations with the simulator MINIMOS NT [3] using the grids generated.

After the description of the grid generation algorithm, it is applied to two examples. The first example is a sample structure which highlights the critical parts near the corners. The second example stems from the simulation of a trench gate MOSFET. Here several areas of refinement were chosen and the grid was generated to take the specific structure of the device and location of the junctions into account. This example emphasizes the applicability of the algorithm to real world examples.

Trench gate MOSFETs (TMOSFETs) are useful for power switching at high voltages [4–8]. They also provide advantages because of their geometric layout, i.e., because their inversion and accumulation channel regions are perpendicular to the wafer surface. Hence they enable to maximize the ratio of cell perimeter to area and thus to increase packing density. The TMOSFET considered is a 120V trench gate UMOS transistor (cf. Figure 3). After generating the structurally aligned grid, we present simulated characteristics of this TMOSFET in the final section.

2. The Grid Generation Method

In this section we discuss the algorithm devised for generating structurally aligned grids. The main idea is to advance one or more fronts through the simulation domain using a level set algorithm [9–11] and constant speed functions. For each moving front a certain number of boundaries are extracted. The number of these boundaries and the spacing between them can be arbitrarily defined and depends on the number of advancing level set steps and their time steps. Clearly the spacing between the intermediate boundaries obtained by the level set algorithm will later determine the diameters of the triangles of the final grid.

Since the boundary segments of the intermediate boundaries obtained after surface extraction from the rect-

0-7803-7999-3/03/$17.00©2003 IEEE.

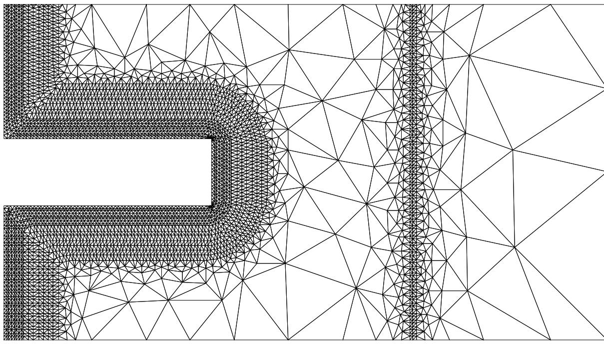

Figure 1. This figure shows a sample structure with angles of 270° and 90°. The set of edges was constructed from three moving boundaries: going downwards from the upper boundary and going upwards and downwards from a boundary in the lower part.

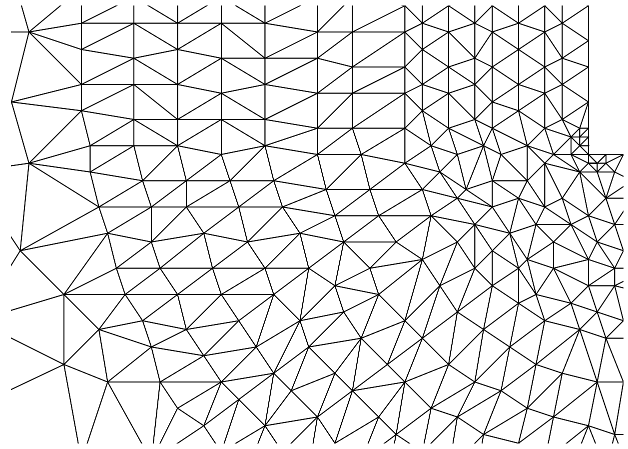

Figure 2. A vertex with an outer angle of 90° of the grid in Figure 1 is magnified.

angular grid may be arbitrarily small, the boundary segments must be normalized. The segments are normalized by choosing points on the boundary that are equidistant when their distance is measured along the boundary. The normalized intermediate boundaries consist of straight lines which are the edges of the final grid to be respected in the second part of the algorithm. This first part of the grid generation is highly customizable and anisotropy can be introduced here by choosing the spacing between the intermediate boundaries and the distance between points of the normalized boundary accordingly.

In the second part of the algorithm the set of edges constructed in the first part serve as input to the actual grid generator. The TRIANGLE program [12] was used in this work because of its robustness. After reworking the edges into the appropriate input format and running TRIANGLE, the output is translated into PIF files [3].

The benefits of this algorithm can be summarized as follows. The grid resolution is customizable and the areas of higher resolution can be chosen arbitrarily. The grid resolution may vary over several orders of magnitude. The algorithm can deal with arbitrary initial structures and an arbitrary number of starting fronts defining areas of high resolution. Anisotropy may be introduced by choosing appropriate parameters for the algorithm. At the same time quality criteria like the Delaunay criterion and requiring that all angles of the triangulation are larger than a certain minimum angle are enforced. It is important to note that the algorithm works reliably, since it is based on edges in contrast to just prescribing sets of points and hence directional information is preserved.

Compared to grid generation algorithms using iso-lines or iso-surfaces of solutions of the Poisson equation, the advantage of this algorithm is its flexibility. This is important, e.g., near the buried layers of SOI devices. The initial boundaries where the advancing fronts start, the prescribed number of intermediate boundaries and their spacing determine the properties of the final grid in a straightforward manner in contrast to the Poisson equation approach.

3. Grid Generation for Sample Structures

The grid in Figure 1 was generated by the above algorithm. The sample structure contains vertices with outer angles of 90° and 270° at the boundary where the grid is finest. Figure 2 shows a magnification of these interesting parts. In the examples we used a constant propagation speed for the first eight steps, starting at the upper boundary, and twice this value for the next seven steps.

Based on the edges constructed in the first step, the grid generator TRIANGLE [12] was used to obtain a Delaunay triangulation. We demanded that the final triangulation contains no angle smaller than 20°. In these examples the grid resolution varies over several orders of magnitude and the critical areas near the corners are resolved without problems.

4. Simulation of a TMOSFET

The device structure of the trench gate UMOS transistor is shown in Figure 3 and its parameters in Table 1. Its trench depth is $3\mu\text{m}$ and its gate oxide thickness is $0.1\mu\text{m}$. It is designed to achieve a forward blocking voltage of 120V.

4.1. Grid Generation

For the grid generation we used four boundaries following the three junctions (cf. Figure 3) and one in the p-region near the gate oxide. First, at the n^+–p junction we used three boundaries in each direction of the initial boundary following the junction with a distance of $0.02\mu\text{m}$ between any two adjacent boundaries.

At the p–n junction we used one boundary above and below the initial boundary and a distance of $0.02\mu\text{m}$. At the n–n^+ junction in the lower part of the device we con-

Table 1. The technological and geometrical parameters considered of the device.

Parameter	Value
n drift doping	$1.5 \cdot 10^{15}\text{cm}^{-3}$
p well doping	$1 \cdot 10^{17}\text{cm}^{-3}$
p well	$\approx 1.4\mu\text{m}$
p^+ buffer	$5 \cdot 10^{18}\text{cm}^{-3}$
n^+ source depth	$\approx 0.38\mu\text{m}$
Gate oxide thickness	$0.1\mu\text{m}$
Trench depth	$3\mu\text{m}$
n drift length	$\approx 9.5\mu\text{m}$

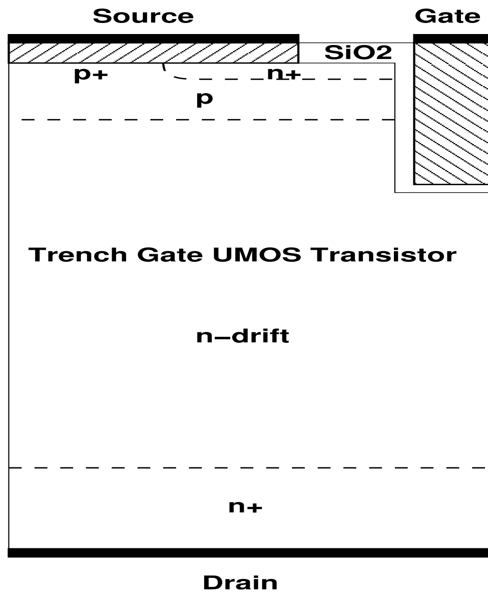

Figure 3. Structure of the TMOSFET. The half cell pitch of the device is $2.5\mu\text{m}$ and its n drift length is about $9.5\mu\text{m}$.

structed two boundaries with a distance of $0.5\mu\text{m}$ going downwards from the initial boundary following the junction. For the last prescribed edges we started at the right hand side of the p-region and moved to the left constructing three boundaries at a distance of $0.005\mu\text{m}$.

In the second step we used the TRIANGLE program requiring a minimum angle of $25°$ with these prescribed edges as input. The grid produced and two enlargements thereof are shown in Figure 4. The junction areas are resolved very finely as demanded.

4.2. Device Simulation

The device simulations were performed using MINIMOS NT [3]. Figure 6 shows typical on-state characteristics of the high voltage TMOSFET. The I–V curves of the figure show that good saturation currents behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Figure 7 for drain voltages of $V_d = 0.1\text{V}$ and 0.5V. From this figure a threshold voltage V_T of 2.5V is obtained. It is important to note that the threshold voltage is independent of the drain voltage.

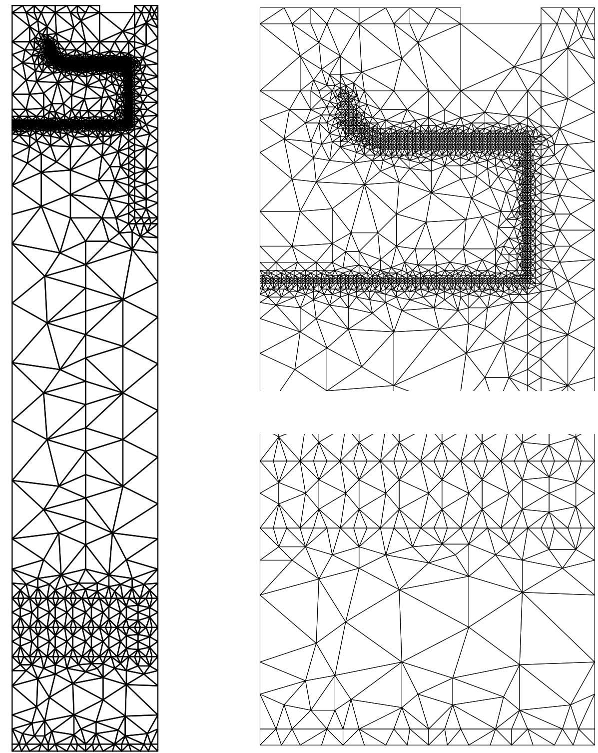

Figure 4. The grid generated for the device in Figure 3. Two enlargements are shown on the right hand side.

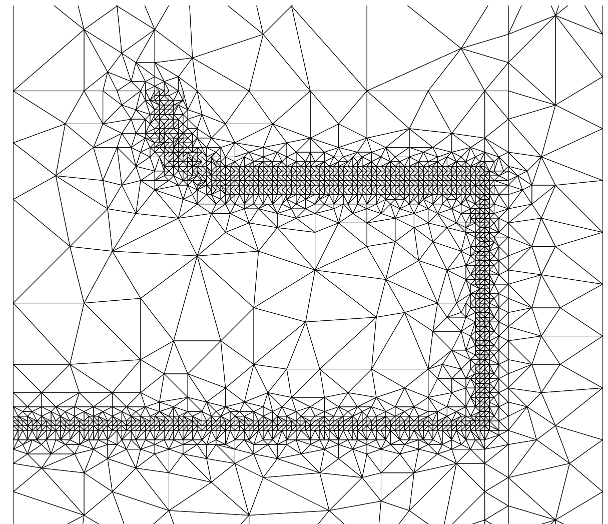

Figure 5. Enlargement of the grid shown in Figure 4.

5. Conclusion

One of the main advantages of this method is the flexibility it provides. The resolution and anisotropy of the grid is customizable and the diameter of the triangles may

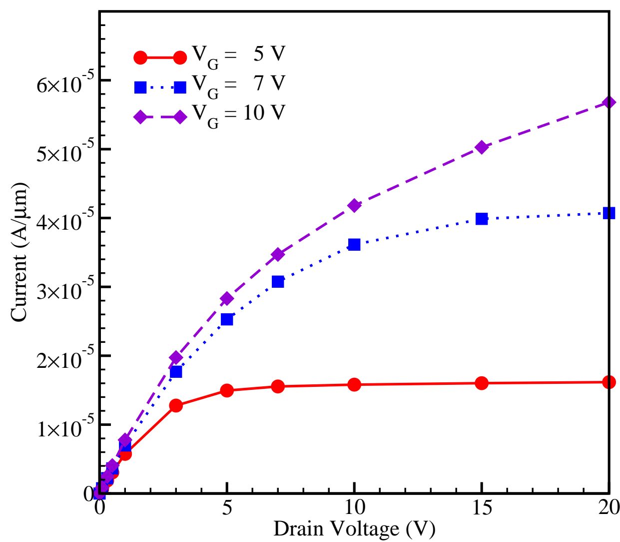

Figure 6. This plot shows the on-state characteristics of the vertical TMOSFET for gate voltages of $5\mathrm{V}$, $7\mathrm{V}$, and $10\mathrm{V}$.

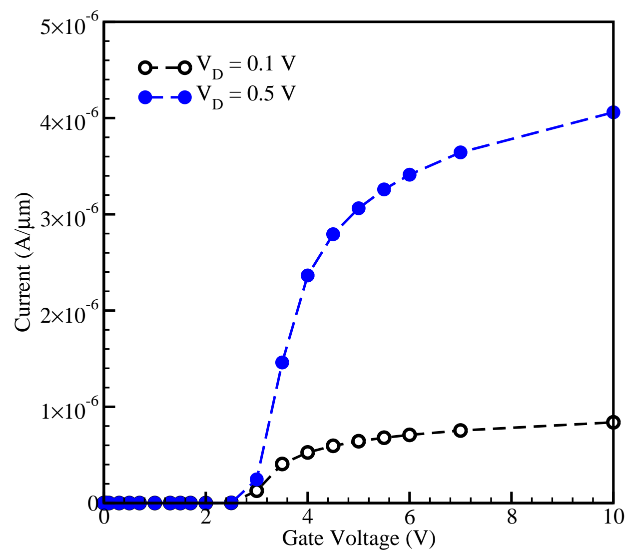

Figure 7. This figure shows the transfer characteristics of the high voltage TMOSFET for drain voltages of $0.1\mathrm{V}$ and $0.5\mathrm{V}$.

vary over several orders of magnitude within one simulation domain. Compared to the approach of using iso-lines or iso-surfaces of solutions of the Poisson equation, our method allows to propagate several fronts through the device and thus to tailor the areas of high resolution precisely and in a straightforward manner. This is, e.g., especially important for the simulation of SOI devices, where high resolution is required in the vicinity of the buried layer.

Furthermore the algorithm is robust since the generation of the final triangulation is based on edges that have to be respected (and not on single points). Finally the grids generated satisfy the Delaunay criterion and the minimum angle criterion which ensures high grid quality with respect to numeric properties.

In a real world example the constructed mesh was used to obtain the on-state and transfer characteristics of a $120\mathrm{V}$ trench gate MOSFET. The simulations of the TMOSFET show that the threshold voltage is independent of the drain voltage. The grid generated for the nontrivial geometry of this device increased the speed and accuracy of the simulations.

[1] C. Großmann and H.-G. Roos, *Numerik partieller Differentialgleichungen*. Stuttgart: B.G. Teubner, 1994.

[2] J. Sethian, "Curvature Flow and Entropy Conditions Applied to Grid Generation," *J. Comput. Phys.*, vol. 115, no. 2, pp. 440–454, 1994.

[3] T. Binder, K. Dragosits, T. Grasser, R. Klima, M. Knaipp, H. Kosina, R. Mlekus, V. Palankovski, M. Rottinger, G. Schrom, S. Selberherr, and M. Stockinger, *MINIMOS-NT User's Guide*. Institut für Mikroelektronik, 1998.

[4] D. Ueda, H. Takagi, and G. Kano, "A New Vertical Power MOSFET Structure with Extremely Low On Resistance," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 2–6, Jan. 1985.

[5] K. Shenai, "Optimized Trench MOSFET Technologies for Power Devices," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1435–1443, 1992.

[6] C. Bulucea and R. Rossen, "Trench DMOS Transistor Technology for High Current (100A Range) Switching," *Solid-State Electron.*, vol. 34, no. 5, pp. 493–507, 1991.

[7] K. Dharmawardana and G. Amaratunga, "Analytical Model for High Current Density Trench Gate MOSFET," in *Proc. of the 10th International Symposium on Power Semiconductor Devices and ICs (ISPSD 1998)*, (Kyoto, Japan), pp. 351–354, June 1998.

[8] K. Dharmawardana and G. Amaratunga, "Modeling of High Current Density Trench Gate MOSFET," *IEEE Trans. Electron Devices*, vol. 47, pp. 2420–2428, Dec. 2000.

[9] J. Sethian, *Level Set Methods and Fast Marching Methods*. Cambridge: Cambridge University Press, 1999.

[10] C. Heitzinger, J. Fugger, O. Häberlen, and S. Selberherr, "On Increasing the Accuracy of Simulations of Deposition and Etching Processes Using Radiosity and the Level Set Method," in *Proc. 32th European Solid-State Device Research Conference (ESSDERC 2002)* (G. Baccarani, E. Gnani, and M. Rudan, eds.), (Florence, Italy), pp. 347–350, University of Bologna, Sept. 2002.

[11] C. Heitzinger, J. Fugger, O. Häberlen, and S. Selberherr, "Simulation and Inverse Modeling of TEOS Deposition Processes Using a Fast Level Set Method," in *Proc. Simulation of Semiconductor Processes and Devices (SISPAD 2002)*, (Kobe, Japan), pp. 191–194, Business Center for Academic Societies, Japan, Sept. 2002.

[12] J. Shewchuk, "Triangle: Engineering a 2D Quality Mesh Generator and Delaunay Triangulator," in *Proc. First Workshop on Applied Computational Geometry*, (Philadelphia, PA, USA), pp. 124–133, May 1996.