Numerical Simulation of Selected Semiconductor Devices

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Abstract

We present a review of industrial heterostructure devices based on SiGe/Si and III-V compound semiconductors analyzed by means of numerical simulation. Critical modeling issues are addressed. Results from two-dimensional hydrodynamic analyses of Heterojunction Bipolar Transistors (HBTs) and Field-Effect Transistors (FETs) are presented in good agreement with measured data.

Introduction

Communication and information systems are subject to rapid development, where semiconductor heterostructure devices, such as Heterojunction Bipolar Transistors (HBTs) and High Electron Mobility Transistors (HEMTs), are among the fastest and most advanced high-frequency devices [1]. SiGe HBTs progressively replace III-V devices for their typical applications, such as low noise amplifiers and frequency dividers up to 99 GHz [2], and are considered essential for 40 Gb/s optical communication systems. Fig. 1 shows the rapid progress of peak-f_T of SiGe HBTs over the last couple of years. GaAs HBTs are popular devices due to their use for power amplifiers in modern cellular phone handsets. Their major advantages are the very low off-state power consumption and the high current amplification for low voltages. InP HBTs are most interesting for oscillator applications because of the low phase noise properties [3]. Due to a combination of high speed and high breakdown voltages they are suitable for high-speed digital applications up to at least 100 Gb/s [4]. Fig. 1 shows the record peak-f_T of InP HBTs over the last years. The AlGaAs/InGaAs pseudomorphic HEMTs combine superb breakdown voltages and high-speed performance. InAlAs/InGaAs/-InP HEMTs have been the fastest three-terminal devices for the last decade, as can be seen in Fig. 1.

Beside mainstream Silicon, the three-dimensional device simulator Minimos-NT [5] can deal with different complex structures and materials, such as SiGe and various III-V binary and ternary compounds, with arbitrary material composition profiles in a wide temperature range. Important physical effects, such as bandgap narrowing, anisotropic electron minority mobility in strained SiGe, carrier transport through heterointefaces, surface recombination, impact ionization, and self-heating, are taken into account.

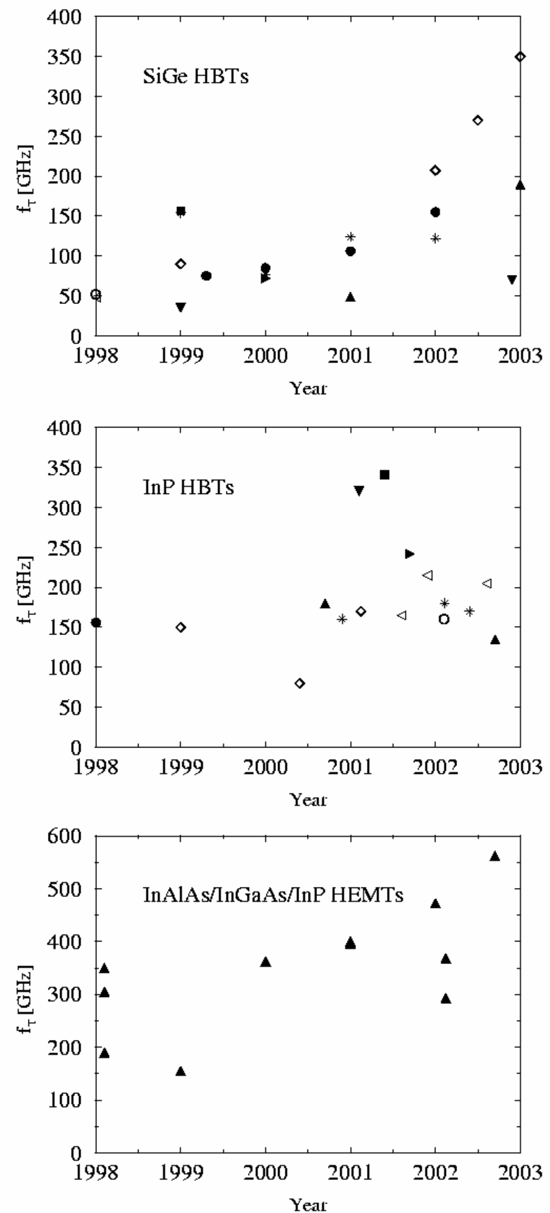

Fig. 1. Cut-off frequency f_T of some major high-speed devices over time

Selected Results of Industrially Relevant Devices

Simulations of GaAs HBTs, SiGe HBTs, InP HBTs, and InP HEMTs show good agreement both with experimental DC-results and with high-frequency data [1]. The following examples are chosen to demonstrate technologically relevant issues, which can be addressed by device simulation, such as device optimization or reliability.

Power amplifiers with InGaP/GaAs HBTs are part of many cellular phones today. Two-dimensional device simulation allows the analysis of experimental data in cases, which cannot be explained by simple analytical assumptions. This proved to be especially useful for explaining and avoiding device degradation, which occurs as a result of electro-thermal stress aging. The impact of the ledge thickness and the negative surface charges existing at the ledge/nitride interface, was studied for a one-finger 3x30 μm^2 InGaP/GaAs HBT with respect to reliability [6]. It is known that active surface states can influence significantly the current gain in bipolar devices [7]. We found a surface charge density of 10^{12} cm^{-2} appropriate to get good agreement with the measured Gummel plots at $V_{CB} = 0$ V. Based on these investigations it is possible to explain the base current degradation (see Fig. 2) of a strongly stressed device by a decrease in the effective negative surface charge density along the interface from 10^{12} cm^{-2} to $4x10^{11}$ cm^{-2} due to compensation mechanisms [8]. Fig. 3 shows simulation result for the electron current density at V_{BE}=1.2 V. Once the possible reason for device degradation is known, it is natural to search for solutions. Some ways to avoid degradation were analyzed, assuming the worst case when the negative surface charges at the ledge/nitride interface of a device with 40 nm ledge thickness are completely compensated due to stress. A possible solution is to avoid the electron leakage path in the ledge by means of electrically isolated base contacts, e.g. by introducing a nitride spacer between the ledge and the base metals. The simulation analysis shows that the depth of such a spacer is of importance. On the one hand, there is the constraint not to exceed the ledge thickness in order to avoid surface recombination in the base. On the other hand, the spacer has to have a sufficient depth to prevent the electron current. Fig. 4 shows the electron current density at V_{BE}=V_{CE}=1.2 V in a device with a distance of 10 nm between the spacer and the base layer. As can be seen in Fig. 4 a current path still exists under the spacer, if the surface charges are compensated. Unfortunately it is technologically challenging to control the exact spacer depth, which has to be about 95% of the ledge thickness in order to solve the reliability problem.

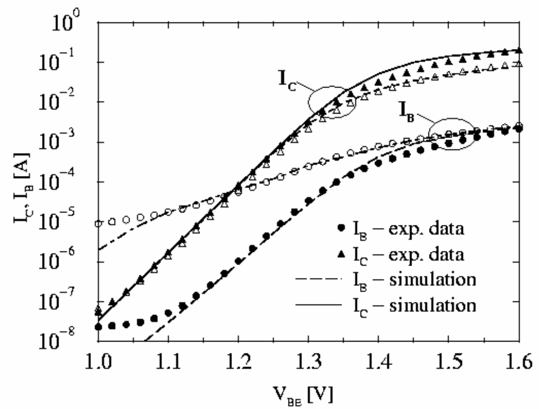

Fig. 2. Comparison of measurements (symbols) and simulation (lines) before (filled) and after (open) stress aging of InGaP/GaAs HBT.

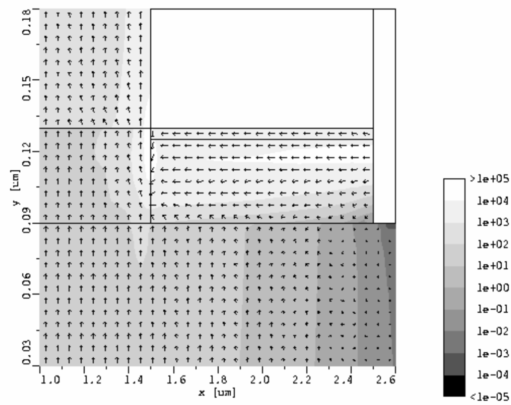

Fig. 3. Electron current density distribution [A/cm^2] at V_{BE}=V_{CE}=1.2 V: Simulation with a surface charge density of $4x10^{11}$ cm^{-2}.

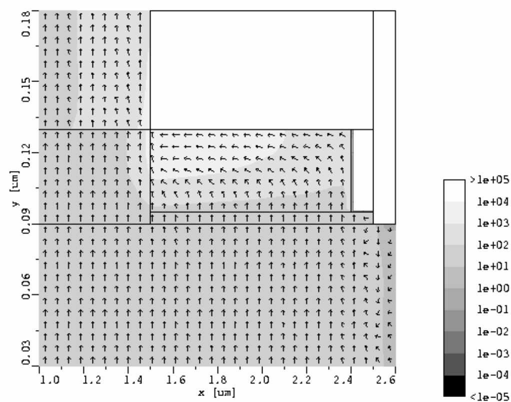

Fig. 4. Electron current density distribution [A/cm^2] at V_{BE}=V_{CE}=1.2 V: Simulation with a spacer between ledge and base contact.

Fig. 5 shows the simulated forward Gummel plots for 40 nm ledge devices with 35 nm deep spacers on the base contact side or on the emitter side of the ledge, respectively. In addition, simulation results for a device with 20 nm ledge thickness are included for comparison in Fig. 5. Measured data for a non-stressed device (symbols) is included as a reference. Note that the device with the 20 nm ledge not only has better device characteristics but also is easier to manufacture.

For HFET performance the very critical issues are process control and inverse modeling of geometrical structures. Various examples for high-power AlGaAs/InGaAs/GaAs and high-speed InAlAs/-InGaAs/InP HEMTs are demonstrated in [9]. Two factors contribute to the gate currents in pseudo-morphic GaAs HEMTs: thermionic field emission effects and impact ionization are analyzed in detail in [10], [11]. For high-speed InAlAs/InGaAs HEMTs, the precise evaluation of low voltage or low power capabilities is useful for development of high-speed optical data transmission beyond 40 Gb/s. The comparison of several lattice matched and metamorphic technologies gave consistent simulation parameters also for this material system [12]. Fig. 7 shows simulation and measurements for two different substrate temperatures for a composite channel $In_{0.52}Al_{0.48}As/In_{0.66}Ga_{0.34}As/In_{0.53}Ga_{0.47}As/InP$ HEMT for l_g=150 nm. High field effects such as impact ionization are considered. This allows the analysis of both, optimized speed and limited gate current, when scaling delta-doping and gate-to-channel separation for the requirements of 80 Gb/s operation.

The methodology for characterization and optimization of SiGe HBTs involves process calibration, device calibration employing two-dimensional device simulation, and automated Technology Computer Aided Design (TCAD) optimization. The investigated 12x0.4 μm^2 SiGe HBT structure is obtained by process simulation, which reflects real device fabrication as accurately as possible. All important physical effects are properly modeled and accounted for in the simulation in order to get good agreement with measured DC characteristics using a concise set of models and parameters. Since advanced SiGe techniques exhibit competitive performance of high-frequency devices in markets that were prior the domain of other materials, small-signal analysis by means of simulation of these devices becomes more important. Fig. 7 shows a comparison between measured and simulated S-parameters in the frequency range between 50 MHz and 31 GHz at V_{CE}=1V and current density J_C=76 kA/cm2.

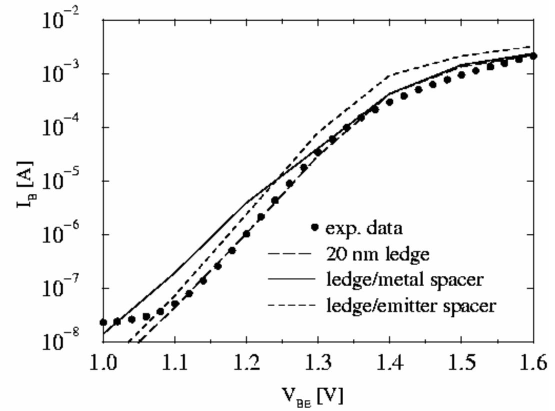

Fig. 5. Base current in a stressed device using spacer between the ledge and the base contact, and device with a thinner ledge. Data from non-stressed device is included for comparison.

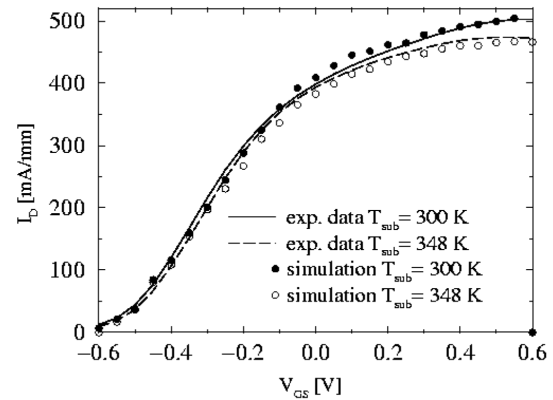

Fig. 6. Measured (symbols) and simulated (lines) transfer characteristics of InAlAs/InGaAs/InP HEMT as a function of substrate temperature at V_{DS}=0.75 V.

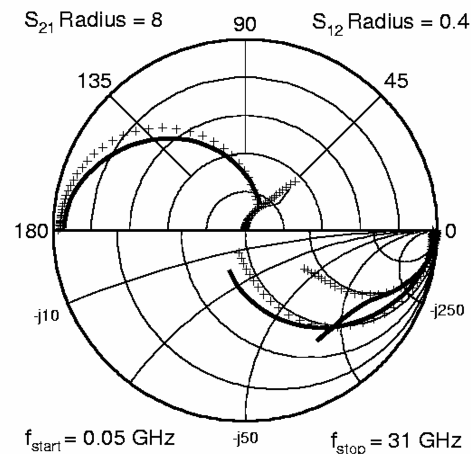

Fig. 7. Measured (symbols) and simulated (lines) S-parameters in a combined Smith-polar chart from 50 MHz to 31 GHz at V_{CE}=1V and J_C=76 kA/cm^2.

Using the models and model parameters for the InP/InGaAs/InGaAsP/InP HBT given in [1], the following study is performed. The $In_{0.53}Ga_{0.47}As$ base layer is replaced by $GaAs_{0.49}Sb_{0.51}$ which is also lattice-matched to the InP substrate, and the InGaAsP launcher is removed. Fig. 8 compares the simulated forward Gummel plots of the conventional InP/-InGaAs/InGaAsP/InP DHBT (Dev. 1) and the novel InP/GaAsSb/InP DHBT (Dev. 2). Measured data for the conventional device are included as a reference.

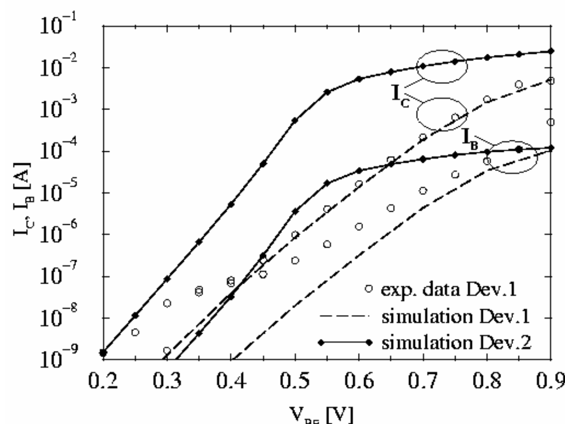

Fig. 8. Forward Gummel plot of 1x8 μm^2 InP/GaAsSb/InP double HBT in comparison to a conventional InP/InGaAs/InGaAsP/InP design.

Conclusion

A brief overview of heterostructure RF-devices based on SiGe/Si and III-V compound semiconductors has been given. GaAs HBTs, SiGe HBTs, InP HBTs, and InP HEMTs have been analyzed by means of numerical simulation. Good agreement was achieved both with experimental DC results and with high-frequency data. Technologically relevant issues, such as device optimization or reliability, have been addressed by device simulation.

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