Optimization and Inverse Modeling for TCAD Applications

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ABSTRACT

We present the capabilities and some applications for the framework SIESTA (Simulation Environment for Semiconductor Technology Analysis). This framework supports a wide range of simulators, optimizers, and strategies to optimize different properties such as speed, geometry, power, or reliability of electronic devices. We present examples for optimizing the topography of a memory cell and for extracting material parameters of a polycrystalline silicon fuse.

Keywords: optimization, inverse modeling, simulation environment, framework

1 INTRODUCTION

With the ongoing shrinking of device structures parasitic effects have to be considered in addition to the main properties of the structure. In state-of-the-art process technology nodes in the submicron regime, effects of grains boundaries, variations of geometry, or fluctuations of process parameters can cause serious problems. For instance, a device under mechanical or thermal stress due to operational conditions may change its behavior significantly.

For these reasons devices have to be designed very carefully and tested in simulation environments. The simulation framework SIESTA was developed in order to optimize device parameters and to investigate the sensitivity of the output characteristics on the input parameters.

2 SIESTA

State-of-the-art simulation environments like the framework SIESTA [1–4] support a wide range of simulators, optimizers, and optimization strategies. Contrary to commercially available software such as [5] and [6] our framework provides an open architecture for numerous types of simulators and optimizers which can be individually chosen for a particular problem. To achieve this goal this simulation environment offers modular and flexible interfaces by which external tools can be integrated with minor changes as outlined in [7].

2.1 Inverse Modeling

Fig. 1 shows an abstracted view of the internal data flow of SIESTA. The optimization procedure consists of a loop that terminates when the result has reached the required accuracy which can be determined by, e.g., the derivative of the score function. Another possible termination criterion is that a local optimum has been detected which cannot be improved any more with a gradient based optimizer [8]. For genetic or evolutionary approaches [9] the loop is terminated if the maximum number of genomes has been reached.

At start-up SIESTA generates the first parameter set based on the initial values within the user-defined constraints for each simulation branch. After applying post processing tools the simulation result is parsed in order to compare it with reference data. A score value is determined which indicates how well these two data sets match. The optimizers use this score value to generate the parameter set for the next simulation run in order to improve the score value that will be evaluated after each simulation run based on the currently generated parameter set. A typical example for the mentioned reference data are measurements with additional requirements to meet specific physical constraints, a global minimization, or a maximization condition.

2.2 Optimization Methods

SIESTA supports different optimization modes in order to achieve appropriate capabilities for a specific problem, such as the optimization for a CVD (chemical vapour deposition) process as shown in Section 4. In this example some input parameters depend implicitly on other input parameters, and, e.g., the constraints may change which can be seen for a special radiosity model [10]. Generally, an optimum with constraints for representing the physics is hard to obtain, because some of the conditions may change with a new optimization state. Another big challenge are optimizations with restrictions and boundaries for the output characteristics.

Additionally, most of the optimization algorithms used in SIESTA do not support such restrictions. Therefore, only a limited number of optimizers can be used for this specific task. Thus, the user has to carefully design the specifica-

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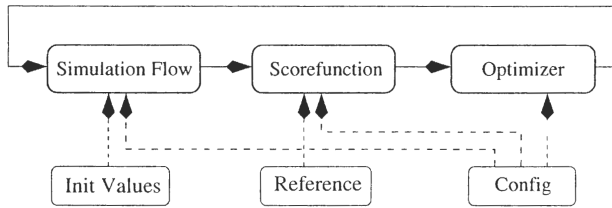

Figure 1: Overview of the internal data flow of SIESTA

tion of the problem in order to obtain a smooth behavior, otherwise the optimization could become instable and an interaction with the user is necessary.

The available optimization modes for SIESTA are called *optimization*, *calibration*, *design of experiment* (*DOE*), and *genetic*. Each of them can be set to minimization or maximization. In all these modes the score function which indicates the quality of the simulation result will be minimized or maximized, respectively.

The default mode is *optimization* which optimizes targets of single values like leakage currents of transistors and side effects like parasitic capacitances of different structures and the on-resistance of transistors. Furthermore, the power consumption, maximum temperature of a device, the maximum value of the electric field can be minimized. Additionally, also combinations of different device parameters like the gain of amplifier devices, different sorts of yield, or the ratio of capacitance per area for memory cells can be optimized.

The simulation mode *DOE* [11] is used to investigate the system behavior with only a small number of simulations. The main goal is to get output characteristic with as few simulations as possible with reasonable accuracy. Therefore, the layout (operational mode) [7] of DOE can be specified to choose the selected subspace best for the input parameters.

The *calibration* mode can be used for inverse modeling. SIESTA optimizes the parameters in order to fit specific requirements which can consist of output characteristics or constraint equations for some optimizers. Section 4 shows examples how process as well as material parameters can be extracted. These techniques can be used to search for parameter sets which best meet the requirements. This enables to predict the behavior also for new devices and structures before fabrication. Thus, valuable time can be saved and the costs of feasibility studies are reduced compared to investigations on hardware.

The *genetic* mode can be used for optimization problems even if no information about the correlation between input parameter and target value is known, for instance when the target function shows many local minima. In such a case gradient based algorithms cannot be used and a genetic algorithm is required.

3 APPLICATIONS

The open software architecture of SIESTA enables to add simulators and optimizers with only minor changes to the configuration. Thus, many software components can be easily added and combined with each other. However, the different file formats of the simulators have to be considered. Different simulations tools of vendors make it necessary to use pre- and post-processing tools to transform the currently available input format to a format readable for the next simulator. In the current stage SIESTA does not automatically check the consistency of the input parameters for the different simulators.

Interfaces to the following simulation tools exist: The three-dimensional device simulator MINIMOS-NT [12] solves the non-linear semiconductor equations together with equations which give corrections according to special effects and different materials. Furthermore, the interconnect simulator STAP from the Smart Analysis Package (SAP) [13, 14] investigates coupled electro-thermal interconnect problems including the extraction of resistances, capacitances, and inductances by means of stationary and transient simulations. The three-dimensional Finite Element Diffusion and Oxidation Simulator (FEDOS) [15] solves complex problems on diffusion and oxidation. In additional to these simulation topics also topography simulations can be included with the three-dimensional topography simulator Enhanced Level Set Applications (ELSA) [10] for the simulation of etching and deposition processes. Moreover, simulation tools from vendors are supported as well, e.g., the device simulator DESSIS [5] from ISE and the process simulator TSUPREM [16] from Synopsys. The procedure of adding new programs to the open architecture of the simulation environment SIESTA is described in detail in [7].

Additionally, licenses for all simulation tools can be set individually which are managed from SIESTA with its own license manager.

4 APPLICATION EXAMPLES

We will give a brief overview of the capabilities of SIESTA by presenting a topography optimization for a TEOS CVD process and the calibration and identification of material parameters for a polycrystalline silicon fusing structure.

4.1 Topography Optimization

The ongoing shrinking of memory devices results mainly in miniaturization of capacitances in the memory cell. The smaller the capacitor, the more devices per area can be integrated. Hence, it is very important to compare the different process parameters to see which settings meet the requirements and can operate within the proposed tolerance band.

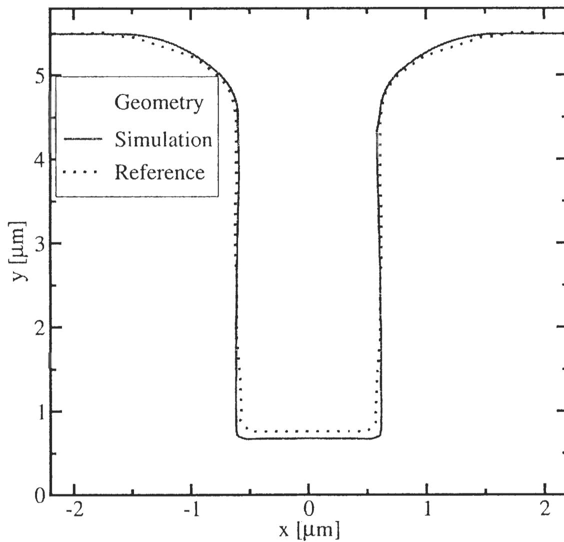

Figure 2: Comparison between measurements and the simulation results of ELSA

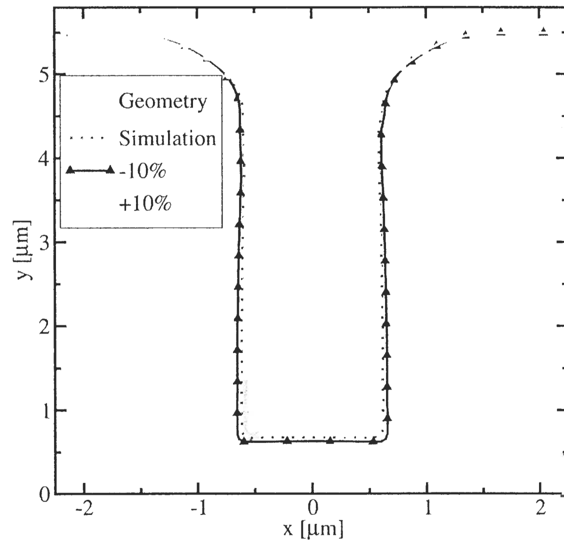

Figure 3: Results of small variation of a sticking coefficient

Fig. 2 shows an optimization result for CVD process parameters using the etching and deposition simulator ELSA. For optimization we investigated the sticking coefficients in order to obtain a good agreement with the measurements. This result allows to apply the model to future device structures. Starting from this point one can use other simulators to follow the fabrication line in order to investigate or optimize a complete series of steps for a complete device structure. Additionally, we can analyze for instance the sensitivity of the output geometry on the sticking parameters for a TEOS CVD process. Fig. 3 compares the original simulation result with the results of slightly changed input parameters. Within the range of the two solid lines we can verify that the results with the tolerance band meet the given requirements according to the internal fabrication specifications.

4.2 Parameter Extraction

With shrinking of critical dimensions small non-volatile memory cells based on fuses become a very interesting alternative in terms of production costs, area saving, and efficency. Therefore, the geometrical and thermal design becomes very important. For instance in fusing structures the electro-thermal transient behavior determines the shortening of the fuse. The faster the structure heats up the shorter is the fusing time. Therefore, a fully three-dimensional electro-thermal investigation is necessary in order to predict the material reaction. As seen in Fig. 4, the resistance shows a significant increase with time. After a certain time the resistance falls rapidly due to thermal run-away until the fuse shortens.

To improve the fusing procedure we investigate the temperature distribution during such a programming cycle in order to obtain improved designs. For these electro-thermal analyses we use the transient mode of the three-dimensional interconnect simulator STAP from the SAP package. The input parameters are measurements of the current through the device with an an applied voltage ramp. The simulator shows the resistance of the complete structure as well as the internal temperature distribution at particular time steps.

After extracting the material parameters we have varied one of the first order thermal coefficients in order to show the significance of proper calculation. The difference between the original simulation and the changed one are shown in Fig. 4. If the temperature is not calculated correctly, thermal run-away starts at a different point, which can cause serious problems. Fig. 5 shows the temperature distribution of the fusing structure at the point of highest resistance at approximately 65 μs, which can be used to analyze the heat flux.

5 CONCLUSION

We have shown a wide range of different applications for our simulation environment SIESTA. Different purposes of the simulation environment, for instance optimizations, calibrations, and DOE (design of experiments) have been used for basic investigations on device and process analysis. These optimization procedures can be performed with already existing systems and devices to verify the developed models and the currently used optimization setup. New devices, models, and systems can be automatically evaluated, optimized, calibrated, and investigated according to the specified requirements. With future simulation software we can optimize a complete process and investigate sensitivities on various process and device parameters.

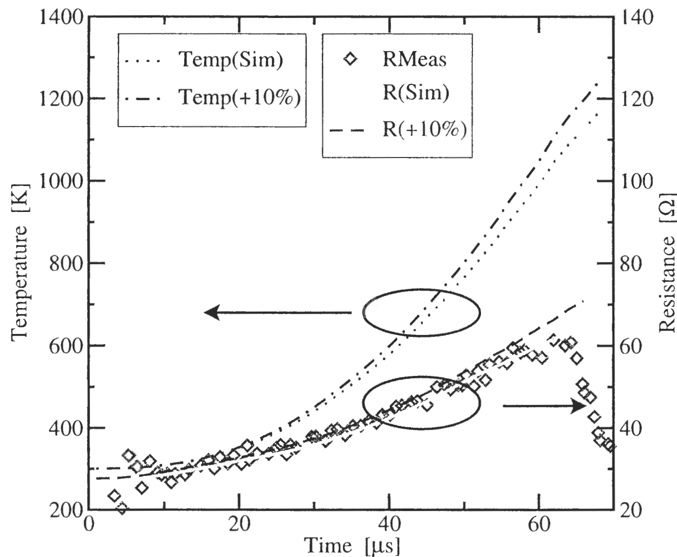

Figure 4: Small variation of a first order temperature coefficient

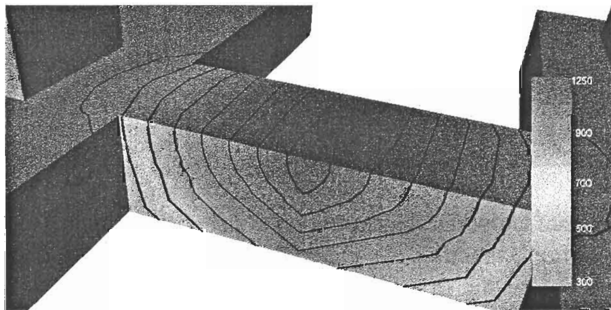
Figure 5: Temperature distribution in [K] at the point with the highest resistance

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