Optimization of Carbon Nanotube Field Effect Transistors

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ABSTRACT

The performance of Schottky barrier carbon nanotube field effect transistors (CNTFETs) depends critically on the device geometry. Asymmetric gate contacts, the drain- and source contact thickness, and nonhomogenous dielectrics above and below the nanotube influence the device operation. We use an optimizer with respect to the sub-threshold slope, high I_{on}/I_{off} ratio, and large on-currents and show that the use of a thin needle-like source contact is favorable whereas large drain contacts can decrease the off-current. The best performance improvements can be achieved using asymmetric gates centered above the source contact, where the position and length of the gate contact varies with the oxide thickness, and high-κ materials on top of the CNT and low-κ materials below the tube. We demonstrate that by geometry optimization the subthreshold slope can be reduced by a factor of two reaching a value of 100 mV/dec for devices with oxide thicknesses of 5 nm.

Keywords: nanoelectronics, carbon nanotubes, field effect transistors, optimization

1 INTRODUCTION

Semiconductor device technology using nanocarbon materials in semiconductor chip wiring is receiving accelerated development. Metallic nanotubes are a promising material for interconnects and vias in integrated circuits because of their high electrical and thermal conductivity, whereas semiconducting tubes have emerged as possible candidates for nanoscale field effect transistors (CNT-FETs).

Surprising effects regarding to the scaling of the performance of CNTFETs have been observed recently [1]. It was shown that these unexpected scaling trends can be well understood, assuming that the transistor action is caused by the modulation of Schottky barriers at the metal-nanotube contact. The barriers can be thinned by applying gate voltages sufficiently large to allow tunneling of electrons or holes.

A critical issue for CNTFET performance is the required scaling of the drain voltage V_d as the gate oxide thickness (T_{ox}) is decreased [2]. The off-current (I_{off}) rises significantly when the absolute value of the drain current is increased leading to a decrease of I_{on}/I_{off}. This effect can be understood within the Schottky band model, where the subthreshold characteristics of CNTFETs with symmetric geometries, i.e. symmetric gate, source, and drain contacts, is symmetric around the gate voltage $V_g = V_d/2$. At this point the barrier for electrons is the same as for holes and the minimum current will flow through the nanotube. The electron current rises with V_g, whereas the hole current rises with $V_d - V_g$. For a large V_d the resulting V_g may be large enough to suppress the Schottky barriers at the nanotube contacts and enable large I_{off} currents. This will occur whenever the devices are scaled to smaller size, or high-κ gate oxides increase the electric field at the metal nanotube contacts.

It was shown recently that the use of dielectrics with different κ above and below the nanotube can enhance device performance [1]. Furthermore it was demonstrated that asymmetric geometries, with gate contacts located only in the vicinity of the source contact, can enhance device performance [3]. This is due to the fact that the performance is not linked to the gate capacitance but to the change in electrostatic potential at the source and drain contact.

In this work we use an optimization setup to be able to capture the impact of all the mentioned geometry related effects on the CNTFET performance at once and to extract geometries optimized for a steep subthreshold slope $S = (\mathrm{d}\log_{10} I/\mathrm{d}V_g)^{-1}$, a high I_{on}/I_{off} ratio, and high on-currents.

2 DEVICE OPTIMIZATION

We concentrated on single-gated device geometries, comparable to conventional MOSFETs with the CNT replacing the silicon channel. We optimized the geometry (see inset of Figure 1) with respect to the following six parameters: the position and length of the gate contact (by varying L_{dg}, L_{sg}), the thickness of source and drain contact (T_s, T_d), and the permittivity of the top and bottom dielectric (ε_{top}, ε_{bottom}). We set the length of both source and
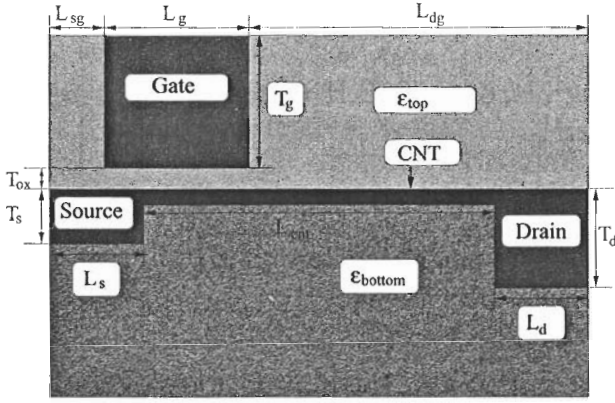
Figure 1: Device geometry with simulation parameters.

drain contacts to 10 nm, the length of the CNT to 120 nm. In our calculations the diameter of the nanotube is 1.4 nm with a band gap of 0.6 eV. We focus on mid-gap Schottky barriers, where the Fermi level of the metal contacts fall in the middle of the CNT bandgap.

2.1 Transport Modeling

Electrostatic simulations were performed using the Smart-Analysis-Package [4]. This software contains a finite element solver which uses a preconditioned conjugate gradient method to solve large linear systems in order to obtain the distributions of the potential and the electric field in the simulation domain. We neglected the charge on the nanotube which is a good approximation for the off-state and the turn-on regime [1]. The nonuniform triangular grid is refined at the metal-nanotube interface, where the Schottky barriers control the current through the tube. The resulting potential profile along the tube is used for the calculation of the transmission coefficient in a postprocessing step.

To account for coherent transport in the nanotube the Landauer-Büttiker formula was used. The drain current through the nanotube is given by an integration in the energy domain [5]

$$I_{\mathrm{d}} = \frac{4q}{h} \int [f_{\mathrm{s}}(E) - f_{\mathrm{d}}(E)] TC(E) \mathrm{d}E, \qquad (1)$$

where $f_{\mathrm{s,d}}$ are equilibrium Fermi functions at the source and drain contacts, and $TC(E)$ is the transmission coefficient. Even if $TC(E) = 1$, the resistance of the tube is given by $h/(4q^2) \approx 6.5\,\mathrm{k\Omega}$, when assuming two conduction channels in the tube. This quantum mechanical resistance stems from the difference of possible conduction channels in the tube and the macroscopic metal contact.

Accounting for an idealized CNT band structure [6] in the vicinity of the Fermi level, the transmission coefficient is estimated within the commonly used Wentzel-Kramers-Brillouin (WKB) approximation.

$$\ln TC(E) = -2 \int \frac{\mathcal{E}_{\mathrm{g}}}{\sqrt{3}a\gamma_0} \sqrt{1 - \left(\frac{E + qV(x)}{\mathcal{E}_{\mathrm{g}}/2}\right)^2} \, \mathrm{d}x \qquad (2)$$

Here $a = 0.246\,\mathrm{nm}$ denotes the lattice constant, $\mathcal{E}_{\mathrm{g}}$ is the band gap energy, $\gamma_0 = 2.5\,\mathrm{eV}$ is the transfer integral, and $V(x)$ is the electrostatic potential along the CNT. $\mathcal{E}_{\mathrm{g}}$ is related to the tube radius R via $\mathcal{E}_{\mathrm{g}} = \sqrt{3}a\gamma_0/3R$ [7]. The integration is performed within the classical turning points.

2.2 Simulation Setup

The simulation framework SIESTA provides various optimizers that can be chosen to fit best for the current problems. The optimizer used for this work is a genetic optimizer that relies on the theory of evolutionary computation and genetic algorithms. The population of the n-tuples of free parameters are chosen randomly with respect to a Gaussian normal distribution where a large set of distribution and generation parameters can be configured and tuned for special kinds of problems. Furthermore, the simulation of the population was distributed on a computer cluster to significantly decrease the optimization time.
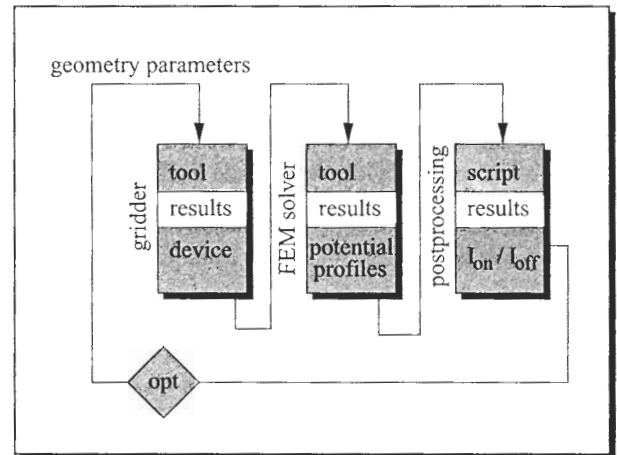

Figure 2: Diagram of the optimization tool flow.

At start time SIESTA provides the initial values of the free geometry parameters (T_{s}, T_{d}, T_{ox}, L_{sg}, L_{dg}, $\varepsilon_{\mathrm{top}}$, and $\varepsilon_{\mathrm{bottom}}$) as shown in Figure 2. These values are passed to the electrostatic solver, which calculates the potential profile for a device in the on-state and in the off-state. Afterwards a script is called, which extracts the potential along the nanotube for the two regimes and calculates I_{on} and I_{off}. The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is submitted to the optimizer which generates corresponding to the last value the next n-tuple of free parameters to improve the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio that will be evaluated after the next simulation run with the currently extracted values.

3 RESULTS

Using asymmetric structures with the gate contact located in the vicinity of the source contact, we find a clear improvement of I_{on}/I_{off} compared to symmetric geometries (see Figure 3). It can be seen that I_{on} and the subthreshold slope are hardly influenced by this geometry modification. However, if the overall gate length is reduced too much, the device can no longer be turned on by the gate, leading to a strong reduction of I_{on} and the subthreshold slope.

The performance enhancement when using different κ materials above and below the carbon nanotube can be explained from the refraction law for electric field lines at interfaces of materials with different permittivities:

$$\frac{\tan \alpha_{top}}{\varepsilon_{top}} = \frac{\tan \alpha_{bottom}}{\varepsilon_{bottom}}, \tag{3}$$

where α_{top} and α_{bottom} are the angles between the field lines and normal to the interface in the top and bottom dielectric. This law is valid within our approximation neglecting the charge on the tube and results in a lowering of the barrier when using materials with different permittivity above and below the tube. The effect is more pronounced for thick gate oxides and becomes stronger as the ratio $\delta = \varepsilon_{top}/\varepsilon_{bottom}$ is increased (see Figure 4). From the inset of Figure 4 it can be seen that the reduction of the barrier results in higher drain currents. However, for symmetric gate geometries this approach results in high I_{off} currents at large V_d and requires a proper scaling of V_d.

We demonstrated that asymmetric geometries and non-homogenous dielectrics can improve device characteristics. Next we focus on the impact of the source and drain thickness. To achieve low I_{off} it is necessary to have large barriers for both electrons and holes at the source and drain contact in the off-state. The barriers can be reduced using thin needle-like contacts which result in a high electric field at the contact. Thus large drain contacts have higher energy barrier for holes than small contacts. In Figure 5 it can be seen how the hole current is reduced for a device with $T_d = 20$ nm as compared to a device with a needle like drain contact, whereas the electron current remains unchanged. In the same manner as I_{off} can be pushed to lower values by increasing the drain thickness, I_{on} can be increased using a thinner source contact.

Finally we present the results of our device optimization for different gate oxide thicknesses (T_{ox}). In our optimization setup we fixed T_{ox} and varied the other geometry parameters in order to find optimized structures for a given T_{ox}. We found that devices with nonhomogenous dielectrics, thin source contacts, and thick drain contacts yield the best subthreshold slope (see Figure 6). The length of the gate contact leading to the optimum device performance depends on T_{ox}. It steadily decreases when reducing the gate oxide thickness. It can be seen that the subthreshold slope of the optimized geometry scales approximately as T_{ox}. For comparison in Figure 6 also the subthreshold slope of a symmetric CNTFET ($L_{dg} = L_{sg} = 5$ nm, $T_s = T_d = 10$ nm,
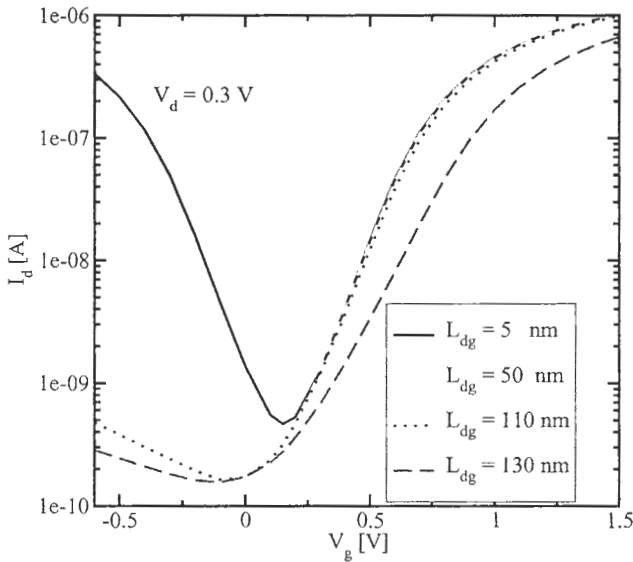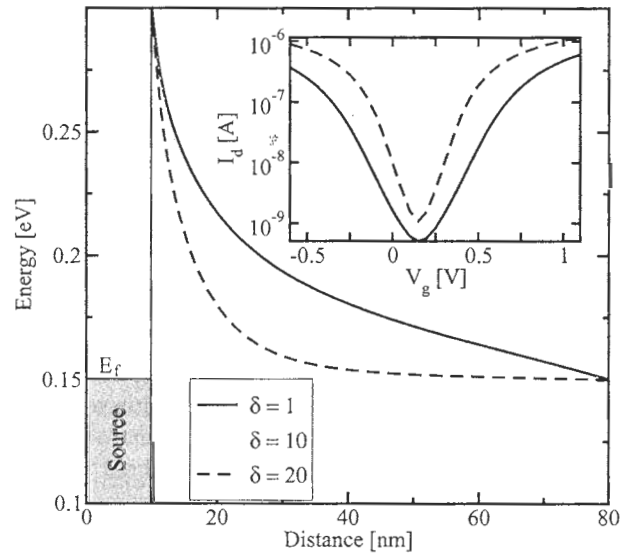
Figure 3: Subthreshold characteristics for different gate contact geometries. The solid line shows the drain current I_d for a symmetric geometry with $L_{dg} = L_{sg} = 5$ nm, whereas the other lines correspond to geometries with an increased distance between the gate and the drain contact.

Figure 4: Conduction band edge near the source contact for a device with $T_{ox} = 10$ nm, plotted for three different ratios $\delta = \varepsilon_{top}/\varepsilon_{bottom}$. For higher δ the energy barrier is thinned. The inset shows the impact of nonhomogenous dielectrics on the subthreshold characteristics at V_d=0.3 V.
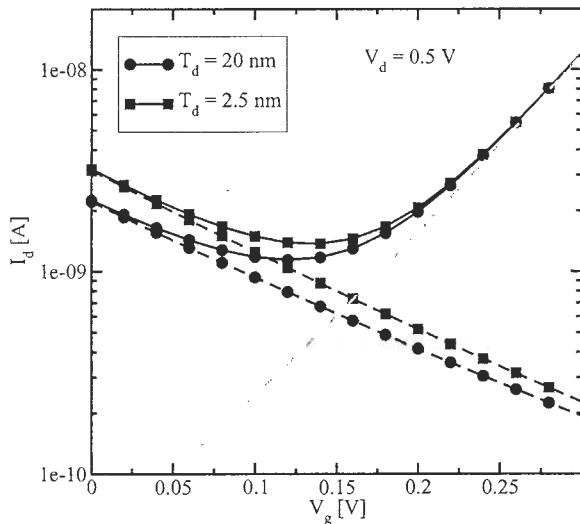
Figure 5: Drain current as a function of V_g for a drain thickness T_d of 20 nm (circles) and 2.5 nm (squares). Solid lines are used for the total current and dashed lines for the hole current which is reduced in the case of large T_d (circles). The electron current (dash-dotted line) is the same for both cases.
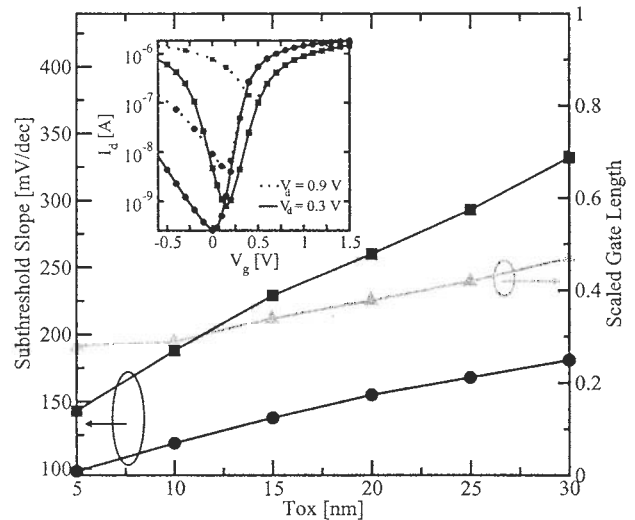

Figure 6: Subthreshold slope for optimized (circles) and conventional (squares) geometries for $V_d = 0.3$ V. The gate length leading to the optimized structures was scaled to the overall device length(triangles). The inset shows the subtreshold characteristics of a symmetric (squares) and an optimized (circles) structure at two values of V_d.

$\varepsilon_{top} = \varepsilon_{bottom} = 3.9$) is given. Beside the improvement of the subthreshold slope for asymmetric CNTFETs, the I_{on}/I_{off} ratio stays above 10^4 independently of the gate oxide thickness, whereas I_{off} rises for symmetric CNTFETs when decreasing T_{ox}. This also holds for large V_d above 0.7 V. In the inset of Figure 6 the simulated transfer characteristics for the symmetric and asymmetric structure are plotted for $V_d = 0.3$ V and 0.9 V. It can be observed that large drain voltages merely increase I_{off} while I_{on} remains almost unchanged. Hence CNTFETs should not be operated at high drain voltages.

4 CONCLUSION

The subthreshold slope can be significantly improved by optimizing a simple CNTFET structure using nonhomogeneous dielectrics above and below the tube, thin source and wide drain contacts, and an asymmetric gate contact located near the source contact. A subthreshold slope below 100 mV/dec was found for optimized geometries with $T_{ox} = 5$ nm, which is significantly closer to the thermal limit of about $k_B T \ln 10 \sim 60$ mV/dec at room temperature than previously reported values for conventional geometries [2].

In contrast to symmetric devices these structures retain a high I_{on}/I_{off} ratio above 10^4 regardless of the gate oxide thickness, whereas the I_{on}/I_{off} ratio steadily decreases with T_{ox} for symmetric devices.

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