Improving SiC lateral DMOSFET reliability under high field stress

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Abstract

We propose a new device structure for a SiC lateral DMOSFET, which improves the reliability of oxides under high field stress. A numerical simulation in order to get an insight into the physics and the characteristic of the device has been carried out. The key parameters that alter the device performance and reliability have been optimized using the device simulator MINIMOS-NT. The relationship between blocking and driving capability of our structure was closely examined. The peak surface electric field has been kept below 1.5 MV/cm at a breakdown voltage of 1460 V. Excellent transfer characteristics with significanly reduced gate bias voltage, and a fairly large advantage in terms of electrical performance and device reliability have been achieved.
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1. Introduction

The physical and electronic properties of silicon carbide (SiC) make it the foremost semiconductor material for high temperature, radiation resistant, and high-power/high-frequency electronic devices [1]. SiC-based electronic devices can operate at extremely high temperatures without suffering from intrinsic conduction effects (10-30 orders lower than Si) because of the wide energy bandgap of 3-3.3 eV and high thermal conductivity of 4.9 W/cm-K [2]. Devices formed in SiC can withstand an electric field of 2.5-3.0 MV/cm (8-10 times higher than Si) without undergoing avalanche breakdown [3]. SiC devices can operate at high frequencies (RF and microwave) because of the larger saturated electron drift velocity of 2-3 times compared to Si [4].

SiC is the only semiconductor material besides silicon on which a thermal oxide can be grown, thus enabling MOS devices. In the particular area of power devices, theoretical appraisals have indicated that SiC power MOSFETs would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly 20 times smaller than correspondingly rated Si-based devices [5]. SiC vertical DMOSFETs have been demonstrated with a specific on-resistance almost ten order of magnitude lower compared to the theoretical lower limit of Si MOSFETs of similar breakdown voltage [6].

SiC lateral DMOSFETs are attractive for monolotic integration with low voltage logic components in form of power IC; however, their design is more challenging due to the presence of a high surface field in SiC. The lack of material development and design is a major cause to most SiC lateral DMOSFETs surface problems such as step-bunching and non-uniform doping density, which leads to poor inversion layer electron mobility and oxide reliability [7].

The off-state operation is hampered by the possibility of gate oxide breakdown before avalanching occurs in SiC. According to Gauss' law, the field in the oxide is approximately 2.5 times larger than the peak field in the SiC bulk. At this field the mean-time-before-failure (MTBF) of the gate oxide can be significantly reduced.

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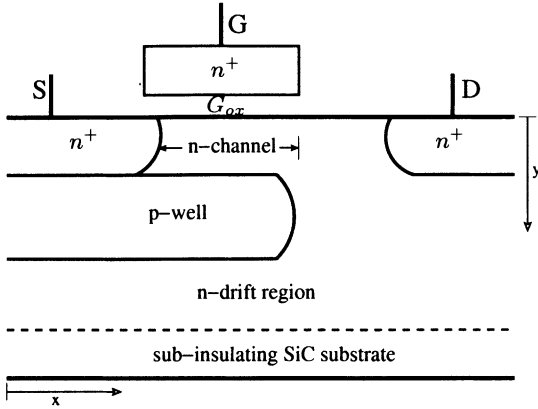*E-mail address:* Ayalew@iue.tuwien.ac.at (T. Ayalew).

Figure 1.   Schematics of the proposed SiC accumulation-mode LDMOSFET.

This raises concerns about the reliability of oxides on SiC under high field stress.

In order to minimize these problems a new design of an accumulation-mode structure for a LDMOSFET (Lateral DMOSFET) is proposed. The key parameters that alter the device performance and reliability have been optimized using the device simulator MINIMOS-NT [8]. A numerical simulation in order to get an insight into the physics and the characteristics of the device has been carried out. The relationship between blocking and driving capability was closely examined. The peak surface electric field has been kept below 1.5 MV/cm at a breakdown voltage of 1460 V. Excellent transfer characteristics with significant improvement on the reduction of the gate bias voltage, and a fairly large advantage on electrical performance and device reliability have been achieved.

2. Device Structure and Operation

The principal difference between our structure depicted in Fig. 1 and the conventional inversion-layer structure is the presence of a thin n-channel region (accumulation-layer) below the gate oxide using a buried p-well region formed by ion-implantation. The thickness, length, and n-doping of this accumulation-layer is carefully chosen so that it is completely depleted by the built-in potential of the p/n junction. This causes a potential barrier between the n+ source and the n-drift regions, resulting in a normally-off device with the entire drain voltage supported by the n-drift region. Thus it can block high forward voltages at zero gate bias with low leakage currents. When a positive gate bias is applied, an accumulation channel of electrons at the SiO_2-SiC interface is created and hence a low resistance path for the electron current flow from the source to the drain

can be achieved. This structure utilizes the buried p-well region as a shield to the influence of a high SiC bulk electric field on the gate oxide, in consequence of that improving the reliability of oxides under high field stress. The structure also offers the possibility of moving the channel away from the oxide interface, thereby removing the effect of the poor interface quality on the channel mobility.

3. Physical Models

The choice of appropriate physical models is fundamental for any comparative study that involves numerical simulation. Among the SiC polytypes commercially available, for this work 6H-SiC is preferred owing to its higher breakdown field strength [9]. A model that takes into account the mobility degradation due to surface scattering has been incorporated with [10] and implemented in our simulator MINIMOS-NT:

$$\mu_{n,p}^{\text{low}} = \mu_{n,p}^{\text{min}} + \frac{\mu_{n,p}^{T_0} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\mu}} - \mu_{n,p}^{\text{min}} \cdot (1 - M(y))}{1 + M(y) \cdot \left(\frac{N_D + N_A}{N_{n,p}^{\mu}}\right)^{\gamma_{n,p}^{\mu}}} \tag{1}$$

$$M(y) = \frac{2 \cdot \exp\left(-\left(\frac{y}{y^{\text{ref}}}\right)^2\right)}{1 + \exp\left(-2 \cdot \left(\frac{y}{y^{\text{ref}}}\right)^2\right)} \tag{2}$$

where the function $M(y)$ depends on the surface distance y, and the parameter y^{ref} describes a critical length.

At high electric field the drift velocity $v_{n,p}$ of the carriers saturates due to increasing optical phonon scattering and finally reaches the saturation velocity $v_{n,p}^{\text{sat}}$, leading to the field dependent mobility as described by [11]

$$\mu_{n,p} = \frac{\mu_{n,p}^{\text{low}}}{\left[1 + \left(\frac{\mu_{n,p}^{\text{low}} \cdot E_{\parallel}}{v_{n,p}^{\text{sat}}}\right)^{\beta_{n,p}^{\text{sat}}}\right]^{\frac{1}{\beta_{n,p}^{\text{sat}}}}} \cdot \tag{3}$$

We take the component of the electric field parallel to the electron motion as driving force. The temperature dependence of $v_{n,p}^{\text{sat}}$ has been modeled by

$$v_{n,p}^{\text{sat}} = v_0^{\text{sat}} \cdot \left(\frac{T}{T_0}\right)^{\delta_{n,p}^{\text{sat}}} \tag{4}$$

and

$$\beta_{n,p}^{\text{sat}} = \beta_0^{\text{sat}} \cdot \left(\frac{T}{T_0}\right)^{\sigma_{n,p}^{\text{sat}}} \cdot \tag{5}$$

Table 1

Model parameters used for simulating 6H-SiC.

species	$\mu_{n,p}^{T_0}$ [cm²/Vs]	$\mu_{n,p}^{min}$ [cm²/Vs]	$N_{n,p}^{\mu}$ [cm⁻³]	$\gamma_{n,p}^{\mu}$	$\delta_{n,p}^{\mu}$	$\delta_{n,p}^{sat}$	$\sigma_{n,p}^{sat}$
n	415	0.0	1.1×10^{18}	0.59	-1.8	-1	1.25
p	99	6.8	2.1×10^{19}	0.31	-1.8	-1	1.25

$v_0^{T_0}$ [cm/s]	β_0^{sat}	E_D [meV]	E_A [meV]	g_D	g_A	a_n [cm⁻¹]	b_n [V/cm]
1.9×10^7	1.7	100	200	2	4	1.66×10^6	1.27×10^7

a_p [cm⁻¹]	b_p [V/cm]	$\hbar\omega_{op}$ [meV]	τ_{n0} [s]	τ_{p0} [s]	$N_{n,p}^{SRH}$ [cm⁻³]	$\gamma_{n,p}^{SRH}$	$C_{n,p}$ [cm⁶/s]
5.18×10^6	1.4×10^7	106	1×10^{-7}	2×10^{-8}	3×10^{17}	0.3	3×10^{-29}

Several temperature-dependent Hall measurements have been reported, regarding the carrier concentration, and hence, the donor (E_D) and acceptor (E_A) energy levels in SiC. A function to describe ionized shallow donor and acceptor substitutional impurities is given by [12]

$$N_D^+ = \frac{N_D}{1 + g_D \frac{n}{N_C} \exp\left(\frac{E_D}{kT}\right)} \qquad (6)$$

$$N_A^- = \frac{N_A}{1 + g_A \frac{p}{N_V} \exp\left(\frac{E_A}{kT}\right)} . \qquad (7)$$

Because of these deep levels, the dopants are not fully ionized even at higher temperatures so that we obtain an explicit relation for the ionization degree of a single donor level in n-type material

$$\xi_D = \frac{N_D^+}{N_D} = \frac{-1 + \sqrt{1 + 4g_D \frac{N_D}{N_C} \exp\left(\frac{E_D}{kT}\right)}}{2g_D \frac{N_D}{N_C} \exp\left(\frac{E_D}{kT}\right)} \qquad (8)$$

and similarly in p-type material

$$\xi_A = \frac{N_A^-}{N_A} = \frac{-1 + \sqrt{1 + 4g_A \frac{N_A}{N_V} \exp\left(\frac{E_A}{kT}\right)}}{2g_A \frac{N_A}{N_V} \exp\left(\frac{E_A}{kT}\right)} . \qquad (9)$$

One of the most important parameters of a SiC device is its breakdown voltage. In order to obtain a clear understanding of its breakdown characteristics, it is important to have an exact knowledge of the impact ionization coefficients for SiC, which are modeled according to [13], where the dependence of the impact ionization rate on the electric field and temperature is given by

$$\alpha_{n,p} = a_{n,p}\gamma_a \exp\left(-\frac{b_{n,p}\gamma_a}{E_\parallel}\right) \qquad (10)$$

$$\gamma_a = \frac{\tanh\left(\hbar\omega_{op}/2kT_0\right)}{\tanh\left(\hbar\omega_{op}/2kT\right)} . \qquad (11)$$

In these expressions α_n and α_p are the impact ionization coefficients for electrons and holes, respectively. The factor γ_a as a function of the optical phonon energy $\hbar\omega_{op}$ expresses the temperature dependence of the phonon gas against which the carriers are accelerated.

Models which account for generation and recombination have been employed. The Shockley-Read-Hall recombination is given by

$$GR_{SRH} = \frac{n_{ie}^2 - np}{\tau_p(n + n_{ie}) + \tau_n(p + n_{ie})} \qquad (12)$$

where the life time $\tau_{n,p}$ can depend on a doping level as experimentally observed in Si technology [14] and is empirically modeled by the so-called Scharfetter relation:

$$\tau_{n,p} = \frac{\tau_{n0,p0}}{1 + \left(\frac{N_D + N_A}{N_{n,p}^{SRH}}\right)^{\gamma_{n,p}^{SRH}}} . \qquad (13)$$

Additionally, the Auger recombination rate is given by [15]

$$R_{Au} = (C_n n + C_p p)\left(np - n_{ie}^2\right) . \qquad (14)$$

Here, C_n and C_p denotes the Auger coefficient of electrons and holes, respectively.

4. Device Simulation

For device simulation we have utilized published material data listed in Table 1. Six parameters that alter the device performance and reliability have been investigated: The doping concentration of the n-drift region; the depth and the concentration of the implanted p-well; the doping concentration and the thickness of the n-channel (accumulation-layer); and the gate oxide overlap length. The p-well region has a Gaussian profile buried between 0.3 and 1.0 μm, which has to be optimized because it determines the thickness of the accumulation-layer region which in turn affects the gate oxide field, breakdown voltage, and on-resistance.

In order to achieve acceptable device reliability, the maximum field in the oxide may need to be limited. If this occurs, the high-field capability of SiC cannot be fully utilized. For the desired breakdown voltage of 1500 V, the proposed structure is optimized to have a 33 μm cell pitch, a 10 μm thick n-drift region doped at 5.0×10^{15} cm^{-3} and an n+ polysilicon gate electrode with a 50 nm thick gate oxide.

When the buried p-well depth is larger, the built-in potential is unable to fully deplete the n-channel which causes high leakage currents, resulting in the degradation of the performance and reliability of the device at high temperature. Therefore, its depth and implanted peak concentration of 0.5 μm (between $0.3 - 0.8 \mu$m) and 1.0×10^{18} cm^{-3} respectively was found to give the optimum accumulation layer thickness at which the criterion for the device optimization (figure of merit, FOM) [16] can be satisfied.

$$\left. \frac{V_{\mathrm{B}}^2}{R_{\mathrm{on,sp}}} \right|_{\mathrm{opt}} = \mu_n \epsilon_s \left(\frac{2E_{\mathrm{c}}}{3} \right)^3 \tag{15}$$

where V_{B} is the breakdown voltage, $R_{\mathrm{on,sp}}$ is the specific on resistance, E_{c} is the critical electric field, μ_n is electron mobility parallel to the c axis and ϵ_s is the SiC dielectric constant.

High breakdown voltages provide for improvements in high power device performance, but this conflicts with the need for high switching devices to have a low on-resistance. The breakdown voltage is limited by the breakdown of the gate oxide which depends on the electric field in the oxide. From Gauss' law, the field in the oxide is approximately 2.5 times greater than the peak field in the SiC. Since the peak field in SiC can be almost 10 times higher than in Si, the fields in the oxide on SiC will tend to be 10 times higher than the oxide fields in Si devices.

For durable reliability simulation results show that the accumulation layer parameters are key factors determined the peak electric field of the gate oxide re-
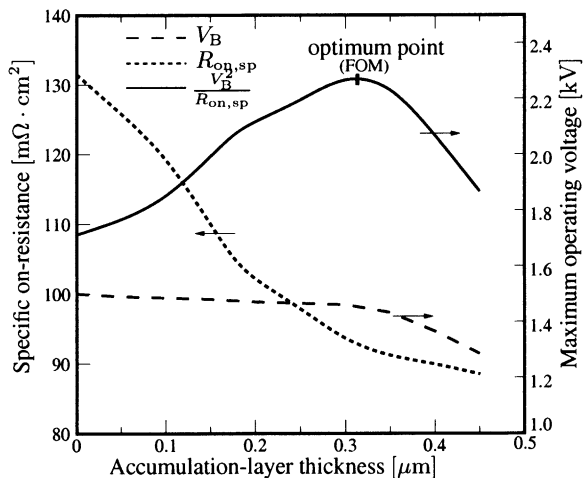

Figure 2. Effect of the accumulation layer thickness on maximum operating voltage and specific on-resistance.

main below the practical limit of 4 MV/cm while utilizing the high-field capability of SiC. Values of the accumulation layer thickness, length and concentration of 0.3 μm, 4 μm and 5.0×10^{15} cm^{-3}, respectively, have been established to achieve the desired on- and off-state characteristics. At these optimum values and room temperature, a specific on-resistance of 93.2 m$\Omega \cdot$ cm^2 and a breakdown voltage of 1460 V with the corresponding small leakage current was achieved. The effect of the accumulation layer thickness on the maximum operating voltage, specific on-resistance and criterion for the device optimization obtained by simulation is illustrated in Fig. 2.

The gate oxide overlap was varied from 4 to 7 μm, and its influence on the surface field and operating voltage was analyzed. For the desired high stress voltage operation this overlap has to be kept as small as possible in order to minimize its parasitic capacitance. Simulation predicted that a gate oxide overlap length of 6 μm is optimal.

5. Result and Discussion

The proposed accumulation-mode LDMOSFET shows a fairly large advantage in terms of electrical performance and reliability compared to its standard inversion-mode LDMOSFET counter part. Excellent I-V characteristics were obtained with good current saturation and gate control at high temperature operation of 470 K as depicted in Fig. 3.

One of the important areas of improvement for the SiC LDMOSFET device is the decrease in its conduction losses which is governed by its specific on-resistance. This on-resistance depends on the channel
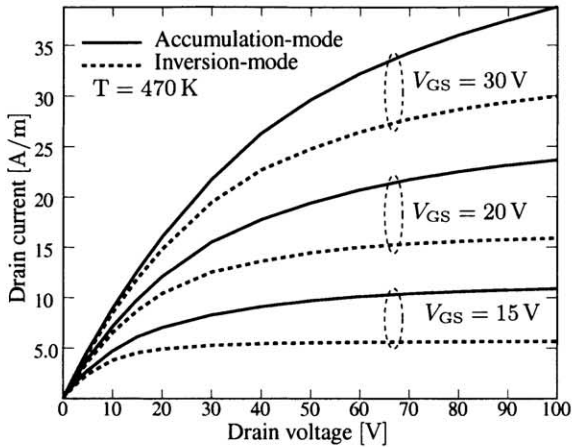
Figure 3. Comparison of on-state characteristics.

Figure 5. Effect of the accumulation-layer thickness on the electric field in the SiC substrate at 470 K.

and the n-drift resistance of the device. An estimate of the on-resistance contribution indicates that 90% of the on-resistance is due to the large channel resistance, owing to the low inversion layer mobility. The proposed structure is able to minimize this resistance and improve the mobility. A simulated accumulation layer mobility of 120 cm^2/Vs compared to the 18 cm^2/Vs for the inversion-layer was observed, which is in good agreement with experimental results extracted at a different temperature [9]. Fig. 4 shows a significant improvement on the reduction of the gate bias voltage (a logic level gate bias of 5 V). The device is normally off with a threshold voltage of only 1 V compared to that of 3 V for the inversion-mode structure.

In addition to moving the channel away from the oxide interface and removing the influence of interface quality on the channel mobility, the proposed struc-
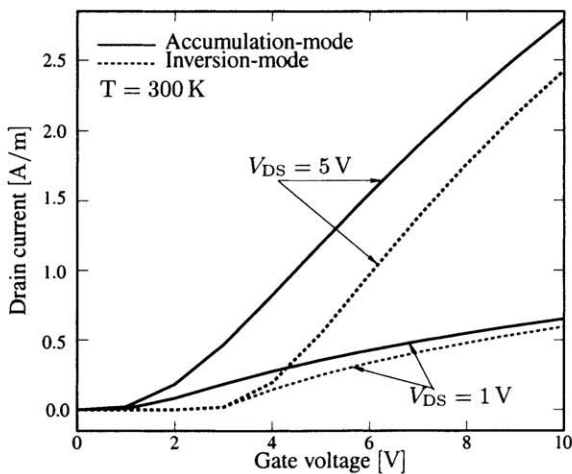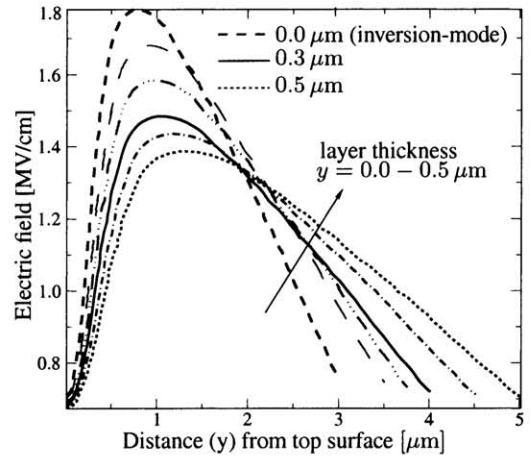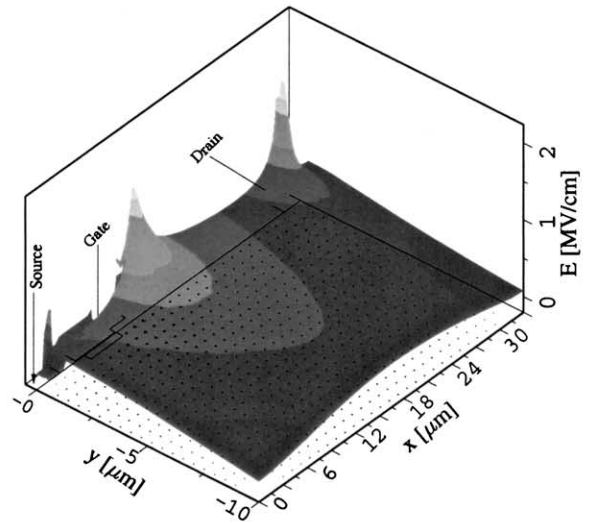

Figure 6. Profile of the electric field at the maximum operating voltage.

ture offers the possibility of serving as a shield to the influence of high SiC bulk electric field on the gate oxide. The influence of the accumulation-layer thickness on the SiC bulk electric field is illustrated in Fig. 5. The result clearly show that the proposed structure accumulation-mode n-channel thickness of 0.3 μm improves the electric field by 0.3 MV/cm compared to its inversion-mode counter part. At this optimum value and maximum operating voltage the peak surface electric field has been kept below 1.5 MV/cm as depicted in Fig. 6. That is equivalent to an oxide field of 3.75 MV/cm, and considerably lower than the practical limit of the electric field strength in the oxide. There-

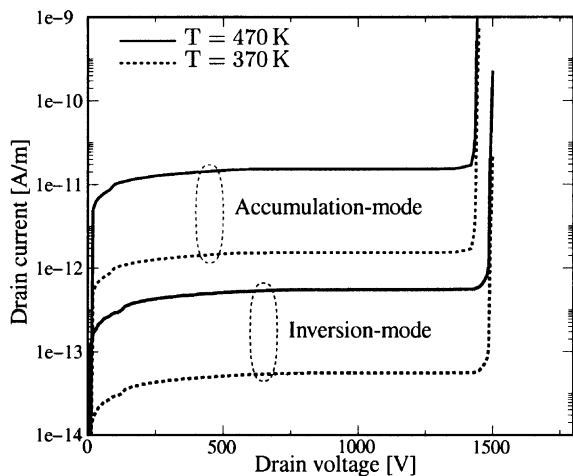
Figure 4. Comparison of transfer characteristics.

Figure 7. Comparison of off-state characteristics.

fore, the proposed structure improves the reliability of the device while utilizing the high breakdown electric field strength of SiC.

A breakdown voltage of 1460 V with a leakage current comparable to that of standard inversion-mode LD-MOSFET was achieved as shown in Fig. 7. The off-state leakage current caused by the built-in potential of the p/n junction is ten orders of magnitude less than the on-state current for the same structure, but one order of magnitude larger than the inversion-mode structure. This can effectively be suppressed by calibrating parameters which enable a fully depleted accumulation-layer. High temperature causes an increase in the leakage current due to the increased intrinsic carrier concentration.

6. Conclusion

A new device structure for a SiC lateral DMOSFET that improves the reliability of oxides under high field stress has been proposed. Key parameters that alter the device performance and reliability were optimized and analyzed. Simulation based comparisons were conducted between the proposed device and the standard structure using the same condition and parameters. It may be concluded that the new structure offers a fairly large advantage in terms of electrical performance. A satisfactory improvement on the reduction of the gate oxide peak electric field to sustain durable reliability while utilizing the high-field capability of SiC has been achieved. A significant reduction on the gate bias voltage to obtain good on-state conduction and excellent transfer characteristics were obtained with the output current increased by two fold. The device also exhibits a blocking voltage of 1460 V with an oxide field below 3.75 MV/cm which is considerably lower than the practical limit of the oxide breakdown field.

References

[1] Cree Inc., 4600 Silicon Drive Durham, NC 27703. Silicon Carbide: Physical & Electronic Properties. http://www.cree.com/Products/sic_index.html.

[2] Chow T. P., Ramungul N., Ghezzo M. Recent advances in high-voltage SiC power devices. *Proceedings of the High-Temperature Electronic Materials: Devices and Sensors Conference*, 22-27 Feb. 1998. pp.55–67.

[3] Bhatnagar M. and Baliga B. J. Comparison of 6H-SiC, 3C-SiC, and Si for Power Device. *IEEE Trans.Electron Devices* 1993;40(3):645–655.

[4] Cooper J. A., Agarwal A. SiC Power-Switching Devices-The second Electronics Revolution?. *Proc.IEEE* 2002;90(6):956–968.

[5] Baliga B. J. Power ICs in the Saddle. *IEEE Spectrum* 1995;32(7):34–40.

[6] Shenoy P. M., Baliga B. J. The Planar 6H-SiC AC-CUFET: A New High-Voltage Power MOSFET Structure. *IEEE Trans.Electron Devices* 1997;18(12):589–591.

[7] Lipkin L. A., Palmour J. W. Improved oxidation procedures for reduced SiO_2/SiC defects. *J.Electron.Mater.* 1996; 25(5):909–915.

[8] Institut für Mikroelektronik, Vienna University of Technology. *MINIMOS-NT User's Guide*, 2002.

[9] Chilukuri R. K., Shenoy P. M., Baliga B. J. High-Temperature Operation of SiC Planar ACCUFET. *IEEE Trans.Industry Applications*. 1999;35(6):1458–1462.

[10] Caughey D., Thomas R. Carrier Mobilities in Silicon Empirically Related to Doping and Field. *Proc.IEEE* 1967; 52:2192–2193.

[11] Canali C., Majni G., Minder R., Ottaviani G. Electron and hole drift velocity measurements in Silicon and their empirical relation to electric field and temperature. *IEEE Trans.Electron Devices* 1975; 22:1045–1047.

[12] Cole D. C., Johnson J. B. Accounting for Incomplete Ionization in Modeling Silicon Based Semiconductor Devices. *Proceedings of the Workshop on Low Temperature Semiconductor Electronics*, 7-8 August 1989. pp.73–77.

[13] Raghunathan R., Baliga B. J. Measurement of Electron and Hole Impact Ionization Coefficients for SiC. *Proceedings of the 9th International Symposium on Power Semiconductor Devices and IC's, ISPSD'97*, 26-29 May 1997. pp.173–176.

[14] Fossum J. G., Lee D. S. A phsical Model for the Dependence of Carrier Lifetime on Doping Density in Nondegenerate Silicon. *Journal of Solid-State Electron.* 1982;25(8):741–747.

[15] Selberherr S. *Analysis and Simulation of Semiconductor Devices*. Springer, Wien, New York, 1984.

[16] Baliga B. J. Power Semiconductor Device Figure of Merit for High-Frequency Applications. *IEEE Electron Device Lett.* 1989;10(10):455–457.