ELSEVIER

Microelectronics Journal 35 (2004) 299–304

Microelectronics Journal

www.elsevier.com/locate/mejo

High-voltage lateral trench gate SOI-LDMOSFETs

J.M. Park*, R. Klima, S. Selberherr

Institute for Microelectronics, TU Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria

Abstract

We present a lateral trench gate SOI-LDMOSFET that uses narrow trenches as channels. The lateral trench gate, which allows the channel current to flow laterally on the trench side walls, decreases its on-resistance because it increases the current spreading area of the device. The specific on-resistance (R_{sp}) strongly depends on the trench depth, which affects the channel area on the side wall of the trench and the space between the trenches affects the channel density of the device. The R_{sp} of the suggested devices as a function of the lateral trench depth and the space between the trenches are studied. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the influence of device parameters on the R_{sp} and the breakdown voltage. The improvement in the current handling capability of the suggested device is about 8.3% compared to the conventional SOI-LDMOSFET.
© 2003 Elsevier Ltd. All rights reserved.

Keywords: High-voltage devices; SOI-LDMOSFETs; Lateral trench gate; Simulation

1. Introduction

Smart power integrated circuits have become popular for automotive applications, consumer electronics, telecommunications, and industrial control. These ICs improve the reliability, reduce the volume and weight, and increase the efficiency of the system [1,2]. Considerable effort has been spent on the development of smart power devices. SOI (silicon on insulator) lateral double diffused MOS transistors (LDMOSFETs) are increasingly used as output power devices in smart power applications. Advantages of SOI technology are the superior isolation, reduced parasitic capacitances and leakage currents, and the superior high temperature performance compared to the traditional junction isolation. The isolation area of junction isolation becomes larger as the voltage rating of the device is increased. In the case of SOI devices it depends only on the fabrication process, this results in a compact chip size of high-voltage devices. These advantages allow monolithic integration of multiple power devices and low-voltage control circuitry on the same chip.

The conventional SOI-LDMOSFET has the channel regions on the surface. The channel is obtained by a double diffusion process. The maximum breakdown voltage (BV) of the conventional SOI-LDMOSFET is limited by the buried oxide thickness and SOI thickness. It has been shown that by proper choice of the n-drift doping and length, optimal on-resistance can be achieved for a given BV requirement. The trench structure is used only for the isolation of power devices and low-voltage circuitry. The main issues in the development of these devices are to obtain the best trade-off between R_{sp} and BV, and to shrink the feature size without degrading device characteristics. New structures such as buried gate oxide devices [3], LUDMOSFETs [4], super-junction [5], trench lateral power MOSFETs with a trench bottom source contact (TLPM/S) [6], multi-channel devices [7], lateral trench gate [8], and folded gate LDMOS transistors (FG-LDMOSTs) [9] are proposed to improve the performance of the conventional power devices.

LUDMOSFETs are based on the concept of the trench diode (or U-diode). The trench of the LUDMOSFETs reduces the potential crowding under the gate edge, allowing higher BV with reduced drift length. Super-junction devices such as COOLMOS [10] and MDmesh [11] assume complete charge balance in the drift region. It can be achieved by introducing alternating n and p columns in the drift region, and the doping in this region can be increased drastically. The drift doping has the inverse relationship with the width of the n and p columns. This results in significant reduction in the R_{sp} of the devices. TLPM/S has a trench bottom source contact. The source polysilicon is connected to the silicon substrate at the bottom of the trench and the channel is created on the side wall at the gate area. Because of the reduced cell pitch of the device, it allows to

* Corresponding author. Tel.: +43-1-58801-36033; fax: +43-1-58801-36099.

E-mail address: park@iue.tuwien.ac.at (J.M. Park).

0026-2692/$ - see front matter © 2003 Elsevier Ltd. All rights reserved.
doi:10.1016/S0026-2692(03)00192-7

increase the channel density per unit area. Multi-channel devices have several separated gates that are connected together. This approach leads to an improvement in the on-state performance of the device. FG-LDMOSTs are suggested to increase the channel density without consuming more chip area. These can be made by trenching the silicon surface before the gate formation, and the channel resistance is reduced by the increased channel density.

We present a lateral trench gate SOI-LDMOSFET that uses narrow trenches as channels. Contrary to the conventional vertical trench MOSFETs with current flow in vertical direction, the lateral trench gate is formed laterally on the side wall of a trench and the channel current flows in lateral direction through the trench side walls. This gives an increased channel area compared to that of conventional SOI LDMOSFETs. Even the reverse characteristics of the proposed device are similar to that of the conventional device. Using three-dimensional simulations it is possible to see the vertical and lateral electric field distribution near the gate and the lateral current spreading at the channel. We have performed such three-dimensional numerical simulations with MINIMOS-NT [12] to investigate the influence of device parameters on R_{sp} and BV.

2. Device structures and operations

Figs. 1 and 2 show the schematic structures of a conventional LDMOSFET on SOI and a proposed lateral trench gate SOI-LDMOSFET, which are used for simulation of BV and on-resistance, respectively. Generally, the BV of the conventional SOI-LDMOSFET is limited by the buried oxide thickness, SOI thickness, and the drift layer length. Most of the voltage is supported by the buried oxide layer, and the maximum electric field strength at the interface between silicon and the buried oxide is limited by that of the silicon region at the interface. To obtain a higher voltage with the thick film SOI-LDMOSFETs, the buried oxide or the SOI layer thickness must be increased.

Fig. 1 shows a view of a conventional n-channel SOI-LDMOSFET designed for a BV of 100 V with an SOI thickness t_{soi} of 1.5 μm and a buried oxide thickness t_{ox} of 1.0 μm. The drift region of the device is doped according to the reduced surface field (RESURF) principle [13,14].

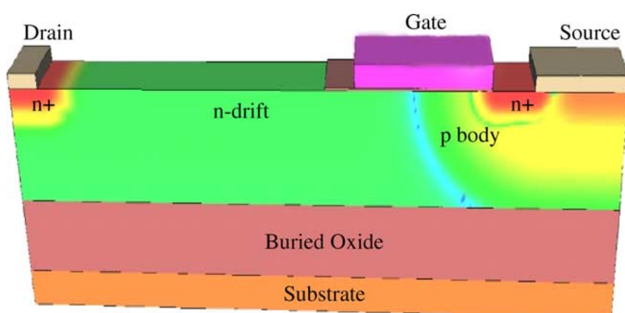

Fig. 1. Conventional LDMOSFET on SOI.

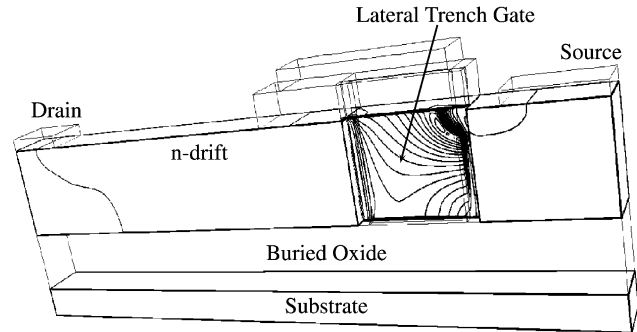

Fig. 2. Proposed lateral trench gate SOI-LDMOSFET and current flow iso-lines at $V_{GS} = 12$ V and $V_{DS} = 2.0$ V. Channel current flows on the side wall of the trench.

To obtain a better trade-off between BV and on-resistance a highly doped n^+ buffer is added at the drain. The on-resistance of the low and medium voltage devices is determined by the drift and channel resistance. To achieve a lower on-resistance, the drift doping or the channel area must be increased. The drift doping, however, is limited by the RESURF condition, and the channel area affects the chip size.

Fig. 2 shows the proposed lateral trench gate SOI-LDMOSFET and current flow iso-lines at $V_{GS} = 12$ V and $V_{DS} = 2.0$ V. As shown in the figure, the proposed device structure has a similar structure as that of a conventional SOI-LDMOSFET except that it has a trench gate on the side wall. Together with the channel on the top of the SOI this gives an increased channel area, and an effective n-drift area (near the gate edge) that contributes to the current conduction during on-state is increased. From Fig. 2 it is clear that the channel current flows on the side wall of the trench. With the increased channel area and the effective n-drift area the reduction of the on-resistance can be achieved. The trench depth determines the channel area, and the space between the trenches determines the channel density of the device. The width, space, and depth of the lateral trench gate are 0.4 μm, from 0.5 to 1.1 μm, and from 0.5 to 1.5 μm, respectively. Simulations are performed for the 100 V lateral trench gate SOI-LDMOSFETs with an n-drift length $L_d = 5.5$ μm and doping $N_D = 1.0 \times 10^{16}$ cm^{-3}. The other structure parameters are the same as that in Fig. 1. Table 1

Table 1
The technological and geometrical parameters considered for device simulations

Parameter	Value
n-Drift doping N_D, cm^{-3}	1.0×10^{16}
n-Drift length L_d, μm	5.5
SOI thickness t_{soi}, μm	1.5
n-substrate doping, cm^{-3}	5.0×10^{18}
Buried oxide thickness t_{ox}, μm	1.0
Lateral trench gate width, μm	0.4
Lateral trench gate space, μm	0.5–1.1
Lateral trench gate depth, μm	0.5–1.5

shows the technological and geometrical parameters considered for device simulations.

3. Simulation results and discussion

Reducing the on-resistance while maintaining a desired BV rating has been the main issue in the development of lateral power devices. The on-resistance of high-voltage SOI-LDMOSFETs strongly depends on the doping of the drift layer. In order to increase the BV of the RESURF devices the doping of the drift layer must be reduced and the drift layer length increased. R_{sp} and BV are inversely related to each other. In the conventional SOI-LDMOSFET, the buried oxide supports a large voltage, and it prevents potential lines from spreading into the substrate. Almost all the voltage is supported by the buried oxide layer. The maximum electric field strength of buried oxide is determined by the electric field strength of silicon at the interface between the silicon and the buried oxide. To achieve a higher BV, the surface electric field must be reduced by optimizing the drift length and doping. Fig. 3 shows the potential distribution of the perfectly resurfed lateral trench gate SOI-LDMOSFET at a drain-source voltage $V_{DS} = 110$ V. The equipotentials are uniformly spaced along the surface of the drift region and the dense potential distribution can be seen at the buried oxide layer. It exhibits a similar potential distribution as that of the conventional device; the lateral trench does not affect the RESURF condition. With the same BV as the conventional device it helps to decrease the on-resistance by increasing the current spreading area at the channel region. Three-dimensional numerical simulations with MINIMOS-NT have been performed to investigate the BV, R_{sp}, and self-heating effects as a function of the lateral trench depth, and the space between the trenches.

3.1. Off-state characteristics and self-heating

Fig. 4 shows the electric field of the conventional SOI LDMOSFET at $V_{DS} = 110$ V, the peak electric fields can be seen at the drain, the field plate, and the gate edge near the surface of the SOI. A polyfield plate at the gate is employed for reducing the surface electric field near the gate edge. Fig. 5 shows the electric field of the lateral trench gate SOI-LDMOSFET at $V_{DS} = 110$ V. Contrary to the conventional RESURF SOI-LDMOSFETs, additional higher electric field can be seen at the middle of the lateral trench gate end. With the n^+ buffer at the drain, the position of the electric field is moved towards the extended drain edge (Fig. 6). Fig. 6 shows the electric field distribution in the lateral trench gate SOI-LDMOSFET along the lateral cross-section of the surface and the middle of the SOI. The peak electric field can be seen clearly at the middle of the lateral trench gate end. This additional peak helps to decrease the electric field near the gate edge on the top of the SOI and increase the depletion area of the device. As a result the BV and leakage current of the proposed device are simultaneously increased compared to the conventional device with

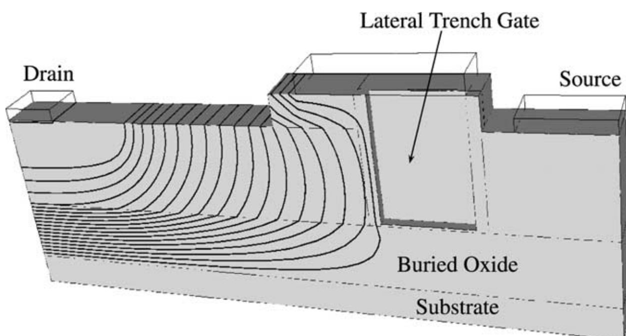

Fig. 3. Potential distribution of a lateral trench gate SOI-LDMOSFET at $V_{DS} = 110$ V.

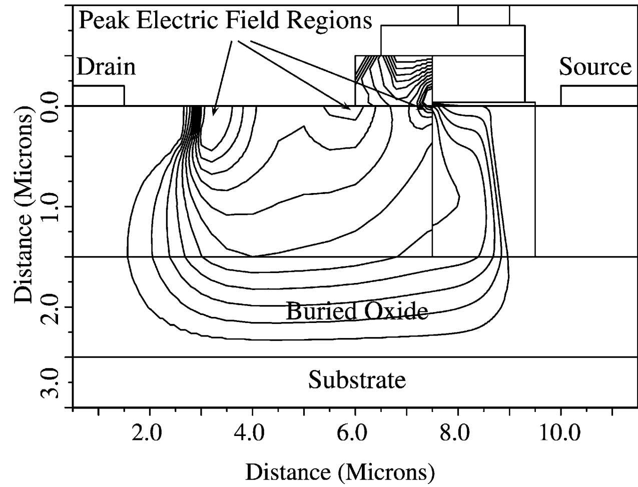

Fig. 4. Constant electric field lines of the conventional SOI-LDMOSFET at $V_{DS} = 110$ V. A higher electric field can be seen at the drain and gate edge near the surface of the SOI.

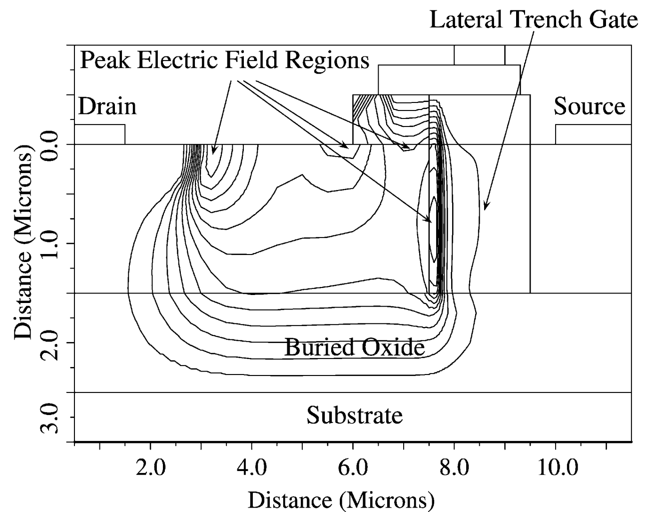

Fig. 5. Constant electric field lines of the lateral trench gate SOI-LDMOSFET at $V_{DS} = 110$ V. A higher electric field can be seen at the drain edge and middle of the lateral trench gate (Fig. 6).

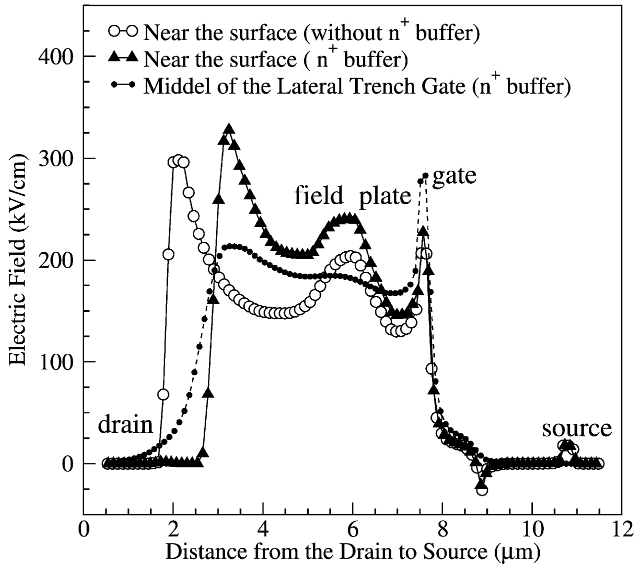

Fig. 6. Electric field distribution in the lateral trench gate SOI-LDMOSFET along the lateral cross-section of the surface and the middle of the SOI.

the same structure parameters. With the n-drift width of 5.5 μm the maximum BV of the lateral trench gate structure is 117 V with $N_D = 1.0 \times 10^{16}\ \mathrm{cm}^{-3}$. The BV of the conventional SOI-LDMOSFET is 112 V with the same doping and structure parameters.

Fig. 7 shows the leakage currents of the lateral trench gate SOI-LDMOSFETs versus drain voltage as a function of the lattice temperature up to 573 K. Because of the increased depletion the leakage current of the proposed structure is larger than that of the conventional device at room temperature. The leakage current increases nearly exponentially with increasing temperature [15], because the space charge generation rate follows the intrinsic carrier density n_i. As shown in the figure, the shape of the leakage current does not change significantly with temperature, but the BV increases. The increase of BV is caused by the reduction of the mean free path of the carriers due to lattice scattering, requiring higher field for the carriers to initiate impact ionization. Generally, there are two components—a space charge generation current and a diffusion leakage current—responsible for the leakage current under reverse bias conditions. The space charge generation current is a function of a depletion layer width, an intrinsic carrier density, and a space charge generation lifetime; it increases with increasing reverse bias. The diffusion leakage current is determined by the minority carrier generation at the depletion boundaries. It decreases with increasing the doping concentration and strongly depends on the temperature.

The temperature distribution inside a device due to self-heating is determined by the heat generation profile and the thermal conduction inside the SOI-LDMOSFETs. In majority carrier devices such as MOSFETs, there is very little carrier recombination and as a result heat generation is mainly caused by Joule heating. It is proportional to the local resistances of the n-drift and channel region. However, the channel resistance of the high-voltage devices (generally over 100 V) is not dominant in the on-resistance. Fig. 8 shows the temperature distributions near the SOI surface of the conventional and lateral trench gate SOI-LDMOSFETs with an applied gate voltage $V_{GS} = 12$ V and a drain-source voltage $V_{DS} = 2$ V. The bottom of the devices is assumed to be isothermal at 300 K. Because of the dominant heat generation at the n-drift region (from 2.5 to 8 m of the figure), the temperature rise is highest near the center of

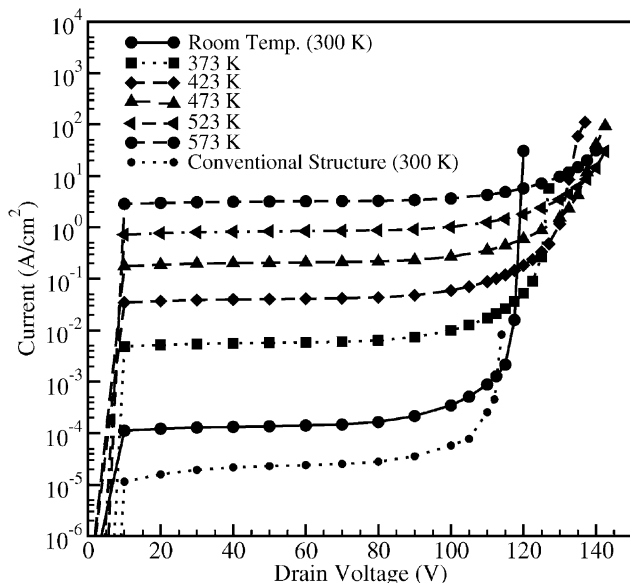

Fig. 7. BV versus lattice temperature of the lateral trench gate SOI-LDMOSFET.

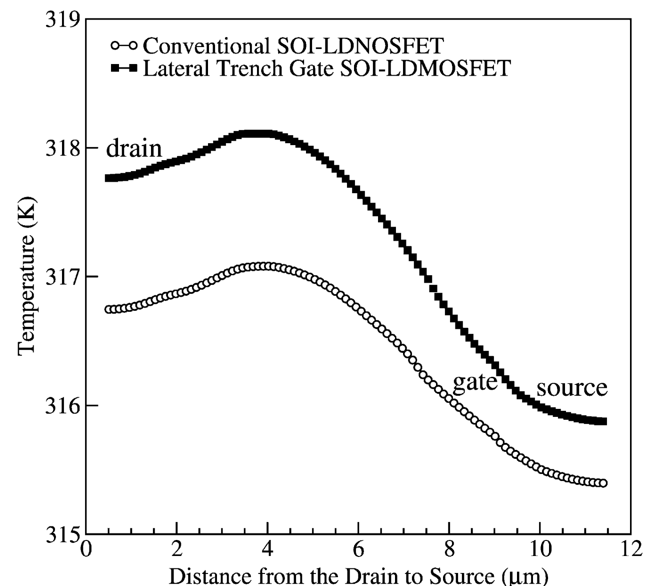

Fig. 8. Comparison of the temperature increase by self-heating between the conventional and lateral trench gate SOI-LDMOSFET near the surface of the SOI.

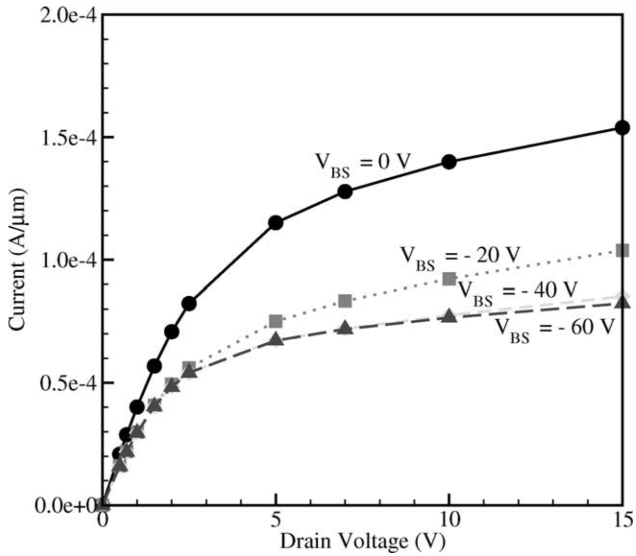

Fig. 9. On-state characteristics of the lateral trench gate SOI-LDMOSFET at $V_{GS} = 12$ V and $V_{BS} = 0, -20, -40, -60$ V.

the n-drift region, and decreases largely towards source and slightly towards drain. The increased conduction area near the gate compared to that near the drain (Fig. 10) causes further decrease of the temperature towards source. Because of the lower on-resistance (by increasing the current) of the lateral trench gate structure, a higher temperature is obtained at the n-drift region of the lateral trench gate SOI-LDMOSFET.

3.2. On-state characteristics

The on-state characteristics of the lateral trench gate SOI-LDMOSFET have been simulated with a negative back-gate bias. The drain current at the quasi-saturation region is determined by the current conduction in the n-drift region. Increased negative back-gate bias causes the reduction of the conduction area at the drift region.

As can be seen in Fig. 9, the threshold back-gate voltage exists at the back-gate bias $V_{BS} = -40$ V. If the back-gate bias is more negative than this value, the hole inversion can be seen on the top of the buried oxide. The drain current remains almost constant below the threshold back-gate bias. This effect is similar to that of the conventional high-voltage SOI-LDMOSFET [16]. For a back-gate bias of 0 V, most of the n-drift region conducts current (Fig. 10). With a negative back-gate bias, the depletion edge moves upwards (Fig. 11), and the drain current is reduced.

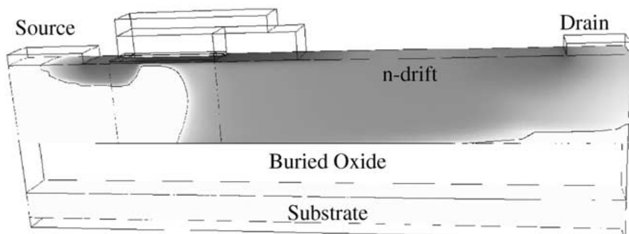

Fig. 10. Electron density of the lateral trench gate SOI-LDMOSFET at $V_{GS} = 12$ V, $V_{DS} = 10$ V, and $V_{BS} = 0$ V. The dark area shows the high electron density.

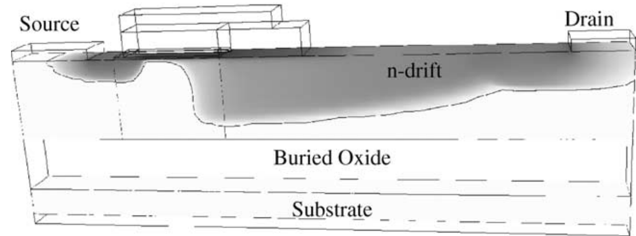

Fig. 11. Electron density of the lateral trench gate SOI-LDMOSFET at $V_{GS} = 12$ V, $V_{DS} = 10$ V, and $V_{BS} = -60$ V. Suppressed electron density (reduced dark area compared to Fig. 10) can be seen by the negative substrate bias.

Fig. 12 and Table 2 show the comparison of the on-state characteristics of a conventional and a lateral trench gate SOI LDMOSFET. From this figure it becomes clear that the lateral trench gate SOI-LDMOSFET has enhanced current handling capability. The R_{sp} rapidly decreases with increase in trench depth, but it weakly depends on the space between the trenches. With a trench depth of 0.5 μm and a space between the trenches of 0.5 μm the R_{sp} has a similar value as that of a conventional device. With a trench depth of 1.5 μm the R_{sp} of the device is 264 mΩ mm^{-2} at $V_{GS} = 12$ V and $V_{DS} = 0.5$ V. Even for the devices with a BV over 100 V, the contribution of the n-drift resistance is dominant in the on-resistance. A further reduction of the on-resistance is achieved by increasing the channel area with the proposed device. The on-resistance of the proposed device is about 8.3% smaller than the corresponding R_{sp} value of the conventional SOI-LDMOSFET (about 288 mΩ mm^{-2}).

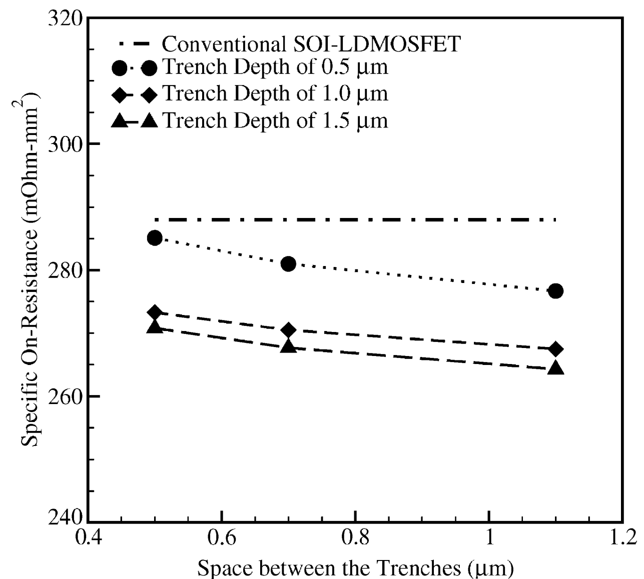

Fig. 12. Specific on-resistance of the conventional and the lateral trench gate SOI-LDMOSFETs at $V_{GS} = 12$ V and $V_{DS} = 0.5$ V.

Table 2
DC performance comparison between the conventional and the lateral trench gate SOI-LDMOSFET

	Conventional LDMOSFET on SOI	Lateral trench gate SOI-LDMOSFET
N_D, cm^{-3}	1.0×10^{16}	1.0×10^{16}
L_d, μm	5.5	5.5
R_{sp}, mΩ mm^{-2}	288	264
BV, V	112	117

4. Conclusions

A lateral trench gate LDMOSFET transistor on SOI is proposed. This allows obtaining an increased channel area of the device. The channel current flows on the side wall of the lateral trench gate can be seen clearly with the three-dimensional simulations. A lower specific on-resistance is obtained in the suggested structure compared to that of a conventional SOI-LDMOSFET. With a lateral trench gate our three-dimensional simulations confirm that it is possible to get the best trade-off between the BV and R_{sp} of the LDMOSFET on SOI. The specific on-resistance strongly depends on the trench depth. It decreases with increasing the trench depth. The space between the trenches weakly affects the on-resistance. Simulations are performed for the 100 V lateral trench gate SOI-LDMOSFETs with an n-drift length $L_d = 5.5$ μm and a doping $N_D = 10 \times 10^{16}$ cm^{-3}. With a lateral trench depth of 1.5 μm a lower R_{sp} of 264 mΩ mm^{-2} is obtained. This is about 8.3% smaller than the corresponding R_{sp} value of the conventional SOI-LDMOSFET.

References

[1] B. Murari, F. Bertotti, G.A. Vignola, Smart Power ICs, Springer, Germany, 1996.

[2] A. Nakagawa, Recent Advances in High Voltage SOI Technology for Motor Control and Automotive Application, Proceedings of International on Bipolar/BiCMOS Circuits and Technology Meeting, 1996, pp. 69–72.

[3] T. Uesugi, M. Kodama, S. Kawaji, K. Nakashima, Y. Murase, E. Hayashi, Y. Mitsushima, H. Tadano, New 3-D Lateral Power MOSFETs with Ultra Low On-Resistance, Proceedings of 10th International Symposium on Power Semiconductor Devices & ICs, 1998, pp. 57–60.

[4] M. Zitouni, F. Morancho, P. Rossel, H. Tranduc, J. Buxo, I. Pages, A New Concept for the Lateral DMOS Transistor for Smart Power IC's, Proceedings of 11th International Symposium on Power Semiconductor Devices & ICs, 1999, pp. 73–76.

[5] T. Fujihira, Y. Miyasaka, Simulated Superior Performances of Semiconductor Super-Junction Devices, Proceedings of 10th International Symposium on Power Semiconductor Devices & ICs, 1998, pp. 423–426.

[6] N. Fujishima, A. Sugi, T. Suzuki, S. Kajiwara, K. Matsubara, Y. Nagayasu, C.A.T. Salama, A High Density, Low On-resistance, Trench Lateral Power MOSFET with a Trench Bottom Source Contact, Proceedings of 13th International Symposium on Power Semiconductor Devices & ICs, 2001, pp. 143–146.

[7] Z. Qin, E.M. Sankara Narayanan, A Novel Multi-Channel Approach to Improve LIGBT Performance, Proceedings of Ninth International Symposium on Power Semiconductor Devices & ICs, 1997, pp. 313–316.

[8] Y. Kawaguchi, T. Sano, A. Nakagawa, 20 V and 8 V Lateral Trench Gate Power MOS-FETs with Record-Low On-resistance, Proceedings of International Electron Devices Meeting, Technical Digest, 1999, pp. 197–200.

[9] Y. Zhu, Y.C. Liang, S. Xu, P.D. Foo, J.K.O. Sin, Folded Gate LDMOS Transistor with Low On-Resistance and High Transconductance, IEEE Trans. Electron Devices 48 (12) (2001) 2917–2928.

[10] L. Lorenz, M. März, G. Deboy, COOLMOS—An Important Milestone Towards a New Power MOSFET Generation, Proceedings of Power Conversion, 1998, pp. 151–160.

[11] M. Saggio, D. Fagone, S. Musumeci, MDmesh™: Innovative Technology for High Voltage PowerMOSFETs, Proceedings of 12th International Symposium on Power Semiconductor Devices & ICs, 2000, pp. 65–68.

[12] Institute for Microelectronics, MINIMOS-NT 2.0 User's Guide, http://www.iue.tuwien.ac.at/software/minimos-nt, 2002.

[13] A.W. Ludikhuize, A Review of RESURF Technology, Proceedings of 12th International Symposium on Power Semiconductor Devices & ICs, 2000, pp. 11–18.

[14] E. Arnold, Silicon-on-insulator devices for high voltage and power IC applications, J. Electrochem. Soc. 141 (7) (1994) 1983–1988.

[15] Y.K. Leung, Y. Suzuki, K.E. Goodson, S.S. Wong, Self-heating Effect in Lateral DMOS on SOI, Proceedings of Seventh International Symposium on Power Semiconductor Devices & ICs, 1995, pp. 138–140.

[16] C.M. Liu, J.B. Kuo, Back Gate Bias Dependent Quasi-Saturation in a High-Voltage SOI MOSFET: 2D Analysis and Closed-form Analysis Model, Proceedings on IEEE Internal SOI Conference, 1994, pp. 25–26.