Device Simulation Demands of Upcoming Microelectronic Devices

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Numerical device simulation plays a vital role in the development of advanced integrated devices. Technology CAD device simulators currently employ current transport models which are semi-classical in nature, extended by quantum correction models and tunneling models. Semi-classical transport in semiconductor devices is well understood, especially through the availability of Monte Carlo simulation tools which deliver an accurate solution of the Boltzmann equation, allowing the rigorous treatment of band structure effects and scattering mechanisms [1].
Nevertheless, research on semi-classical transport models is still needed for several reasons. Since the Monte Carlo method still demands too much computation time for Technology CAD purposes, computationally more efficient transport models must be developed. A promising approach is to continue the well accepted moment-based transport model hierarchy currently employed in TCAD. State of the art are the drift-diffusion model, based on two moments of the Boltzmann equation, and the energy transport model, based on four moments. Six moments transport models are presently investigated, which, while computationally still efficient, provide additional information on the shape of the distribution function allowing an improved description of hot carrier effects, such as avalanche generation, hot carrier induced gate currents, hot-carrier diffusion in the SOI floating body, and non-local effects in the deca-nanometer regime [2].
Furthermore, there is a lack of mobility models for strained semiconductors. Especially the hole mobility under general strain conditions can only be predicted by Monte Carlo calculations and still needs to be cast into TCAD ready, analytical mobility models.
The semi-classical transport models have to be augmented by tunneling models [3]. Tunneling currents are exploited in non-volatile memory cells such as EEPROM and Flash devices to transfer charge to and from a floating gate electrode. Parasitic tunneling currents through very thin gate dielectrics cause increased power consumption of deca-nanometer CMOS circuits.
As potential alternative to conventional CMOS FETs, the concept of the carbon nanotube FET is currently widely investigated. Transistor action is achieved by varying the resistance of Schottky contacts rather than the channel conductance. These devices require careful modeling of the tunneling current through the Schottky barrier and in many cases a three-dimensional analysis of the electrostatic potential distribution [4].
Microelectronic devices contain large reservoirs with strong carrier scattering, and small active regions where quantum effect are important or even dominate. This explains the general interest to incorporate both semi-classical and quantum mechanical approaches in TCAD device simulators. The Wigner equation can handle both regimes and is often used to derive quantum-corrected models such as the Density-Gradient model. Various research efforts are currently directed on numerical solution methods for the Wigner equation, such as the spherical harmonics expansion method and the Monte Carlo method [5].

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