

MESHING ASPECTS ON THREE-DIMENSIONAL FIN-FET DEVICE SIMULATIONS

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Abstract

Three-dimensional semiconductor device simulation has become more and more important over the last couple of years. The generation of suitable grids for such simulations is, unfortunately from a technology point of view, still something of an art, as well as a science. In this work we have a close look at two common meshing technics, namely octree-based cuboid and tetrahedra based meshes. These two approaches are compared for their device simulation suitability on a most promising three-dimensional device – the FINFET.

Introduction

As the feature size of semiconductor devices becomes smaller and smaller, three-dimensional effects get more pronounced, and three-dimensional device geometries noticeably influence the electrical characteristics of the devices. Multi-gate MOSFETs have been considered the most attractive devices to achieve channel lengths smaller than 20nm. Recently, several structures have been proposed such as delta structures [1] which use a thin vertical silicon membrane or gate-all-around structures [2] whereby a silicon fin is completely surrounded by a ring-shaped gate. The alignment of the gates to each other and to the implanted doping profiles is very crucial for the device performance and constitutes one of the key issues for multi-gate device manufacturing. Therefore, self-aligned processes have been introduced, where the FINFET concept is one of the most promising. FINFET devices with gate lengths down to 18nm and a gate oxide thickness of 2.5nm have been tested experimentally. Moreover, three-dimensional simulations are mandatory to gain additional insight in the operation of real three-dimensional structures.

Three-dimensional simulation poses several difficulties, one of the main issues is the computational effort. The use of appropriate numerical solvers is mandatory to obtain accurate results within affordable simulation time. Even the definition of geometries is difficult due to the lack of adequate software tools. The numerical results strongly depend on the quality of the grid. For three-dimensional simulations high quality grid generation is even more important than in the two-dimensional case, because adjustment by hand becomes rather tedious.

We compare two major grid approaches for three dimensional device simulations, octree based grids where the elementary element is a cuboid and unstructured

tetrahedra based grids. Our results are gained on the three-dimensional device simulation with MINIMOS-NT [3] of a FINFET structure according to an experimentally tested device [4, 5].

Grid Generation Aspects

Creating a grid for a specific application is highly dependent on several factors which include details and features of the configuration to be analyzed, the grid generation and solver codes to be used, and the type of grids being generated, i.e., structured, overset, or unstructured. Grid generation is also subject to management issues such as schedule, budget, and resource allocation.

Structured vs. Unstructured Grids

The simplest grid type is a tensor-product grid which consists of three one-dimensional grids. All grid elements are boxes. The advantages of this kind of grid are the simple implementation of grid generators and efficient data-management and algorithms. Orthogonal grids enabled to refine grids easily. The disadvantages are the arbitrary shaped geometries and directions which cannot be resolved and the large amount of grid points appearing.

On the other extreme are completely unstructured tetrahedral based meshes. The basic difference between structured and unstructured grids lies in the form of the data structure which most appropriately describes the grid. In the two-dimensional case a structured grid of quadrilaterals consists of a set of coordinates and connectivities that naturally map into elements of a matrix. For an unstructured mesh the points cannot

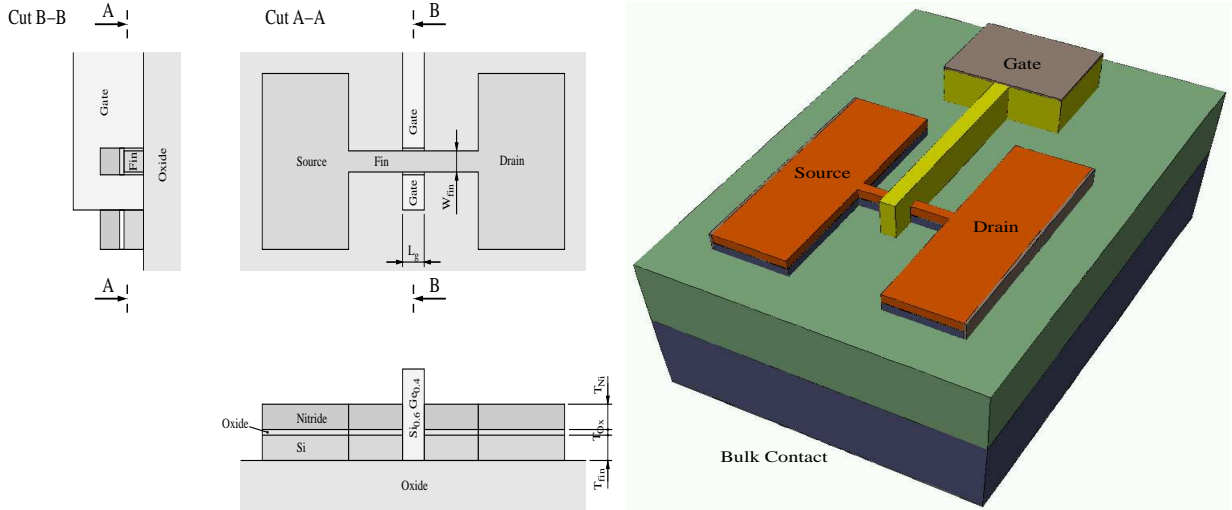


Figure 1: Geometry of the simulated FINFET structure.

be represented in such a manner and additional information has to be provided. For any particular point the connection with other points must be defined explicitly in the connectivity list.

The unstructured approach is ideally suited for the discretization of complicated geometrical domains. Element size and orientation can vary over the simulation domain, which allows a flexible spatial resolution. Downsides of these advantages are complex data structures and in contrast to the generation of structured grids, algorithms to construct unstructured grids are frequently based upon geometrical ideas which are unfortunately from a technology point of view, still something of an art, as well as a science.

In this work we analyze the suitability of structured and unstructured meshes for three-dimensional device simulation. Both meshing approaches have to fulfill Delaunay's criterion which is essential for the box integration discretization scheme.

Delaunay Properties

Delaunay's criterion [6] defines a property essential for grids used in device simulation. It is based on the definition of Voronoi boxes [7]. It is well known, that Delaunay's criterion and the definition of Voronoi boxes are dual. Grids suitable for three-dimensional device simulation must consist of elements which satisfy Delaunay's criterion. Moreover obtuse and small angled elements should be avoided.

Box Integration Method

For the discretization [8] of the differential equations the finite box method (box integration) is used. It uses a grid consisting of points and lines where each point P_i is assigned its Voronoi box Ω_i which is defined as its

corresponding part of the simulation area. All boxes together form the whole simulation area Ω .

The FinFET

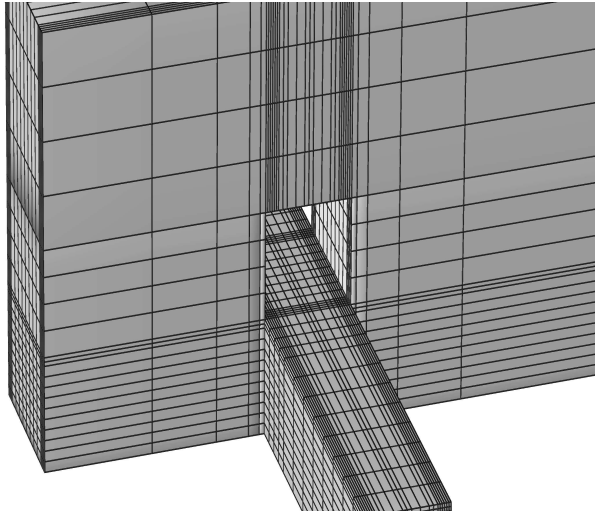
Figure 1 shows the basic structure of a FINFET analyzed in [4]. The device is formed on a thin silicon on insulator (SOI) finger termed fin. On the top of the silicon fin nitride has been deposited on a thin pad oxide to protect the silicon fin during gate poly-SiGe etching. The gates are formed at the vertical sides of the fin using a thin gate oxide layer. Gate work-function tailoring is essential to adjust the threshold voltage. Therefore, for the gate material poly-SiGe has been chosen.

According to Figure 1 the device dimensions are: $T_{fin} = 50\text{nm}$, $T_{OX} = 4\text{nm}$, $T_{Ni} = 50\text{nm}$, $W_{fin} = 40\text{nm}$, and $L_g = 60\text{nm}$. The thickness of the gate-oxide (not T_{OX}) is 1.5nm. The geometrical channel width is given by $2T_{fin}$ for one fin since both channels have to be taken into account. Due to the thick silicon nitride cap on the top of the fin the influence of the top gate can be neglected and the FINFET can be termed a double-gate device.

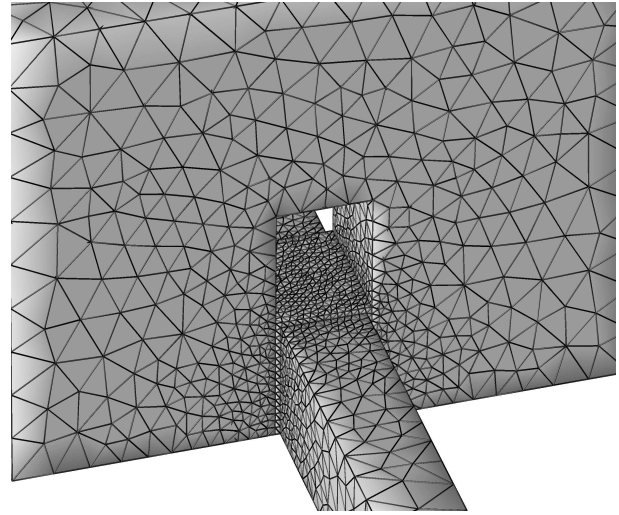
To obtain higher drive currents additional fins must be applied in parallel. The gate comb is formed as a small stripe which contacts the gates of all fins.

The crucial geometric device dimensions are:

- L_g : printed gate length.
- L_{eff} : effective gate length which is determined by the distance of the junctions.
- T_{fin} : Height of the fin.
- W_{fin} : Width of the fin, which is the distance between the gate oxides of the two gates.



(a) Structured ortho-based grid without terminating lines. The high mesh density is not local to the gate-oxide and channel area.



(b) Unstructured mesh with element grading from a fine channel mesh up to a coarse mesh for the surrounding gate line..

Figure 2: Mesh comparison between structured and unstructured mesh representation of the simulated FINFET device. Cut-out of the fin area without the protection nitride layer on top of fin, source, and drain line.

Mesh Representation

Figure 2(a) shows a structured ortho-based grid without terminating lines. As already noticed, the high mesh density is continuative in regions where a coarser mesh would be sufficient and produces therefore an unneeded high amount of grid points and elements.

For the unstructured grid, see Figure 2(b), we used Gmsh¹ which is a finite element mesh generator (primarily Delaunay) with built-in pre- and post-processing facilities [9]. The element grading was chosen from very small elements within the gate-oxide and the channel area, where large elements are placed in the surrounding gate line.

The third test structure is shown in Figure 5. The specialty of this structure is the combination of two meshing approaches. The fin is represented by an highly regular orthogonal octree-based meshed. Such meshes are constructed by the usage of a pure cuboid mesh where every cube is divided into six tetrahedrons. For the rest of the structure an unstructured mesh was used.

Source Drain Doping Profile

The device is very sensitive to the gate under-lap ΔL and the lateral source - drain doping gradient of the junctions doping. For the FINFET simulations a source - drain doping concentration of $N_D = 10^{20} \text{cm}^{-3}$ has been assumed. The doping profile at the junctions have

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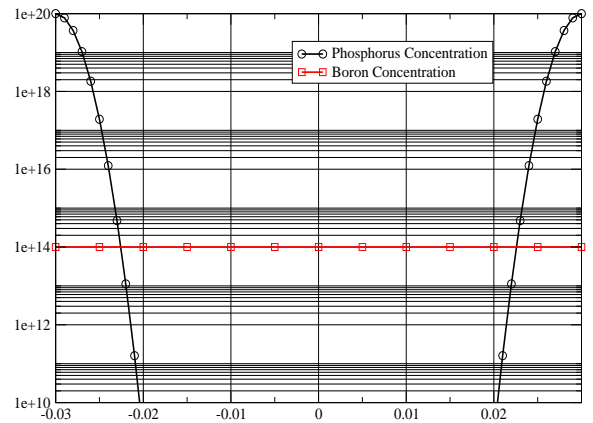


Figure 3: Gaussian shaped doping concentration over gate length L_g in μm .

a Gaussian shape and is shown in Figure 3. The source - drain gradient was set to approximately 1nm/dec. The Boron concentration can be neglected. For all simulations a gate under-lap of $\Delta L = 4\text{nm}$ was used. Therefore the effective gate length is assumed to be fixed at $L_{eff} = L_{gate} - 2\Delta L = 52\text{nm}$.

Simulation Results

Figure 4 gives the $I_D - V_{DS}$ characteristics of the device. The threshold voltage is $V_{th} = -0.13\text{V}$ and the current is normalized by the channel width which is given by $2T_{fin}$. All teststructures show the same characteristics within a tolerance band of approximately 2.5 percent. The error bars shows the different simulation results according to the three test structures.

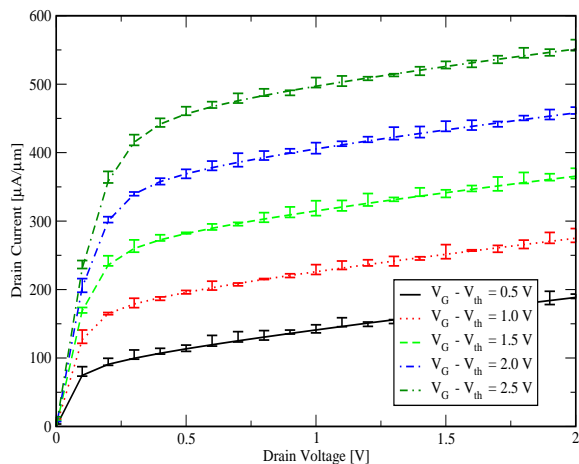


Figure 4: Result of three-dimensional simulation of the double-gate FinFET shown in Figure 1. The current is normalized by $2T_{fin}$. $V_{th} = -0.13V$.

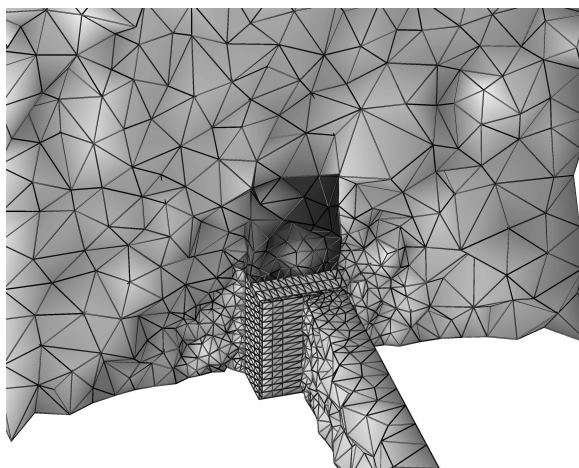


Figure 5: Cutout of the three-dimensional test structure. The fin is presented by an highly regular tetrahedron mesh. Source, drain, fin-nitride, and gate-line are meshed in an unstructured manner.

Table 1 shows a short simulation benchmark data overview. The mesh density was chosen with respect to the total amount of elements which gives for the box integration method roughly the same rank of the linear equation system. So the simulation time differs which depends in the first instance on the rank and secondly on the convergence of the Newton iteration scheme. It has been observed that for the unstructured mesh the convergence of the solver was inferior than on the structured example. The mixed approach shows good convergence behavior by nearly the same equation system dimension compared to the others examples.

Conclusion

We compared two meshing approaches for their suitability on three-dimensional device simulation. It is clear that for cuboid based grids without terminating lines the amount of mesh points for realistic three-

#	Ortho	Unstr.	Mixed
Points	98.317	15.803	16.356
Elements	11.737 Cubes 70.965 Tets	63.212	72.312
Rank	47.768	36.158	43.363
Sim. time	5h 33'	6h 34'	5h 7'

Table 1: Benchmark values of the simulated test structures, see Figure 2.

dimensional structures is prohibitive high. If a high mesh density is needed only in one region of the device, it is inescapable that other regions are influenced because of the non-terminating lines. To bear down this we used an unstructured meshing approach which allows more flexible variations of the element size over the simulation domain. The drawback of this approach is the rather bad convergence of the solver in the channel region of the device. So the best solution for this problem is to use an mixed approach which offers the benefit of the orthogonal mesh for the channel region and the unstructured approach for the rest of the simulation domain.

Acknowledgment

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