Simulation of Dynamic NBTI Degradation for a 90nm CMOS Technology

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ABSTRACT

The NBTI effect has become the limiting factor for the reliability of p-MOSFETs in the sub-100nm regime. In this work the dynamic NBTI degradation was systematically investigated for a 90nm p-MOSFET by experiment and simulation. For thin gate oxides stressed at low to medium gate voltages the bulk traps can be neglected and NBTI occurs mainly due to the generation of interface traps. Under this condition the reaction-diffusion model can be applied for the prediction of NBTI degradation. The model parameters were calibrated for NBTI simulations at arbitrary gate voltage, frequency, and duty cycle within a calibrated range. The long-time NBTI degradation was simulated up to 10 years in order to estimate the transistor lifetime under typical chip operation conditions.

Keywords: negative bias temperature instability, dynamic NBTI effect, silicon-oxide interface trap density, reaction-diffusion model, transistor lifetime estimation

1 INTRODUCTION

Negative bias temperature instability (NBTI) leads to rapid negative shifts of the p-MOSFET threshold voltage V_T due to the buildup of positive charged interface traps N_{it}. The generation of interface traps occurs when the transistor is stressed by negative gate voltages at elevated temperatures. NBTI degradation increases the absolute V_T value and reduces the drain current and transconductance of the transistor. It was found that the DC degradation follows a power-law time dependence which can be approximately described by $N_{it}(t) \propto t^{\frac{1}{4}}$. Under AC operation the interface traps generated during the on-state of the transistor are partially annealed in the off-state. Compared to static NBTI behavior the dynamic NBTI effect thus significantly improves the transistor lifetime.

While the microscopic details of the NBTI mechanism are not fully understood, it is speculated that interface traps are generated by dissociation of Si–H bonds at the silicon-oxide interface during NBTI stress [4]. A released hydrogen atom diffuses away from the silicon-oxide interface and leaves an interface trap behind which is charged positive. Although interface traps are mainly responsible for NBTI in the majority of the cases, oxide traps dominate the overall degradation for high gate voltages particularly in thick oxide devices [5].

In order to allow the treatment of bulk traps as well, an equivalent positive sheet charge located at the silicon-oxide interface can be defined, which is caused by interface and bulk traps during inversion of the p-MOSFET. The equivalent sheet charge density ($N_{it} \cdot q$) produces a threshold voltage shift ΔV_T which depends on the oxide capacitance per unit area, C_{ox}, according to

$$\Delta V_T = -\frac{N_{it} \cdot q}{C_{ox}} \tag{1}$$

The V_T degradation in the p-MOSFET reduces the gate overdrive ($V_G - V_T$) wich leads to a reduced drive current. This is consistent with the observation that the rise time of the CMOS inverter output signal, controlled by the p-MOSFET, degrades over time, whereas the fall time, controlled by the n-MOSFET, stays unchanged. The magnitude of the NBTI induced parameter shift depends also significantly on the frequencies and duty cycles which occur during operation of the transistor [1]. Nitrogen plays a key role in NBTI sensitivity, especially if it is located near the silicon-oxide interface. It can be speculated that the application of thinner SiON gate dielectrics leads to a faster hydrogen diffusion due to the lower quality of the nitrided oxide compared to pure silicon dioxide. The faster loss of hydrogen at the interface increases the NBTI degradation. For heavily nitrided, thin gate oxides at low electric fields NBTI may dominate over hot carrier injection (HCI) which occurs primarily in the n-MOSFET [2].

In this paper NBTI degradation was systematically investigated for the p-MOSFET of a 90nm technology with 20Å equivalent oxide thickness (EOT). Specific experiments were performed in order to analyze the gate voltage, duty cycle, and frequency dependence of the NBTI degradation behavior. Frequency measurements were performed in the range from DC to 1 MHz and "ON" duty cycles in the range of 30% to 70% were used. Stress voltages were applied from -1.5 V up to -2.7 V to the gate of the transistor at a temperature of 125° C. The collected measurement data were used to fit the model parameters for NBTI simulations.

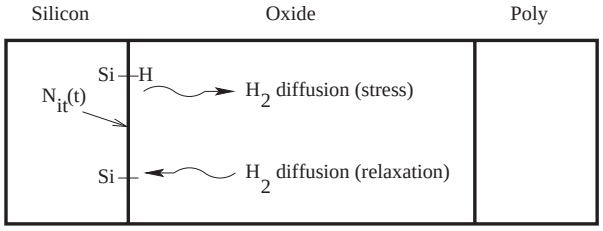

Figure 1: Description of the R-D model [4].

2 REACTION-DIFFUSION MODEL

A reaction-diffusion (R-D) model is used for the simulation of NBTI degradation, because this model accurately reproduces experimental NBTI data [3]. The R-D model states that the buildup of interface traps N_{it} arises from dissociation of hydrogen (constant dissociation rate k_f) governed by an electrochemical reaction between inversion layer holes and Si–H bonds. The released hydrogen diffuses away from the silicon-oxide interface or reacts with a dangling silicon bond. The N_{it} passivation occurs with anneal rate k_r [4]. When the transistor is switched off, annealing occurs at unchanged anneal rate k_r and dissociation rate $k_f = 0$. The R-D model is schematically explained in Figure 1. This sketch demonstrates that the released hydrogen diffuses into the oxide during the stress phase and returns to the interface during the relaxation phase. In the first few seconds the trap generation is controlled by the reaction process (fast N_{it} build-up), while the long-time generation is governed by the diffusion process (slow N_{it} generation). The stress phase (N_{it} generation) and relaxation phase (N_{it} annealing) can be observed in Figure 2. The R-D model is described by the following two coupled differential equations

$$\frac{\partial N_{it}(t)}{\partial t} = k_f\,[N_0 - N_{it}(t)] - k_r\,N_{it}(t)\,C_H(x,t)|_{x=0} \quad (2)$$

$$\frac{\partial N_{it}(t)}{\partial t} = -D\,\frac{\partial C_H(x,t)}{\partial x}\Big|_{x=0} + \frac{\delta}{2}\frac{\partial C_H(x,t)}{\partial t} \quad (3)$$

A prerequisite for the applicability of the R-D model is that the generated bulk traps during NBTI aging can be neglected compared to the generated interface defect density. Recently, charge pumping and stress-induced leakage current (SILC) measurements revealed that this prerequisite is fulfilled for thinner oxides stressed at low to medium gate voltages [5]. Also, the generation of bulk traps caused by injection of hot holes into the oxide shows a much stronger voltage dependence than the interface trap generation. However, an excellent ΔV_T versus N_{it} correlation over a wide range of gate voltages supports the absence of bulk traps and that ΔV_T is purely due to interface traps N_{it} [5].

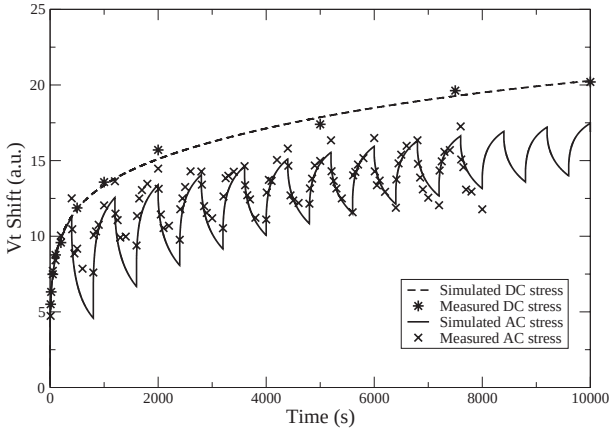

Figure 2: Simulated and measured NBTI.

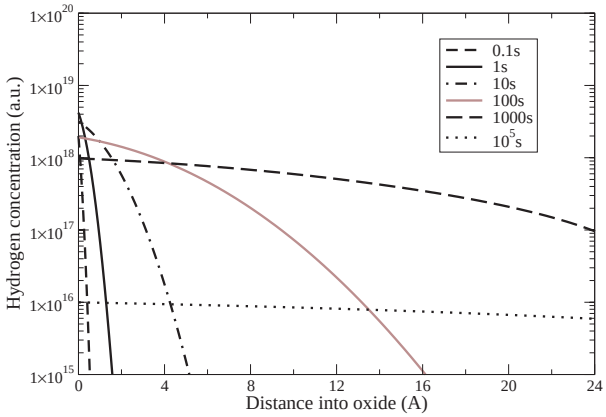

Figure 3: Hydrogen diffusion profiles.

3 SIMULATION

A one-dimensional finite differences method was applied for the discretization of the differential equations with the boundary condition of an absorbing wall at the oxide-poly interface. A neutral diffusion species (atomic or molecular hydrogen) is assumed and the hydrogen distribution profile in the oxide $C_H(x,t)$ is calculated for every time step [6]. The result is the defect density N_{it} and the corresponding shift $\Delta V_T \propto N_{it}$. Figure 2 shows the simulation result for DC stress compared to some cycles of AC stress at a very low frequency. It demonstrates a good agreement of the predicted V_T degradation with measured NBTI data. Figure 3 shows snap-shots of the corresponding hydrogen distribution in the oxide during DC stress. Note that the traps at the interface are built up quickly during the first seconds (reaction-limited regime) corresponding to a fast generation of a high level of hydrogen concentration in the interface zone. With increasing time the hydrogen diffusion front moves towards the oxide-poly interface

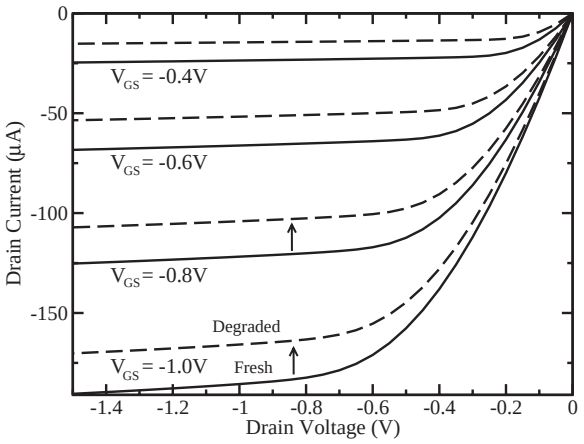

Figure 4: Degraded output characteristics.

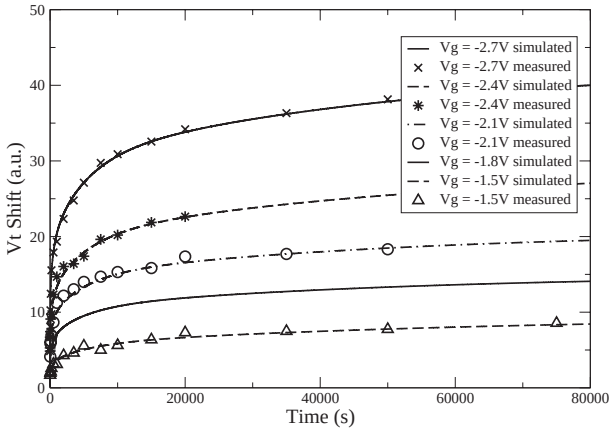

Figure 5: NBTI gate voltage dependence.

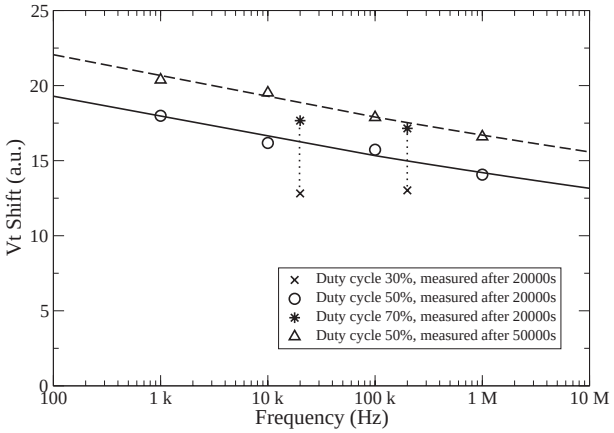

Figure 6: NBTI frequency dependence.

(diffusion-limited regime). After long times the hydrogen concentration at the silicon-oxide interface becomes low again corresponding to a high level of generated defects.

The calculated N_{it} value can further be used as input value for the device simulator Minimos-NT in order to simulate the degraded output characteristics of the p-MOSFET. Figure 4 shows the Minimos-NT result for the degraded drain curent of a p-MOSFET with 30Å EOT at the end of the lifetime, defined by $\Delta V_T = 60mV$ [7].

3.1 Gate Voltage Dependence

In order to allow an NBTI simulation under more realistic operation conditions, the gate voltage dependence was included in the simulations. The dissociation rate k_f is determined by the available surface hole concentration which depends on the applied gate voltage. The dissociation rate is directly proportional to the inversion hole density P ($k_f \propto P$) [5]. The inversion holes tunnel to the Si–H bonds located in the SiO_x interface zone governed by the electrical field. The amount of Si–H bonds N_0 at the interface which can be reached by this stochastic tunneling process increases with the oxide field. The holes get captured and take away one electron from the Si-H bonds. The weakened Si-H bonds are then broken by thermal excitation [5]. Figure 5 shows an excellent agreement between the simulation results and NBTI experimental data in the whole measurement range from -1.5V up to -2.7V. It can be observed that the V_T degradation depends on the gate voltage in a non-linear manner, especially in the higher stress voltage regime.

3.2 Frequency Dependence

Contrary statements can be found in the literature, whether NBTI depends on the frequency or not. No frequency dependence was found for NBTI measurements up to 200kHz after a stress time of only 1000s [8]. However, as depicted in Figure 6 the NBTI degradation is significantly reduced for higher frequencies and/or smaller "ON" duty cycles. The measured frequency dependence can be described by using a reference frequency $f_0 \in$ [1kHz,1MHz] according to

$$V_T(f) \;=\; V_T(f_0)\;\left(\frac{f}{f_0}\right)^{-0.03323} \qquad (4)$$

The reaction-diffusion model predicts no frequency dependence of the NBTI degradation. In this first order model the dynamic NBTI degradation depends only on the duty cycle of the gate signal. On the other side, NBTI simulations in the range of years for high frequency operation are not feasible due to the required small time resolution which should be in the range of about $\frac{1}{10}$ of the period duration. For fast simulation at high frequencies we suggest to perform the simulation at low frequency f_0 with equal duty cycle and to correct

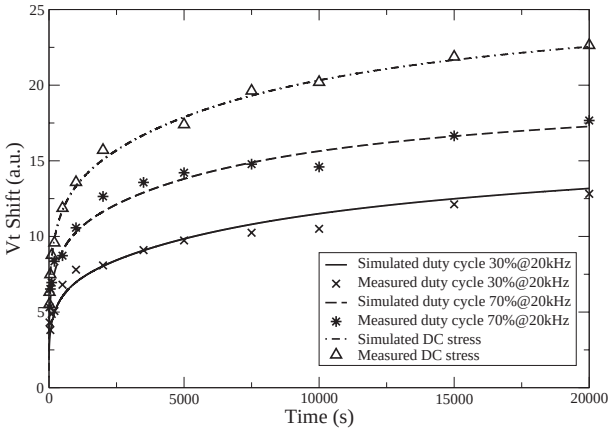

Figure 7: NBTI duty cycle dependence.

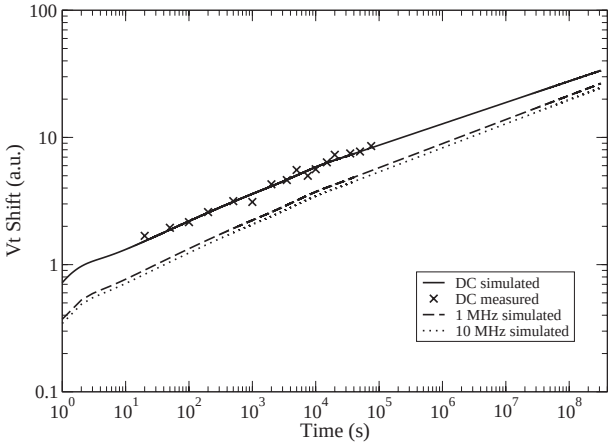

Figure 8: Long-time NBTI simulation for 10 years.

the result afterwards with the NBTI shift as function of the frequency according to (4). As depicted in Figure 7, this simple approach can accurately predict measurements for 20 kHz at different duty cycles.

3.3 Lifetime Estimation

Currently there is no agreed standard procedure available for the characterization and the measurement of NBTI reliability. Companies use different failure criterions for the definition of the device lifetime. Often the stress conditions for the NBTI measurements are chosen in a way which allows to extrapolate a theoretical transistor lifetime of 10 years. A reasonable failure criterion for the lifetime of the 90nm technology is, for instance, $\Delta V_T/V_T = 10\%$. For other transistor types, such as power devices, this criterion may be too strict since a higher V_T shift may be tolerable. Figure 8 compares long-time NBTI degradation simulations for the lifetime estimation under DC and typical chip operation frequencies. It can be observed that the diffusion-limited regime is reached after about two seconds which is characterized by a reduced slope of the V_T shift over time.

4 CONCLUSION

The NBTI mechanism was systematically investigated for a 90nm CMOS technology. Experiments at different gate voltages, frequencies, and duty cycles were performed in order to analyze the NBTI behavior of the p-MOSFET. The simulation method is based on the numerical solution of the reaction-diffusion model. The R-D model was extended to include the gate voltage and frequency dependence. The successful calibration of the model parameters is demonstrated by comparing the simulation results with measured NBTI data. All experimental data could be well reproduced. The presented simulation approach allows to predict the p-MOSFET lifetime depending on the applied stress operation conditions.

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