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Enhancement of breakdown voltage for Ni-SiC Schottky diodes utilizing field plate edge termination

T. Ayalew*†, A. Gehring°, T. Grasser†, and S. Selberherr°

†*Christian-Doppler-Laboratory for* TCAD *in Microelectronics at the Institute for Microelectronics*

°*Institute for Microelectronics, TU Vienna, Gußhausstraße 27–29, A-1040 Wien, Austria*

Abstract

In this work the improvement in breakdown voltage of Ni-SiC Schottky diodes utilizing field plate edge termination is presented. We have performed numerical investigations on how the addition of the field plate affects the relationship between the device structure, performance, and reliability. The key parameters that alter the overall device performance have been optimized using the device simulator MINIMOS-NT. This structure with a high barrier height metal such as Ni results in Schottky diodes with breakdown voltages in excess of 35% compared to the Schottky diodes without edge termination. The ratio of the maximum field under the anode corner to the field under the center of the contact at the same depth is reduced by a factor of two for edge terminated diodes for a wide range of doping levels. The leakage current in reverse biased operation is lowered by two orders of magnitude at room temperature and nearly by an order of magnitude at 500 K.

1. Introduction

SiC has been projected to have tremendous potential for high voltage solid state power devices with very high voltage and current ratings because of its high electric breakdown field of $1.5-4\times10^6$ V/cm and high thermal conductivity of $2.5-5$ W/cm K, depending on the doping level [1]. The high breakdown field allows the use of much higher doping and thinner layers for a given voltage than required in Si devices, resulting in specific on-resistances for SiC unipolar devices that can be $1/300^{th}$ that of the equivalent Si devices.

Schottky barrier diodes (SBDs) are attractive, because they provide rectification without significant switching loss. Although SBDs are desirable because of their low switching loss, it is not feasible to build high voltage SBDs in silicon. The main reason in addition to an extremely large specific on-resistance is the relatively low barrier height between common metals and silicon. However, with SiC due to its wide bandgap energy, it is easy to fabricate SBDs with barrier heights as high as 1.5 eV [2].

For high-voltage Schottky diodes it is necessary to have an edge termination around the periphery of the diodes to reduce the electric field crowding at the diode edges. Several techniques have been shown to reduce the field crowding at the edges, thus resulting in higher breakdown voltages. These include:

i. a resistive termination extension (RTE) [3];

ii. a junction termination extension (JTE) by implantation at the periphery of the diode to form an amorphous area around the periphery of the device [4, 5]; and

iii. a p-n junction guard-ring termination by a local oxide process (LOCOS) [6].

In most of these structures the SiC surface is unpassivated and there is no dielectric isolation between devices on the chip. In this work we used a simple metal

*Corresponding author. Tel.: +43-1-58801/36025; fax: +43-1-58801/36099.

E-mail address: Ayalew@iue.tuwien.ac.at (T. Ayalew).

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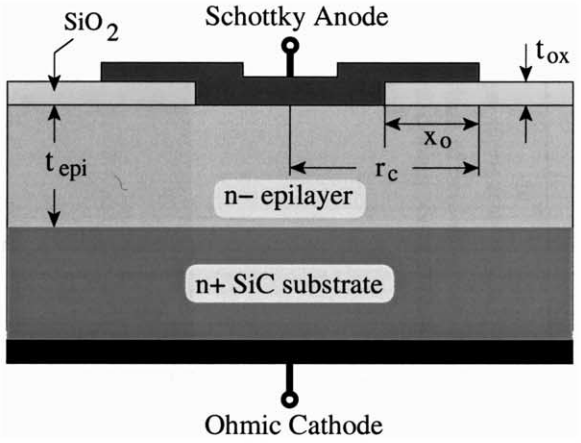

Figure 1. Schematics of the cross section of a field plate terminated Ni-SiC Schottky barrier diode.

field plate structure as shown Fig. 1, in which the Schottky contact overlaps a thermally grown SiO_2 layer so that the maximum electric field at any applied bias is at the SiO_2-metal interface. In addition, the oxide layer grown serves two other purposes: a) surface passivation; and b) removal of surface defects from the SiC layer which upon oxidation is etched off from the areas where the Schottky contact is to be formed.

We have performed numerical investigations using the general-purpose device simulator MINIMOS-NT [7] on how the addition of the field plate affects the relationship between the device structure, performance, and reliability. The key parameters that alter the overall device performance have been optimized. This structure with a high barrier height metal such as Ni results in Schottky diodes with breakdown voltages in excess of 35% compared to the Schottky diodes without edge termination. The ratio of the maximum field under the anode corner to the field under the center of the contact at the same depth is reduced to 50%. The leakage current is minimized by two orders of magnitude at room temperature and nearly by an order at 500 K.

2. Device Structure

Schottky barrier diodes (SBDs) in SiC are often made of an n-type material because of the higher electron mobility [8], and 4H-SiC is preferred because its electron mobility is about twice that of 6H-SiC. The cross section of a field plate edge terminated SBD in SiC shown in Fig. 1 consists of an n-type SiC epitaxial layer with a doping concentration of 2×10^{16} cm^{-3} grown over an n+ SiC substrate. The method of edge termination of the SBD has been found to be of importance for obtaining acceptable reverse blocking characteristics.

The barrier height of the metal-Schottky contact plays a critical role in the leakage current and the on-state voltage drop of the Schottky diodes. Selection of the metal to be used for the Schottky contact is thus based on the power loss of the diode which depends on the temperature at which the diode is to be operated. In forward bias, since the on-resistance of SiC Schottky diodes is low, the dominant component of the voltage drop occurs across the metal-SiC Schottky barrier.

Thus diodes utilizing metals with a larger Schottky barrier to SiC experience a larger on-state voltage drop. However, for high-temperature operation of SiC power rectifiers, such metals are still preferable because they also result in lower leakage currents [9]. Thus, the overall on/off ratio of the Schottky diode is higher if we use metals that form a larger Schottky barrier. To determine the optimum barrier height of the Schottky contact, the static power-loss analysis can be performed for rectifiers operating at a 50% duty cycle. Under these conditions, the maximum sum of static power loss dissipated during the on-state and the off-state per unit area is given by (1)

$$P_{\text{loss}} = \frac{1}{2}\left(J_{\text{F}}V_{\text{F}} + J_{\text{R}}V_{\text{R}}\right), \tag{1}$$

where J_{F} and J_{R} are the forward and reverse current densities, while V_{F} and V_{R} are the forward and reverse voltages, respectively. The calculated power losses for 1.2 kV SiC Schottky diodes as a function of metal barrier height and temperature show [10] that it is more efficient to use metals that form large barrier heights ($\geq$ 1.5 eV) if operation of diodes at higher temperatures is desired. Several reports (see Table 2) have shown that Ni results in suitably large barrier heights (1.5 – 1.7 eV) to SiC. Thus, we have utilized this metal to study high-voltage Schottky rectifiers on 4H-SiC for high-temperature applications.

The epitaxial layer thickness t_{epi}, oxide thickness t_{ox}, and the lateral metal overlap x_{o} were varied to study their effects on the electric field, the breakdown voltage, and the leakage current. In particular, t_{epi} was varied to ensure that there is no punch-through up to the breakdown voltage. The optimum value of x_{o} by which

Table 1
Optimized device parameters for a field plate edge terminated Ni/4H-SiC SBD.

parameter	value
epilayer thickness t_{epi}	11 μm
epilayer doping N_{D}	2×10^{16} cm^{-3}
oxide thickness t_{ox}	50 nm
lateral metal overlap x_{o}	11 μm
contact radius r_{c}	22 μm

the breakdown voltage should not be affected by electric field crowding is found to be approximately equal to the thickness of the SiC epilayer t_{epi}. The symbol r_c denotes the radius of the metal contact. Optimized device parameters for a field plate edge terminated Ni/4H-SiC SBD are listed in Table 1.

3. Schottky Contact Formation and Modeling

A Schottky barrier refers to a metal-semiconductor contact having a large barrier height (i.e. $\phi_B > k_B T_L$) and a low doping concentration that is less than the density of states in the conduction or valence band. The potential barrier between the metal and the semiconductor can be identified on an energy band diagram. To construct such a diagram we first consider the energy band diagram of the metal and the semiconductor, and align them using the same vacuum level as shown in Fig. 2 (a). As the metal and semiconductor are brought together, the Fermi energies of the two materials must be equal at thermal equilibrium Fig. 2 (b).

The barrier height ϕ_B is defined as the potential difference between the Fermi energy of the metal and the band edge where the majority carriers reside.

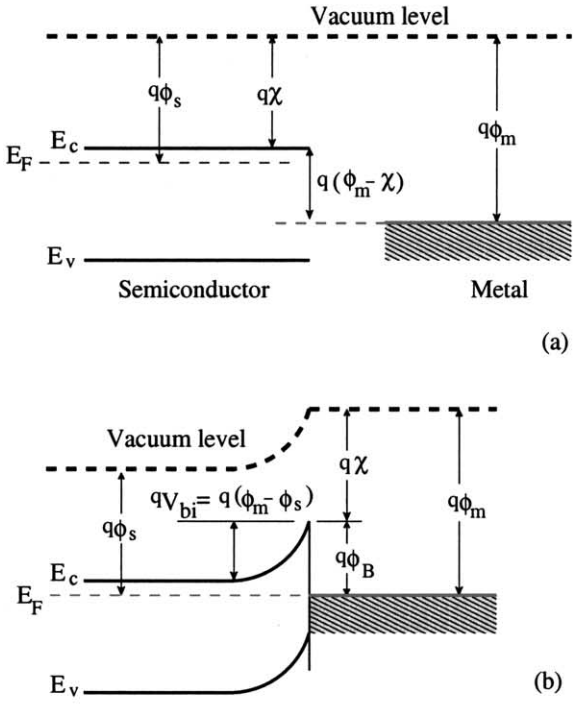

Figure 2. Energy band diagram of a metal adjacent to an n-type semiconductor under thermal nonequilibrium condition (a), metal-semiconductor contact in thermal equilibrium (b).

From Fig. 2 one finds that for n-type semiconductors the barrier height is obtained from

$$\phi_{Bn} = \phi_m - \chi, \tag{2}$$

where ϕ_m is the work function of the metal and χ is the electron affinity of the semiconductor.

A metal-semiconductor junction will therefore form a barrier for electrons if the Fermi energy of the metal is located between the conduction and the valence band edge.

In addition, we define the work function difference as the difference between the work function of the metal and that of the semiconductor. For n-type material it reads

$$\phi_{wf} = \phi_m - \chi - \frac{E_c - E_{F,n}}{q}, \tag{3}$$

The work function difference energy becomes

$$E_w = q\phi_{wf}. \tag{4}$$

The work function measured in vacuum and the barrier height for selected metal/4H-SiC junctions are listed in Table 2 [11–13]. These experimental barrier heights depend on the surface polarity of SiC (Si- and C-face), and often differ from the ones calculated using (2). This is due to the detailed behavior of the metal-semiconductor interface [13, 14]. The ideal metal-semiconductor theory assumes that both materials are pure and that there is no interaction between the two materials nor any interfacial layer [15]. Chemical reactions between the metal and the semiconductor alter the barrier height as do interface states at the surface of the semiconductor and interfacial layers. Furthermore, one finds the barrier heights reported in the literature to vary widely due to different surface cleaning procedures [11, 16].

The current density is calculated according to the thermionic emission condition [17] neglecting tunneling currents:

$$\mathbf{J}_n = -qv_n(n - n_s), \tag{5}$$

where n and n_s are the electron carrier concentrations at quasi-equilibrium and at the surface, respectively.

Table 2
Work function of selected metals and their measured and calculated barrier height on n-type 4H-SiC.

	Al	Ti	Ni	Au	Pt
ϕ_m	4.28	4.33	5.10	5.15	5.65
ϕ_B: Si-face	-	1.12	1.69	1.81	-
ϕ_B: C-face	-	1.25	1.87	2.07	-
ϕ_B: calculated	1.01	1.06	1.63	1.68	2.08

The thermionic recombination velocity v_n for electrons is given by [17]

$$v_n = \sqrt{\frac{k_B T_L}{2\pi m_n}} = \frac{4\pi m_n (k_B T_L)^2}{N_c h^3}. \quad (6)$$

Equation (6) is usually represented by the expression

$$v_n = A^* \frac{T_L^2}{qN_c}, \quad (7)$$

where

$$A^* = \frac{4\pi q m_n k_B{}^2}{h^3} \quad (8)$$

is known as the effective *Richardson constant*. It depends on the electron effective mass and has a theoretical value of 146 and 72 $Acm^{-2}K^{-2}$ for n-type 4H- and 6H-SiC, respectively [11].

The electron carrier concentration at quasi-equilibrium is given by

$$n = N_c \exp\left(-\frac{\phi_{Bn}}{k_B T_L}\right), \quad (9)$$

and at the surface

$$n_s = N_c \exp\left(\frac{-E_c - E_w}{k_B T_L}\right). \quad (10)$$

Note that (5) is equivalent to the most commonly used expression [17]

$$J_n = A^* T_L^2 \exp\left(\frac{q\phi_m - E_c}{k_B T_L}\right) \times \left[\exp\left(\frac{q\phi_{Bn} - q\phi_m}{k_B T_L}\right) - 1\right]. \quad (11)$$

To make the numerical investigation more realistic, a model that takes the effect of an oxide/SiC interface charge density on the reverse voltage operation into account has been incorporated [18].

4. Simulation Results and Discussion

From numerous simulation results on diodes with different epilayer doping concentration, Fig. 3 shows the on-state characteristics of the Ni/4H-SiC SBD at different temperatures for an epilayer thickness of 11 μm with a doping concentration of 2×10^{16} cm^{-3}.

The optimum value of the oxide thickness t_{ox} is predicted to be ~50 nm as depicted in Fig. 4. For extremely thick oxide layers, the field plate is so far away from the semiconductor that it does not have much influence on the electric field distribution. In this case, there is also not much improvement in breakdown voltage.

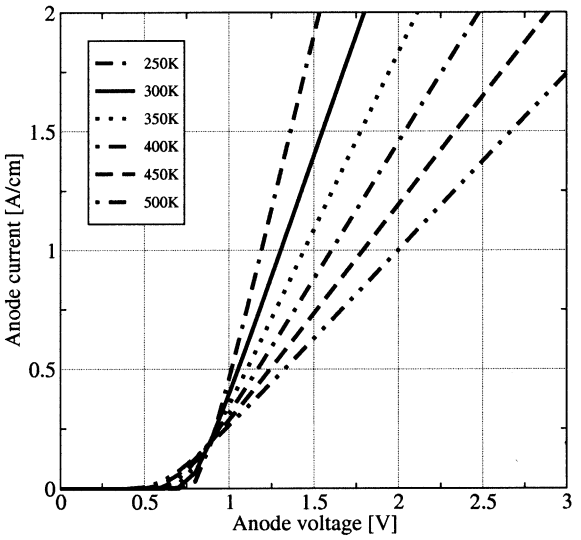

Figure 3. Forward biased characteristics of Ni/4H-SiC schottky barrier diode.

Hence, the optimum thickness of the field plate oxide is that which will be sufficiently thick that the peak electric field inside the oxide will not exceed the breakdown strength of the oxide; and will be sufficiently thin that the field plate can influence the electric field distribution inside the semiconductor and provide sufficient field relief at the corner. Fig. 4 also illustrates the influence of t_{ox} on the breakdown voltage caused by the presence of the peak electric field either in the oxide or inside the semiconductor under the corner.

Simulation results show that the optimum field plate

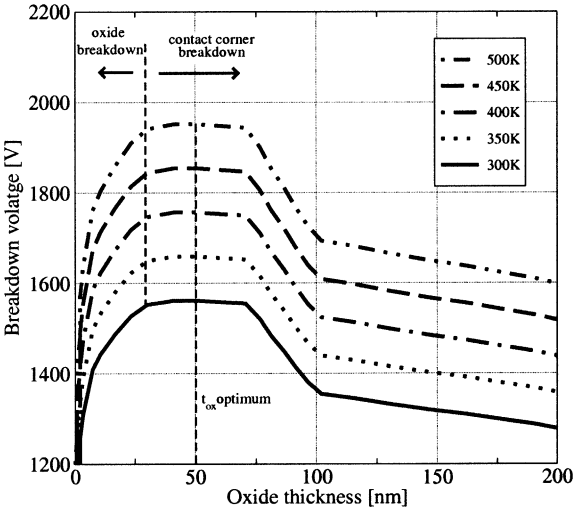

Figure 4. Relation between breakdown voltage and oxide thickness for an epilayer thickness of 11 μm with a doping concentration of 2×10^{16} cm^{-3}.

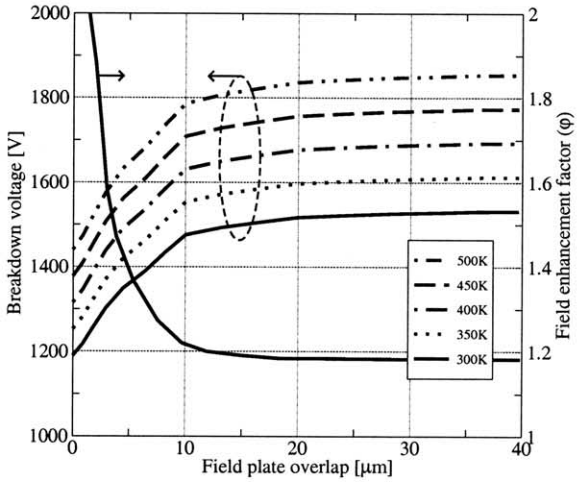

Figure 5. Effect of metal overlap on breakdown voltage and field enhancement factor.

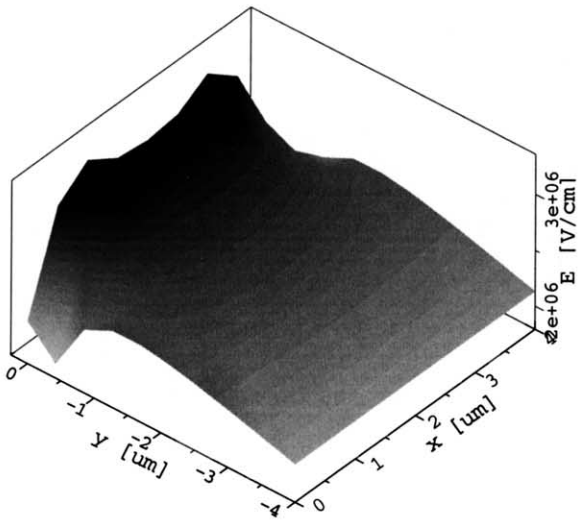

Figure 7. Electric field profile at the breakdown voltage.

overlap x_o for achieving the maximum breakdown voltage of a given doping concentration is roughly equivalent to the optimized epilayer thickness (which is determined by the depletion overlap at breakdown). Fig. 5 shows how the breakdown voltage and field enhancement factor φ (the ratio of the maximum field under the anode corner to the field under the center of the contact at the same depth) varies as a function of the metal overlap. It is clear that increasing the field plate overlap up to a certain limit will raise the breakdown voltage. Beyond that limit the breakdown voltage becomes almost independent of this overlap. The value of φ decreases progressively from the value for the unterminated diode with increasing field plate overlap until x_o is approximately equal to the depletion width at breakdown.

The field enhancement factor for unterminated Schottky diodes varies from approximately 2 for highly doped devices ($\sim 10^{17}\,\mathrm{cm}^{-3}$) to approximately 4 for diodes with a doping level of $\sim 10^{15}\,\mathrm{cm}^{-3}$. For diodes with edge termination the field enhancement factor varies from approximately 1.2 to 2.0 over the same range of doping levels as shown in Fig. 6.

From the electric field profile shown in Fig. 7 one can

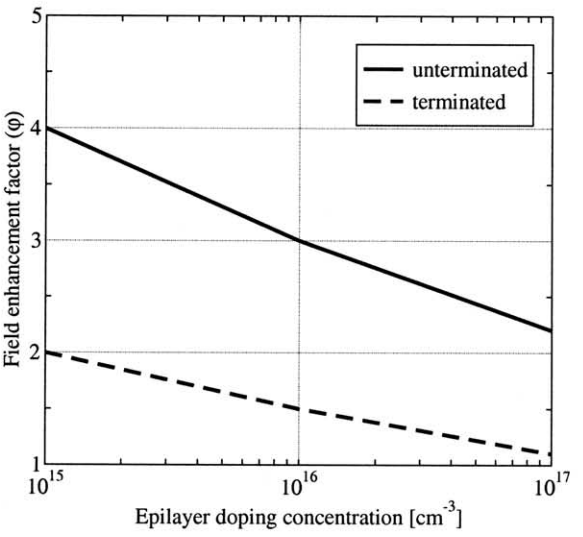

Figure 6. Comparison of field enhancement factor as a function of epilayer doping concentration at a depth of 1 μm under the anode.

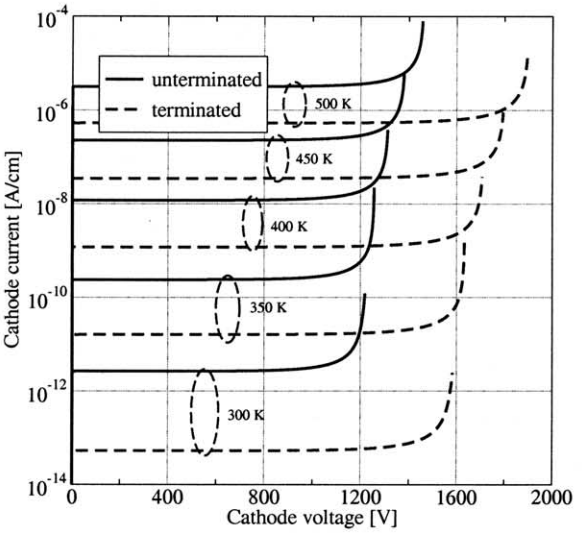

Figure 8. Comparison of unterminated and field terminated reverse voltage characteristics at different temperatures.

see that the peak electric field in the epitaxial layer occurs directly under the corner of the Schottky contact. The electric field directly under the center of the Schottky contact is smaller than the value under the corner.

Fig. 8 shows that the field plate edge terminated Ni-SiC Schottky barrier diodes improve the breakdown voltage by 35% while simultaneously reducing the leakage current by two orders of magnitude at room temperature and nearly by a factor of 10 at 500 K compared to the unterminated Schottky barrier diodes.

5. Conclusion

A new device structure that improves the breakdown voltage of Ni-SiC Schottky diodes by utilizing field plate edge termination is proposed. Numerical investigations on how the addition of the field plate affects the relationship between the device structure, performance, and reliability have been performed. The key parameters that alter the overall device performance are optimized using the general-purpose device simulator MINIMOS-NT. This structure improves the breakdown voltage by 35% compared to Schottky diodes without edge termination. The ratio of the maximum field under the anode corner to the field under the center of the contact at the same depth is reduced to 50% for an edge terminated diode compared with an unterminated counter part. The leakage current during the reverse biased operation for edge terminated structure is reduced by a factor of 100 at room temperature and nearly by a factor of 10 at 500 K.

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