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Numerical Simulation and Optimization for 900V 4H-SiC DiMOSFET fabrication

S. C. Kim[1, a], W. Bahng[1,b], N. K. Kim[1,c], E. D. Kim[1,d]
T. Ayalew[2,e], T. Grasser[2,f], and S. Selberherr[3,g]

[1]Power Semiconductor Research Group, Korea Electrotechnology Research Institute (KERI), Sung-ju dong 28-1, ChangWon-city, Gyungnam 641-120 Korea

[2]Christian Doppler-Laboratory for TCAD in Microelectronics at the Institute for Microelectronics, TU Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria

[3]Institute for Microelectronics, TU Vienna, Gusshausstrasse 27-29, A-1040 Vienna, Austria

[a]sckim@keri.re.kr, [b]bahng@keri.re.kr, [c]nkkim@keri.re.kr, [d]edkim@keri.re.kr,

[e]ayalew@iue.tuwien.ac.at, [f]grasser@iue.tuwien.ac.at, [g]selberherr@iue.tuwien.ac.at

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Abstract. We report the simulation results of 25μm half cell pitch vertical type 4H-SiC DiMOSFET using the general-purpose device simulator MINIMOS-NT. The best trade-off between breakdown voltage and on-resistance in terms of BFOM is around 19MW/cm^2 with a p-well spacing 5μm. The specific on -resistance, $R_{ON, sp}$, simulated with V_{GS}=10V and V_{DS}=1V at room temperature, is around 22.76mΩcm^2. An 900V breakdown voltage is simulated with ion-implanted edge termination.

Introduction

In power switching devices, Silicon was approached their theoretical limits in late 1980s [1]. Therefore many research works has been done using wideband gap semiconductor materials, especially Silicon Carbide or semiconducting diamond. Silicon Carbide has been around for over a century. However, only in the past two or three decades its semiconducting properties have been sufficiently studied and applied, especially for high-power and high-frequency devices. In this paper, we present numerical simulation-based optimization results of DiMOSFET with various edge termination using the general-purpose device simulator MINIMOS-NT [2].

Device Design

A cross section of the simulated DiMOSFET cell is shown in Fig. 1. The DiMOSFET structure is formed in SiC using a double implantation with two separate implantation masks. The initial wafer specification, which is commecially available wafer, is 10μm thick drift layer with doping concentration of 5x10^{15}cm^{-3}. P-well, with a surface concentration of around 5x10^{17}cm^{-3}, is formed by boron multiple implantation. We use experimental data of multiple energy boron implants for simulation and p-well junction depth is 0.6μm. Generally aluminum is used for p-well region, but we use boron impurities as p-well region to compare the experimental device which we will fabricate. Then a 0.2μm deep p+ region for an ohmic contact was formed with a box profile concentration of 5x10^{19}cm^{-3}. Nitrogen implants are used for n+ source region, and the peak concentration and junction depth are 5x10^{19}cm^{-3} and 0.15μm, respectively. Finally a 50nm gate oxide is formed. The ion-implanted edge termination has been realized in the same way, but with a lower dose, to achieve a box profile at about 1.5x10^{16}cm^{-3}.

For device simulation, we have utilized published material data in Table 1. Impact ionization is a typical non-equibrium process which requires large electric fields. It is modified by the reciprocal of the mean free path which is denoted the impact ionization coefficient. A review of measured data on impact ionization coefficients in α-SiC has been first published by Ruff et. al. and later by Bakowsky st. at., but most recently measured data compiled by Raghunathanr and Baliga at different temperatures show an about 20% higher critical electric field compared to the previous reports. It seems that the impact ionization coefficients are decreasing with increasing temperature. This implies the increase of the breakdown voltage, which is a desirable property for SiC power devices. The average impact ionization coefficients a_n and a_p are summarized in Table 1.

The mobility commonly measured is perpendicular to the c-axis. It is different from the mobility parallel to the c-axis. The difference between the two mobilities has been stuided experimentally. In 4H-SiC, ratio between perpendicular and parallel mobility is generally 0.8.

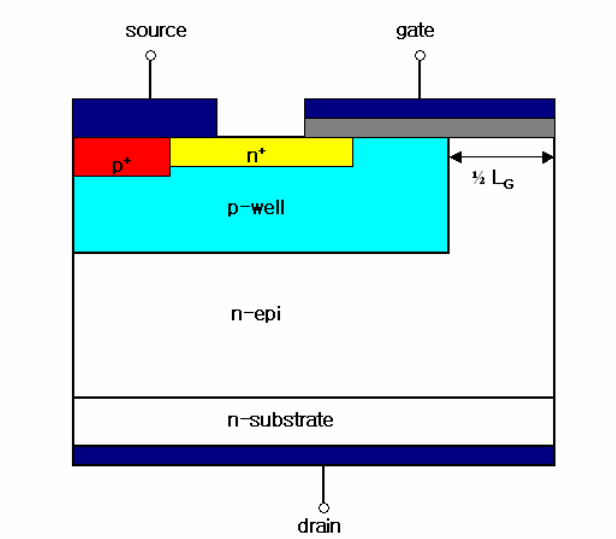

Fig. 1. Basic cell structure of simulated DiMOSFET.

Table 1. Model parameter used for simulating 4H-SiC DIMOSFET

Electron mobility μ_n $N_D = 10^{16}$ cm $^{-3}$	Hole mobility μ_p $N_A = 10^{16}$ cm $^{-3}$	Donors & Ionization Energy [meV]	Acceptors & Ionization Energy [meV]	Saturated Electron Velocity v [10^7 cm / s]
|| c-axis : 900 ⊥ c axis : 800	115	N : 50, 92 P : 54, 93	Al : 200 B : 285	2
α_n [cm $^{-1}$]	b_n[V/cm]	α_p [cm $^{-1}$]	b_p [V/cm]	←ω_{op} [meV]
3.44x10^6	2.58x10^7	3.5x10^6	1.7x10^7	106

Simulation Results and discussion

In order to achieve acceptable device performance, the maximum electric field in the oxide layer must be limited. For the desired breakdown voltage of 900V, the proposed device structure is optimized to have a 25μm half cell pitch and a 10μm thick n-drift region doped at 5x10^{15}cm^{-3}. The doping

concentration and the thickness of the p-well region are very important. If we decrease the p-well doping concentration below $3x10^{17}cm^{-3}$, the blocking voltage decreases because of a punchthrough. If we increase it further, the maximum operating voltage becomes limited by the maximum oxide field. The best trade-off between these relations has been achieved by setting the p-well doping concentration to $5x10^{17}cm^{-3}$.

Fig. 2 shows the on-state characteristics of simulated DiMOSFET at room temperature. The specific on-resistance, $R_{ON,sp}$, simulated with V_{GS}=10V and V_{DS}=1V at room temperature, is around $22.76m\Omega cm^2$. The specific on-resistance depends on the gate bias. A high gate bias was required to turn the device fully on. This means that the on-resistance is dominated by the MOS channel resistance at room temperature[2]. So that reducing the on-resistance results in increasing high channel mobility. In this simulation, the device has an MOS channel mobility of $84cm^2/Vs$ and a threshold voltage of around 6V. These specific-on resistance simulation results are introduced into Baliga's Figure of Merit (BFOM) as the criterion for structure optimization and comparision[3,4]. Fig. 3 shows the simulated results of BFOM depending on the p-well spacing. As shown in Fig. 3, the best trade-off relation between breakdown voltage and on-resistance in terms of BFOM is achieved with a p-well spacing 5μm.

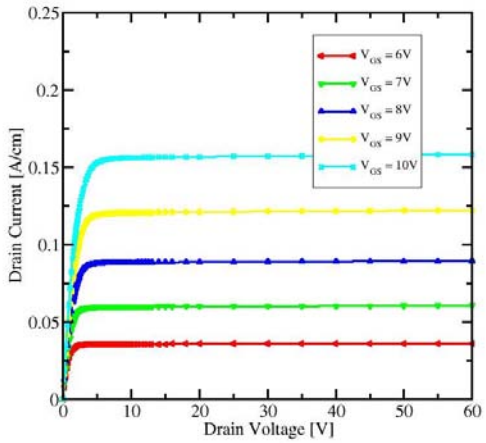

Fig. 2. Drain current characteristics of simulated DiMOSFET devices.

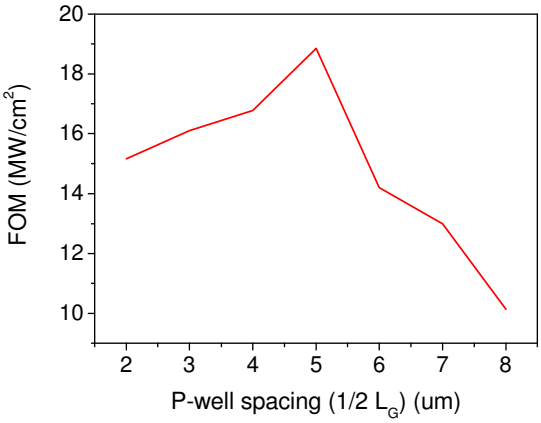

Fig. 3. Effects of p-well (1/2 L_G) spacing on the Baliga's Figure of Merit.

Fig 4. shows the breakdown voltage characteristics according to the termination structures. The two types of edge termination are simulated at 400K. One clear difference among the three structures is a higher breakdown voltage for the ion-implanted edge termination structure. In this figure, an ion-implanted edge termination structure improved the breakdown voltage from 720V to 900V

compared with the field plate structure. The no edge termination, field plate and ion-implanted edge termination structures feature 600, 720, and 900V breakdown voltages, respectively. The breakdown voltages are approximately 35, 45 and 53% of the ideal breakdown voltage in this DiMOSFET devices, respectively. In this simulation, the maximum electric field in the bulk region is 2.69MV/cm, which is 89% of the breakdown field in 4H-SiC. And also, the maximum electrical field in the gate oxide is 20% lower than the bulk electrical field, i.e. 2.16MV/cm.

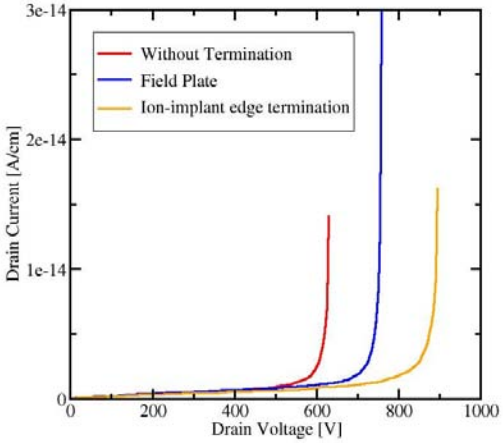

Fig. 4. Comparison of the breakdown voltage depending on the termination structures.

Summary

In this study, vertical DiMOSFET was simulated, and electrical characteristics were presented using the general-purpose device simulator MINIMOS-NT. The best trade-off between breakdown voltage and on-resistance is achieved with a p-well spacing 5μm. The specific on -resistance, $R_{ON,\ sp}$, simulated with V_{GS}=10V and V_{DS}=1V at room temperature, is around 22.76mΩcm^2. As the spacing between the p-well regions is increased to reduce the JFET resistance, the area of the device also increase, resulting larger $R_{ON,\ sp}$. The devices have an MOS channel mobility of 84cm^2/V·s and a threshold voltage of 6V. The on-resistance is dominated by the MOS channel resistance, therefore, high channel mobility is necessary to improve device performance. We compare the termination structures. Among three types, ion-implanted edge termination structure has best blocking capability. The breakdown voltage of around 900V is simulated in ion-implanted edge termination structure.

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