Improving the Ambipolar Behavior of Schottky Barrier Carbon Nanotube Field Effect Transistors

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Abstract

Due to the capability of ballistic transport, carbon nanotube field-effect transistors (CNTFETs) have been studied in recent years as a potential alternative to CMOS devices. CNTFETs can be fabricated with Ohmic or Schottky type contacts. We focus here on Schottky barrier CNTFETs which operate by modulating the transmission coefficient of Schottky barriers at the contact between the metal and the carbon nanotube (CNT). The ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices. We show that a double gate design can suppress the ambipolar behavior of Schottky barrier CNTFETs considerably. In this structure for an n-type device the first gate which is near the source controls electron injection and the second gate which is near the drain suppresses hole injection. The voltage of the second gate can be set to a constant voltage or to the drain voltage. We investigated the effect of the second gate voltage on the performance of the device and finally discuss the advantages and disadvantages of these designs.

1. Introduction

Carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale field effect transistors. While early devices have shown poor device characteristics, improvements were achieved by using doped CNTs [1] or high-κ materials [2]. The contact between metal and CNT can be of Ohmic [3] or Schottky type [4, 5]. Schottky contact CNTFETs operate by modulating the transmission coefficient of the Schottky barriers at the contact between the metal and the CNT [1, 5], but the ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices [6, 7].

Two important figures of merit of transistors are the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio and the subthreshold slope. By using thin high-κ materials as gate dielectric the subthreshold slope of CNTFETs can be improved [8], but due to their ambipolar behavior the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is limited. In this work we propose a double gate structure for CNTFETs. Using this structure the carrier injection at the source and drain contacts can be separately controlled. We show that for an n-type device electron injection at the source contact can be controlled via the first gate while the detrimental hole injection at the drain contact can be reduced by the second gate. Thus, the ambipolar behavior of CNTFETs can be completely avoided.

2. Approach

Assuming ballistic transport, we calculate the drain current using the Landauer-Büttiker formula [9]

$$I_{\mathrm{d}} = \frac{4\mathrm{q}}{\mathrm{h}} \int [f_{\mathrm{s}}(\mathcal{E}) - f_{\mathrm{d}}(\mathcal{E})] TC(\mathcal{E}) \mathrm{d}\mathcal{E}, \qquad (1)$$

where $f_{\mathrm{s,d}}$ are equilibrium Fermi functions at the source and drain contacts and $TC(\mathcal{E})$ is the transmission coefficient through the device. The factor 4 in (1) stems from the twofold band and twofold spin degeneracy [1]. In this work we focus on ambipolar devices, where the metal Fermi level is located in the middle of the CNT band gap at each contact.

We evaluate $TC(\mathcal{E})$ using the WKB approximation [8, 10, 11]

$$\ln TC(\mathcal{E}) = -2 \int k(x) \mathrm{d}x, \qquad (2)$$

and an idealized band structure [8, 10–12]

$$k = \frac{\mathcal{E}_{\mathrm{g}}}{\sqrt{3}\mathrm{a}\gamma_0} \sqrt{1 - \left(\frac{\mathcal{E} + \mathrm{q}V(x)}{\mathcal{E}_{\mathrm{g}}/2}\right)^2} \mathrm{d}x, \qquad (3)$$

The symbol $\mathrm{a} = 0.246\ \mathrm{nm}$ denotes the lattice constant, $\mathcal{E}_{\mathrm{g}}$ is the band gap energy set here to $0.6\ \mathrm{eV}$ corresponding to a CNT of a diameter of $1.4\ \mathrm{nm}$, $\gamma_0 = 2.5\ \mathrm{eV}$ is the transfer integral, and $V(x)$ is the electrostatic potential along the

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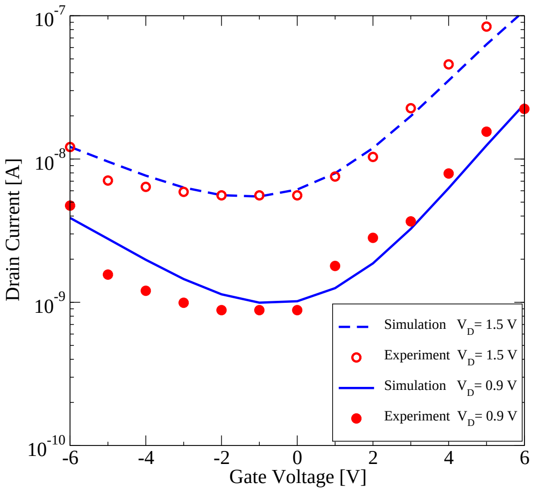

Figure 1. Comparison between the simulation and experimental results for an axial CNT.

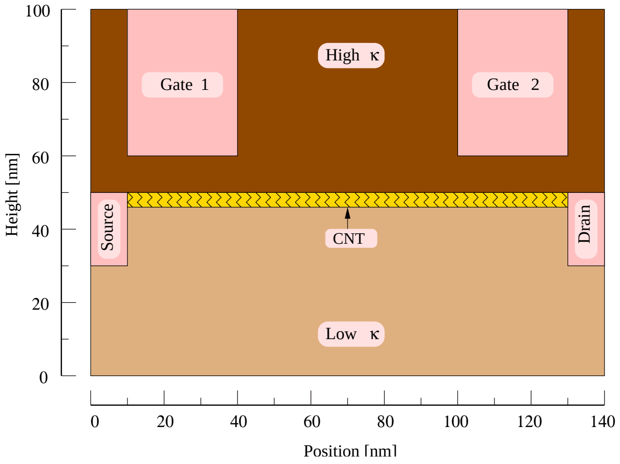

Figure 2. Sketch of the the double gate structure.

CNT. The integration in (2) is performed only within the classical turning points.

For electrostatic analysis the Smart-Analysis-Package (SAP) [13] was used. Since we focus on the subthreshold behavior of CNTFETs, we neglect charge on the CNT, which is considered to be a good approximation for the off-state regime [1, 6–8].

As seen in Fig. 1 our approach is in good agreement with experimental results for an axial CNT [14], more details can be found in [15]. Note that these calculations were performed for axial CNTs, which explains the low $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio and also the ambipolar behavior. In the following we will focus on lateral CNTs.

3. Results and Discussion

We investigated a double gate structure as sketched in Fig. 2 and a single gate structure. In the latter case the gate is extended from source to drain, like in conventional FETs. We used the same geometric dimensions for simulations as indicated in Fig. 2, except the CNT diameter was set to $1.4\ \mathrm{nm}$.

As seen in Fig. 2 high-κ and low-κ materials were used above and below the CNT. Like light refraction at the boundary of two media having different relative dielectric constants, the direction of the electric field will change. If the relative dielectric constant of the top material is higher than the bottom one, the direction of the electric field near the CNT is directed along the CNT axis, suppressing the Schottky contact. As a result the control of the gate over the Schottky barrier is increased, leading to a higher subthreshold slope [8]. In this work we use the relative dielectric constants of the high-κ and low-κ materials of 11 and 3.9 respectively.

Fig. 3 shows the current-voltage characteristics of the single gate structure. For this structure the current is symmetric with respect to the gate voltage, in agreement with experimental results [6, 8]. To understand this behavior the band edge profile for this single gate structure is shown in Fig. 4. Positive gate voltages near the source increase the tunneling current of electrons, which is desirable for n-type devices. By decreasing the gate voltage the tunneling current of electrons decreases, but the thermionic emission current of electrons does not vary. If the gate voltage decreases further to negative values the thermionic emission current of electrons also decreases. On the other hand by applying positive voltages higher than the gate voltage to the drain, the Schottky barrier near the drain is suppressed and consequently hole injection at the drain increases, an undesirable phenomenon for an n-type device. Especially in the off regime this would result in an intolerably high off-current.

From the above discussion it seems reasonable to control the band edge profile near the source and the drain contacts separately, leading to a double gate structure as shown in Fig. 2. The first gate near the source controls electron injection and the second gate near the drain suppresses hole injection at the drain contact. We considered two possibilities for the second gate voltage:

a) Applying the same voltage as the drain voltage.

b) Applying a constant voltage equal or higher than the maximum drain voltage.

If the same voltage as at the drain is applied to the second gate, at any drain voltage the band edge profile near the drain would be flat, see Fig. 6. In consequence the tunneling current of holes is suppressed and there is just some thermionic emission current of holes, resulting in an off-current which is nearly independent of the drain voltage and equals to the thermionic emission current over the Schottky barrier, see Fig. 5.

If an even lower off-current is required, then the second gate can be biased at a fixed voltage which is higher than the maximum drain voltage. This results in suppressing the hole thermionic emission current, see Fig. 6. As seen in Fig. 5 by using this design a very low off-current can

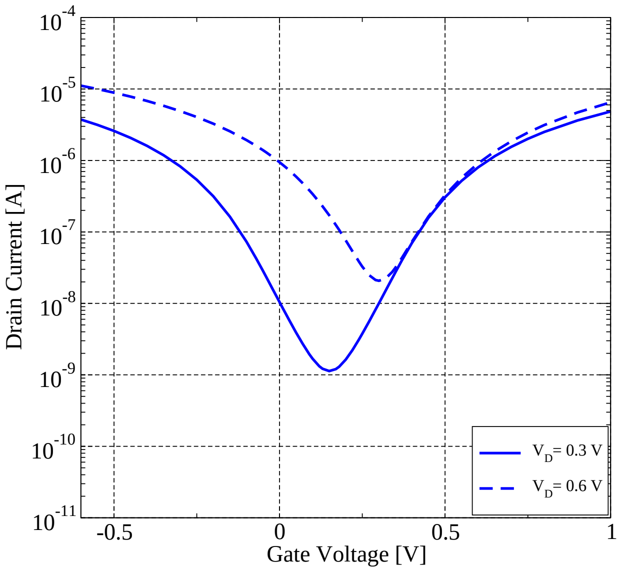

Figure 3. Current-voltage characteristics of the single gate structure.

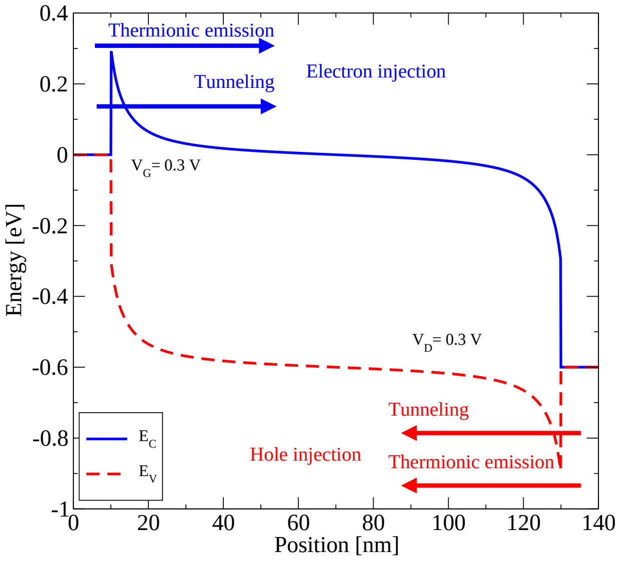

Figure 4. Band edge profile of the single gate structure.

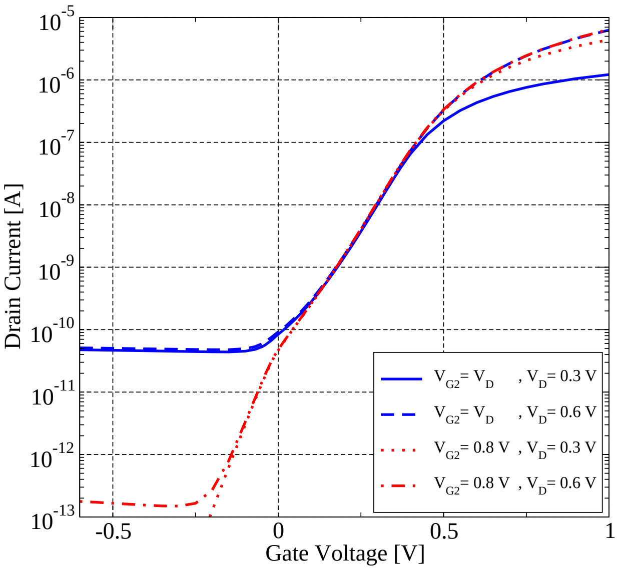

Figure 5. Current-voltage characteristics of the double gate structure.

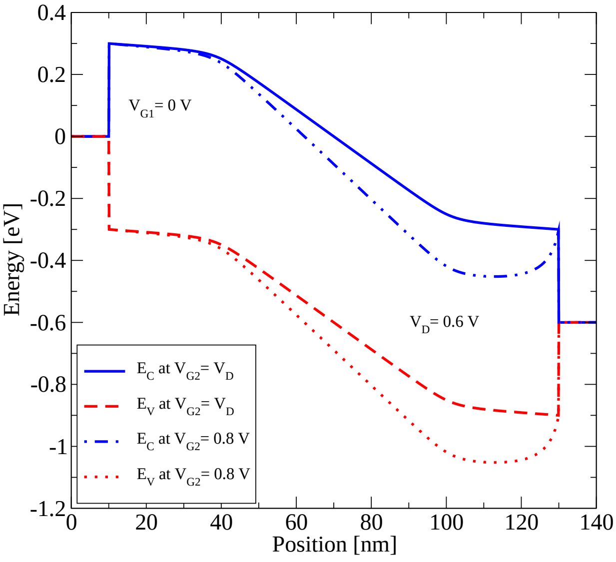

Figure 6. Band edge profile of the double gate structure.

be obtained, but due to the exponential relationship between thermionic emission current and the barrier height the off-current increases exponentially as the drain voltage increases. When the drain voltage reaches the second gate voltage the drain current reaches the limit of the thermionic emission current of holes over the Schottky barrier. If the drain voltage is more increased, the tunneling current of holes also appears. This means that for having an off-current below the thermionic emission limit it is necessary to apply a voltage higher than the maximum drain voltage to the second gate.

In Fig. 5 for the case of $V_{G2} = 0.8$ V a change in the subthreshold slope near zero gate voltage is seen. This phenomenon results from suppressing the thermionic emission current of electrons at the source contact. Since the relationship between the thermionic emission current and the barrier height is exponential, the subthreshold slope in this regime is near its ideal value $70\ \mathrm{mV/dec}$. This behavior is not seen in other current voltage characteristics since in other cases the hole current dominates over the electron current in the off regime. Here, however, the hole current is suppressed and the electron current is the dominant part of the total current.

For a better comparison between these designs current-voltage characteristics of the single gate and the double gate structures are shown in Fig. 7. For the single gate

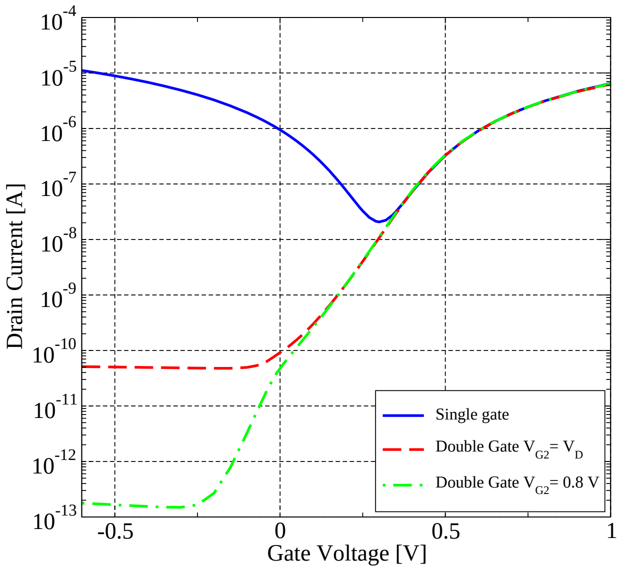

Figure 7. Comparison between current-voltage characteristics of different structures at $V_\mathrm{d} = 0.3\ \mathrm{V}$.

structure the off-current is very high, but for the both double gate structures an $I_\mathrm{on}/I_\mathrm{off}$ ratio higher than five orders of magnitude can be obtained.

4. Conclusions

Our simulation results show that by using a double gate structure the $I_\mathrm{on}/I_\mathrm{off}$ ratio of CNTFETs can be increased considerably. The second gate voltage can be either set to the drain voltage or to a constant voltage higher than the maximum value of the drain voltage. The advantages of connecting the drain voltage to the second gate are avoiding parasitic capacitances between the second gate and the drain, avoiding a separate voltage source for the second gate, and also ease of fabrication. The disadvantage of this method is that the minimum off-current is limited to the thermionic emission current over the Schottky barrier. By applying a constant voltage higher than the maximum value of the drain voltage to the second gate, a very high $I_\mathrm{on}/I_\mathrm{off}$ ratio can be obtained. However, for both of these methods the $I_\mathrm{on}/I_\mathrm{off}$ ratio is higher than five orders of magnitude which is completely satisfactory for conventional logic applications.

5. Acknowledgments

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6. References

[1] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, “Carbon Nanotubes as Schottky Barrier Transistors,” *Physical Review Letters*, vol. 89, no. 10, pp. 106801–4, 2002.

[2] B. M. Kim, T. Brintlinger, E. Cobas, H. Zheng, M. Fuhrer, Z.Yu, R. Droopad, J. Ramdani, and K. Eisenbeiser, “High-Performance Carbon Nanotube Transistors on SrTiO3/Si Substrates,” *Appl.Phys.Lett.*, vol. 84, no. 11, pp. 1946–1948, 2004.

[3] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, “Ballistic Carbon Nanotube Field-Effect Transistors,” *Letters to Nature*, vol. 424, pp. 654–657, 2003.

[4] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. Chan, J. Tersoff, and P. Avouris, “Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes,” *Physical Review Letters*, vol. 87, no. 25, pp. 256805–4, 2001.

[5] J. Appenzeller, J. Knoch, V. Derycke, R. Martel, S.Wind, and P. Avouris, “Field-Modulated Carrier Transport in Carbon Nanotube Transistors,” *Physical Review Letters*, vol. 89, no. 12, pp. 126801–4, 2002.

[6] M. Radosavljevic, S. Heinze, J. Tersoff, and P. Avouris, “Drain Voltage Scaling in Carbon Nanotube Transistors,” *Appl.Phys.Lett.*, vol. 83, no. 12, pp. 2435–2437, 2003.

[7] S. Heinze, J. Tersoff, and P. Avouris, “Electrostatic Engineering of Nanotube Transistors for Improved Performance,” *Appl.Phys.Lett.*, vol. 83, no. 24, pp. 5038–5040, 2003.

[8] S. Heinze, M. Radosavljevic, J. Tersoff, and P. Avouris, “Unexpected Scaling of the Performance of Carbon Nanotube Schottky-Barrier Transistors,” *Physical Review B*, vol. 68, no. 23, pp. 235418–5, 2003.

[9] S. Datta, *Electronic Transport in Mesoscopic Systems*. Cambridge University Press, 1995.

[10] F. Léonard and J. Tersoff, “Novel Length Scales in Nanotube Devices,” *Physical Review Letters*, vol. 83, no. 24, pp. 5174–5177, 1999.

[11] T. Nakanishi, A. Bachtold, and C. Dekker, “Transport Through the Interface Between a Semiconducting Carbon Nanotube and a Metal Electrode,” *Physical Review B*, vol. 66, no. 7, pp. 073307–4, 2002.

[12] J. W. Mintmire and C. T. White, “Universal Density of States for Carbon Nanotubes,” *Physical Review Letters*, vol. 81, no. 12, pp. 2506–2509, 1998.

[13] R. Sabelka and S. Selberherr, “A Finite Element Simulator for Three-Dimensional Analysis of Interconnect Structures,” *Microelectronics Journal*, vol. 32, no. 2, pp. 163–171, 2001.

[14] W. Choi, J. Chu, K. Jeong, E. Bae, and J. Lee, “Ultrahigh-Density Nanotransistors by Using Selectively Grown Vertical Carbon Nanotubes,” *Appl.Phys.Lett.*, vol. 79, no. 22, pp. 3696–3698, 2001.

[15] E. Ungersboeck, A. Gehring, H. Kosina, S. Selberherr, B.-H. Cheong, and W. B. Choi, “Simulation of Carrier Transport in Carbon Nanotube Field Effect Transistors,” *Proceedings ESSDERC 2003*, pp. 411–414, 2003.