Vertically Grown Coaxial Double Gate Carbon Nanotube Field Effect Transistors for Tera Level Integration

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ABSTRACT

Vertically grown carbon nanotubes have the potential for tera-level integration. However, the well-known ambipolar behavior limits the performance of carbon nanotube field effect transistors. In this work we demonstrate that a double gate structure effectively suppresses the ambipolar behavior. Using the double gate design excellent device characteristics along with the potential for high scale integration are achieved, which are necessary for future nanoelectronic applications.

Keywords: ambipolar behavior, double gate device, carbon nanotube field effect transistor

1 Introduction

Exceptional electronic and mechanical properties together with nanoscale diameter make carbon nanotubes (CNTs) a candidate for nanoscale field effect transistors. While early devices have shown poor device characteristics, high performance devices were achieved recently [1]–[5].

Conventional CNTs are grown laterally [6], which is not optimal for high scale integration. A new method has been developed to grow CNTs vertically [7]–[9]. Vertically aligned CNTs are selectively grown in nanoholes formed in anodized alumina oxide (AAO) templates. Each device is formed by a vertical CNT attached to the bottom (source) and upper (drain) electrodes and a gate electrode, which can be integrated in large arrays with the potential for tera-level density (10^{11} cm^{-2}) [7], [8], see Fig. 1. Due to easier fabrication, the top gate structure depicted in Fig. 1-d was used to manufacture device arrays, but because of low coupling between the gate and the CNT, poor device characteristics were achieved [7], [8]. The best coupling between the gate and the CNT can be achieved, if the gate surrounds the CNT. We refer to this structure as coaxial Single Gate (SG) structure. In this work we performed a comprehensive numerical study of this structure. Based on the results we propose a new optimized structure, referred to as coaxial Double Gate structure (DG), so that a high-performance device can be achieved.

2 Modeling

The contact between metal and CNT can be of Ohmic [10], [11] or Schottky type [12], [13]. In this work we focus on Ohmic contact CNTFETs which show better performance than Schottky type devices [14]. In order to account for the ballistic transport we have solved the coupled Poisson and Schrödinger equations [15].

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho}\frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\epsilon} \tag{1}$$

$$-\frac{\hbar^2}{2\mathrm{m}^*}\frac{\partial^2 \Psi^{\mathrm{n,p}}_{\mathrm{s,d}}}{\partial z^2} + (\mathrm{U}^{\mathrm{n,p}} - \mathcal{E})\Psi^{\mathrm{n,p}}_{\mathrm{s,d}} = 0 \tag{2}$$

We have considered an azimuthal symmetric structure, in which the gate surrounds the CNT, such that the Poisson equation (1) is restricted to two-dimensions. In (1) $V(\rho, z)$ is the electrostatic potential, and Q is the space charge density.

In the Schrödinger equation (2) the effective mass is assumed to be $\mathrm{m}^* = 0.06\mathrm{m}_0$ for both electrons and holes [16]. In (2) superscripts denote the type of the carriers. Subscripts denote the contacts, where s stands for the source contact and d for the drain contact. For example, $\Psi^{\mathrm{n}}_{\mathrm{s}}$ is the wave function associated with electrons that have been injected from the source contact, and U^{n} is the potential energy that is seen by electrons. The Schrödinger equation is just solved on the surface of the tube, and is restricted to one-dimension because of azimuthal symmetry.

The space charge density in (1) is calculated as:

$$Q = \frac{\mathrm{q}(p-n)\delta(\rho - \rho_{\mathrm{cnt}})}{2\pi\rho} \tag{3}$$

where n and p are total electron and hole concentrations per unit length. In (3) δ/ρ is the Dirac delta function in cylindrical coordinates. Including the source and drain injection components, the total electron concentration in the CNT is calculated as:

$$n = \frac{4}{2\pi}\int f_{\mathrm{s}}|\Psi^{\mathrm{n}}_{\mathrm{s}}|^2 \mathrm{d}k_{\mathrm{s}} + \frac{4}{2\pi}\int f_{\mathrm{d}}|\Psi^{\mathrm{n}}_{\mathrm{d}}|^2 \mathrm{d}k_{\mathrm{d}} \tag{4}$$

where $f_{\mathrm{s,d}}$ are equilibrium Fermi functions at the source and drain contacts. All our calculations assume a CNT

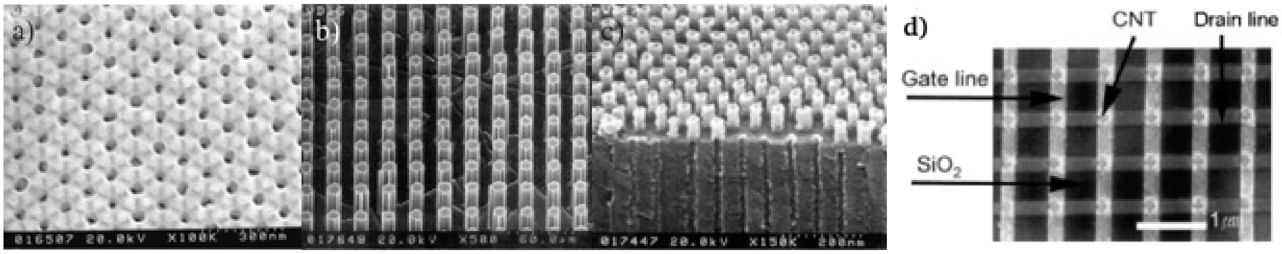

Figure 1: SEM images of a) porous AAO, b) Cross section of nanotube blocks or towers grown selectively, c) Vertically aligned CNTs grown in the patterned nanoprobes. d) Array of top gate devices [7],[8].

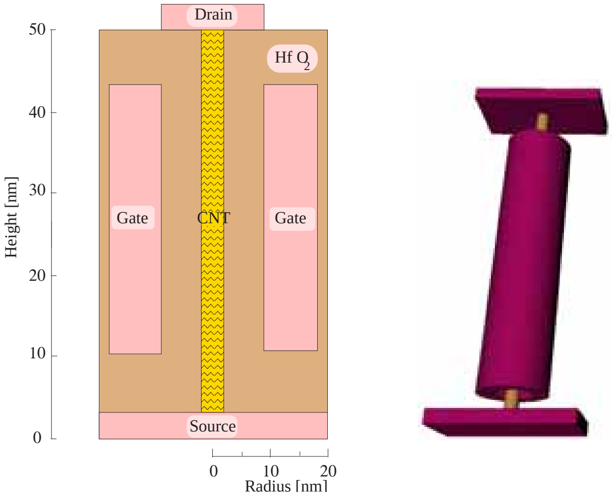

Figure 2: Coaxial SG device.

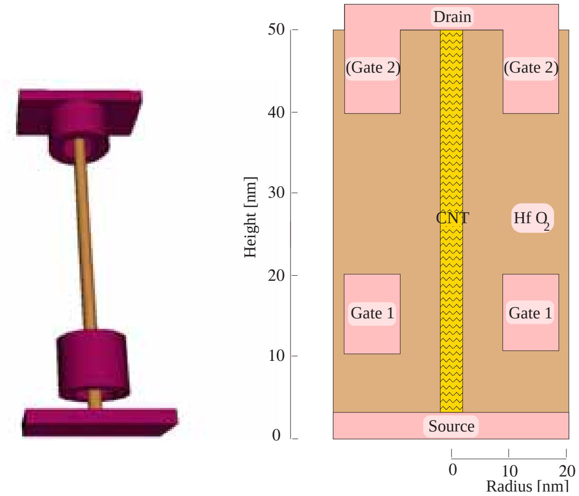

Figure 3: Coaxial DG device.

with 0.5 eV band gap [3]. The total hole concentration in the CNT is calculated analogously. Carriers were taken into account by means of a sheet charge distributed uniformly over the surface of the CNT [15].

The Landauer-Büttiker formula [17] is used for calculating the current:

$$I^{\mathrm{n,p}} = \frac{4\mathrm{q}}{\mathrm{h}} \int [f_{\mathrm{s}}^{\mathrm{n,p}}(\mathcal{E}) - f_{\mathrm{d}}^{\mathrm{n,p}}(\mathcal{E})] TC^{\mathrm{n,p}}(\mathcal{E}) \mathrm{d}\mathcal{E} \tag{5}$$

where $TC^{\mathrm{n,p}}(\mathcal{E})$ are the transmission coefficients of electrons and holes through the device. The factor 4 in (4) and (5) stems from the twofold band and twofold spin degeneracy.

MINIMOS-NT is a semiclassical device simulator [18] which has been enhanced to perform quantum simulations by solving the coupled Schrödinger-Poisson equation system. Conventionally the coupled Schrödinger and Poisson equations are solved iteratively, by using appropriate numerical damping. If a high damping factor is selected the simulations may oscillate and will not converge. Using a low damping factor will also result in long simulation time. To avoid this problem a nonlinear Poisson equation is used. Using this method improved stability and reduced simulation time can be achieved [19].

3 Simulation Results

First we consider a coaxial SG structure in which the gate covers the whole CNT as shown in Fig. 2. Transfer and output characteristics of this structure are shown in Fig. 4 and Fig. 5. The insets in the figures show experimental results [3]. We used the same material and geometrical parameters as reported in [3]. Although unlike the real device a cylindrical symmetry for simulations was assumed, there is a good agreement between simulation and experimental results.

In this type of device holes see no barrier while the barrier height for electrons is $\mathcal{E}_{\mathrm{g}}$. By changing the gate voltage the transmission coefficient of holes through the device is modulated and as a result the total current changes [10]. However the ambipolar behavior of these devices is observed when the drain voltage becomes much higher than the gate voltage, see Fig. 4. Under this situation the barrier thickness for electrons is reduced and the tunneling current of electron increases. The ambipolar behavior is more apparent in Schottky contact devices [20], [21]. The ambipolar behavior limits the performance of the device by decreasing the $I_{\mathrm{on}}/\ I_{\mathrm{off}}$ ratio. To avoid this phenomenon, we propose a coaxial DG structure as shown in Fig. 3. We have previously shown

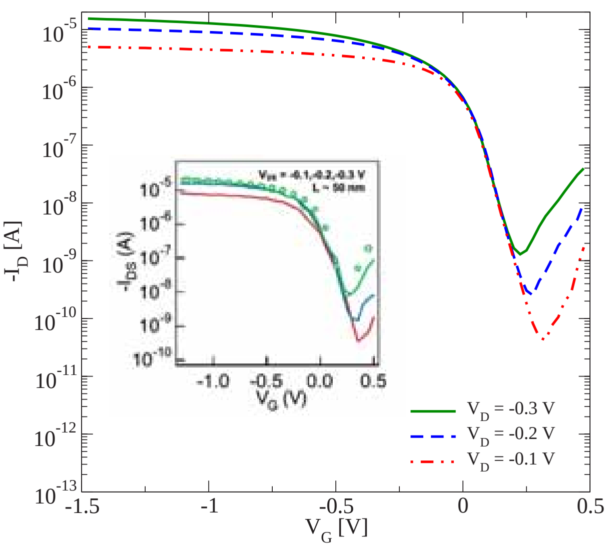

Figure 4: Transfer characteristics of the SG device. Experimental results are shown in the inset.

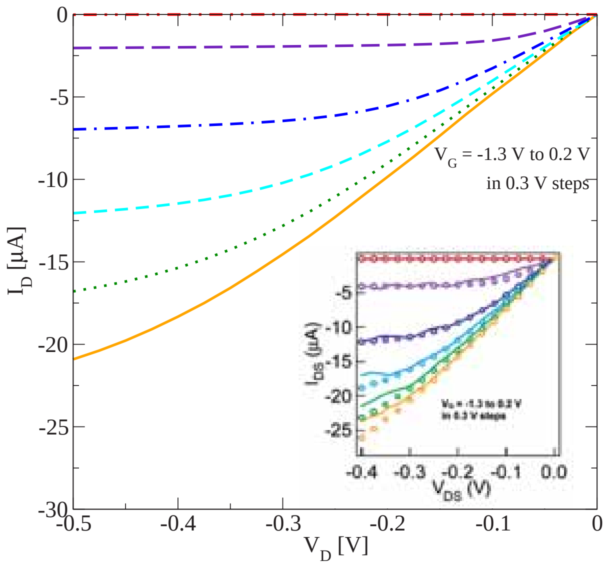

Figure 5: Output characteristics of the SG device. Experimental results are shown in the inset.

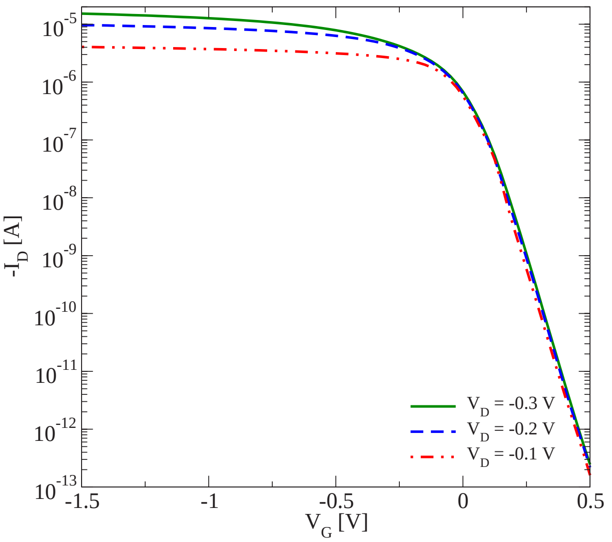

Figure 6: Transfer characteristics of the DG device.

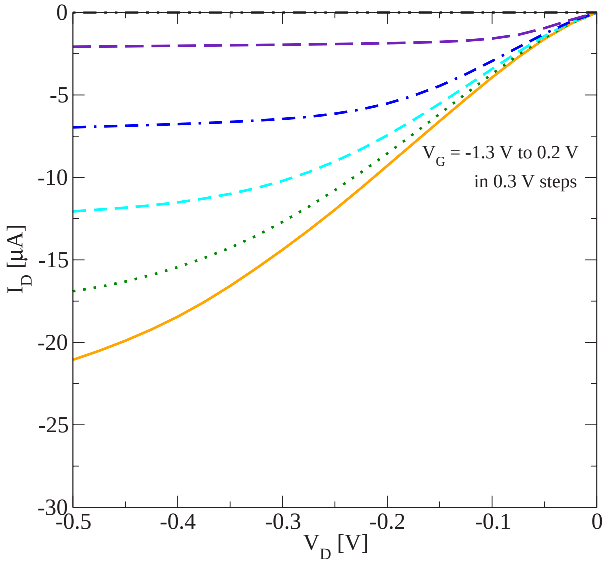

Figure 7: Output characteristics of the DG device.

that this structure suppresses the ambipolar behavior of Schottky contact devices [22]. While the lower gate controls hole injection at the source contact, the upper gate is connected to the drain and controls the band edge profile near the drain contact. If the drain voltage is applied to the upper gate, the band edge profile near the drain contact will be flat at any drain voltage, meaning that the barrier thickness for electrons near the drain contact will not be reduced. In consequence the tunneling current of electrons at the drain contact is suppressed. The same discussion holds for n-type devices. By applying positive voltages to the lower gate, electron injection at the source contact can be controlled and the upper gate suppresses parasitic hole current at the drain contact.

As seen in Fig. 6 and Fig. 7, the proposed DG structure shows improved device characteristics in comparison with the SG structure. Possessing excellent device characteristics and the potential of high-scale integration, the DG structure can be used for device arrays. One advantage of the device array in Fig. 8 is the layered structure. Fabrication of this structure includes the following steps: after covering the vertical CNT with a coaxial gate insulator, different layers are deposited and patterned, starting with inter-metal dielectric between the source and lower gate contacts, the metal layer for the lower gate contact, inter-metal dielectric between the lower and upper gate contacts, and the top metal layer for the upper gate and drain contacts.

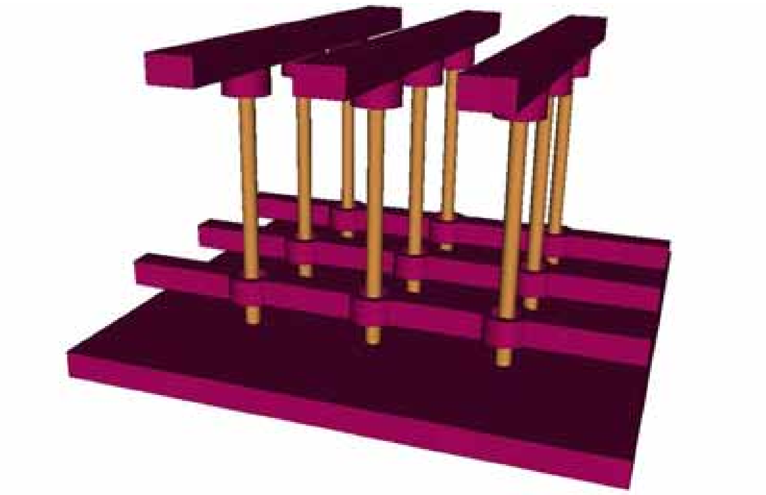

Figure 8: Array of coaxial DG devices.

4 Conclusion

To improve the performance of CNTFETs, the ambipolar behavior of these devices must be suppressed. For this purpose a DG structure is proposed. In the DG structure the first gate controls the carrier injection at the source contact and the second gate controls parasitic carrier injection at the drain contact. The DG structure can be also integrated in device arrays with the potential for tera level integration.

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