Transient Electro-Thermal Investigations of Interconnect Structures Exposed to Mechanical Stress

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ABSTRACT

Investigations of state-of-the-art integrated circuit designs clearly show that the temperature in interconnect structures is becoming the dominant and straitening factor for system performance. In this work we combine three-dimensional transient electro-thermal simulations with a finite element formulation of the thermo-mechanical stress problem in order to study the evolution and development of mechanical stress in complex layered interconnect structures at different operating conditions.

Keywords: Three-dimensional electro-thermal simulation, thermal stress simulation, promoting factors for electromigration, transient simulation, interconnect lines, vias, self-heating

1. INTRODUCTION

The everlasting shrinking of devices requires interconnect layouts which exhibit significant thermal effects. These effects have to be accurately modeled in order to obtain reasonable prediction of the interconnect behavior for the applied electrical, thermal, and mechanical operating conditions. Accordingly, the allowed operating conditions are mainly determined by the reduced electrical reliability of the interconnect structures and of the semiconductor devices due to thermal and mechanical stresses as well as electromigration. These parasitic effects, especially electromigration, have become a serious design challenge for densely packed interconnect lines.

Experimental results report that Joule heating has a strong impact on the range of the maximum allowed temperature of the global lines, despite negligible changes in the chip power density[1]. The existence of high temperature gradients in interconnect structures is known as a significant promoting factor for electromigration[2]. Furthermore, the thermal expansion mismatch between the metal lines and the passivation layer causes mechanical stress which contributes additional electromigration failures[3, 4].

The confinement of the interconnect metal lines by their passivation layers is essential for controlling the characteristics of the thermal stresses and their relaxation behavior. With decreasing line dimensions the confinement effect of the surrounding layers is drastically enhanced, because the passivation layers cannot be shrunk accordingly as the line dimensions do. Therefore, the stress levels increase significantly in the interconnect lines and cause an additional increase of the promoting factor for void formations. The current density becomes more dominated by diffusive ion current which is a net mass flux inside the metalization. This phenomenon starts at the weakest point in the interconnect, mostly at a grain boundary of the interconnect metal and results in migration of the metal atoms from one place to another. With the increasing concentration of tangling bonds (vacancies) caused by missing metal atoms the electrical resistivity increases as well. If the resistivity of an interconnect line exceeds a certain value, for example 120%, the interconnect can be assumed as broken. Thus, the global behavior of the device is changed.

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2. SIMULATION

Since the electrical characteristics of the complete system do not significantly change with stress or other mechanical phenomena occurring during standard operation we can separate the simulation within small time increments into a electro-thermal and a thermo-mechanical part[5, 6]. This assumption holds as long as there is no void nucleation in the interconnect lines, the passivation has not been broken, or the electrical behavior is not dominated by a diffusive ion transport[5].

Therefore, the simulation can be performed in two steps. The first one includes the three-dimensional transient electro-thermal simulation of the interconnect structure in order to calculate the potential and temperature distribution as well as the current density. Subsequently, a three-dimensional thermo-mechanical simulation is performed to obtain the information which is necessary for the investigation of electromigration[6].
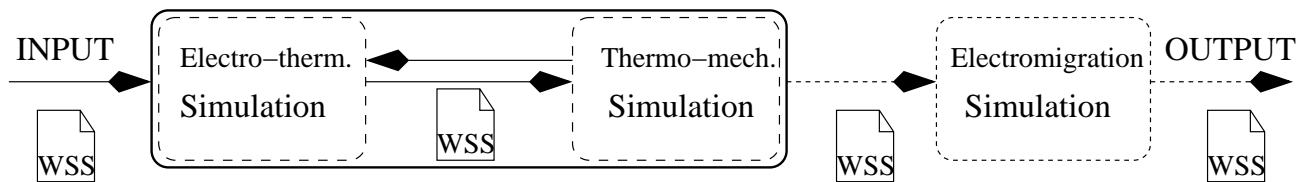
Figure 1: Simulation flow sequence showing the data flow between the simulators and the communication techniques.

Figure 1 shows the complete sequence of the discussed simulation flow and the additional electromigration simulator. At the beginning the electro-thermal simulation is performed which uses a file interface for communication with the thermo-mechanical simulator. After the complete electro-thermal and thermo-mechanical simulation the results are submitted to the electromigration simulator.

The WAFERSTATESERVER (WSS) format for the simulators has been recently developed at the Institute for Microelectronics and is a unified data exchange format for simulators which includes distributed attributes on unstructured two- and three-dimensional meshes, supports different meshes in one file, and allows to specify different boundary conditions.

Since this file format can be used to store different meshes in one file, it can be easily used to couple different simulators, for example the interconnect simulator STAP[7] and the diffusion and oxidation simulator FEDOS[8], which are introduced in the following sections. This file format enables us to use input data generated by different software tools like geometric modeling tools and process simulation tools.

The output of each simulation tool we used for our investigation needs a WSS input file with the geometry of the structure and the boundary conditions as well as a separate configuration file. As a result we obtain a WSS output file which includes the investigated structures, the specified commonly distributed output parameters, and the corresponding meshes for the included attributes.

2.1. Electro-Thermal Model

The three-dimensional simulator STAP from the *Smart Analysis Programs* (SAP)[7, 9] package is able to investigate interconnect structures under different electrical and thermal operating conditions. For the investigations introduced in this work the coupled electro-thermal transient simulation mode was chosen. Typical simulations take a couple of minutes up to an hour, depending on the complexity of the structure as well as the number and the quality of the chosen mesh points.

Therefore, we have to supply the simulator with the appropriate models for the electro-thermal system as well as with the parameters of the different materials.

The transient electro-thermal problem including the self-heating phenomena can be described by the three-dimensional heat conduction equation, the power loss equation, and the Laplace equation[10, 11]:

$$\mathrm{div}\left(\gamma_{\mathrm{T}}(T)\,\mathrm{grad}\,T\right) \;=\; c_{\mathrm{p}}(T)\rho_{\mathrm{m}}\frac{\partial T}{\partial t} - \rho \; , \tag{1}$$

$$\rho \;=\; \gamma_{\mathrm{E}}(T)\|\,\mathrm{grad}\,\varphi\|^2 \; , \tag{2}$$

$$\mathrm{div}\left(\gamma_{\mathrm{E}}(T)\,\mathrm{grad}\,\varphi\right) \;=\; 0 \; . \tag{3}$$

The material specific thermal conductivity is denoted by γ_{T} and the electrical conductivity by γ_{E}, φ the electrical potential, and T the temperature. ρ represents the electrical power loss density, c_{p} the specific heat capacitance, and ρ_{m} the mass density.

As a solution we obtain the time-dependent distributions for the potential and for the temperature in the interconnect lines, the barriers, and in the passivation layers. This resulting temperature distribution is used to set up the mechanical problem described in the following section.

2.2. Thermo-Mechanical Model

The equations for the temperature-dependent stress development due to thermal expansion[12] can be formulated as

$$\sigma_{ij} \;=\; B\alpha(T - T_0)\delta_{ij} + \lambda\varepsilon_{kk}\delta_{ij} + 2\mu\varepsilon_{ij} \; , \tag{4}$$

$$\frac{\partial \sigma_{ij}}{\partial x_j} \;=\; 0 \; , \tag{5}$$

$$\varepsilon_{ij} \;=\; \frac{1}{2}\Big(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\Big) \; . \tag{6}$$

B denotes the bulk modulus, α the thermal volume expansion coefficient, μ and λ are the Lame constants, u_i the components of the local displacement vector $\vec{u}$, and x_i the current position vector $\vec{x}$. ε_{ij} and σ_{ij} are the components of the strain tensor $\tilde{\varepsilon}$ and the stress tensor $\tilde{\sigma}$, respectively.

After finite element discretization we obtain an equation system[13]

$$\mathrm{K}\vec{u} \;=\; \vec{f} \; , \tag{7}$$

$$\vec{f} \;=\; -\mathrm{B}^{\mathrm{T}}\mathrm{D}\tilde{\varepsilon}_0 V \; , \tag{8}$$

$$\tilde{\varepsilon}_0 \;=\; \alpha(T - T_0)\,\mathrm{I} \; , \tag{9}$$

where K denotes the stiffness matrix, $\vec{u}$ the displacement vector, and $\vec{f}$ the force vector. B^{T} represents a geometry matrix and D a material matrix which depends in the elastic case only on Young's modulus and Poisson's ratio[12, 13]. I stands for the identity matrix.

The three-dimensional *Finite Element for Diffusion and Oxidation Simulator* (FEDOS)[8] solves these equations numerically, which takes more time than the electro-thermal simulation. Realistic structures take a couple of hours to simulate with reasonable values for the time steps and mesh points.

Thus, we have a coupling between the STAP program and FEDOS in order to obtain consistent electro-thermal and thermo-mechanical results.
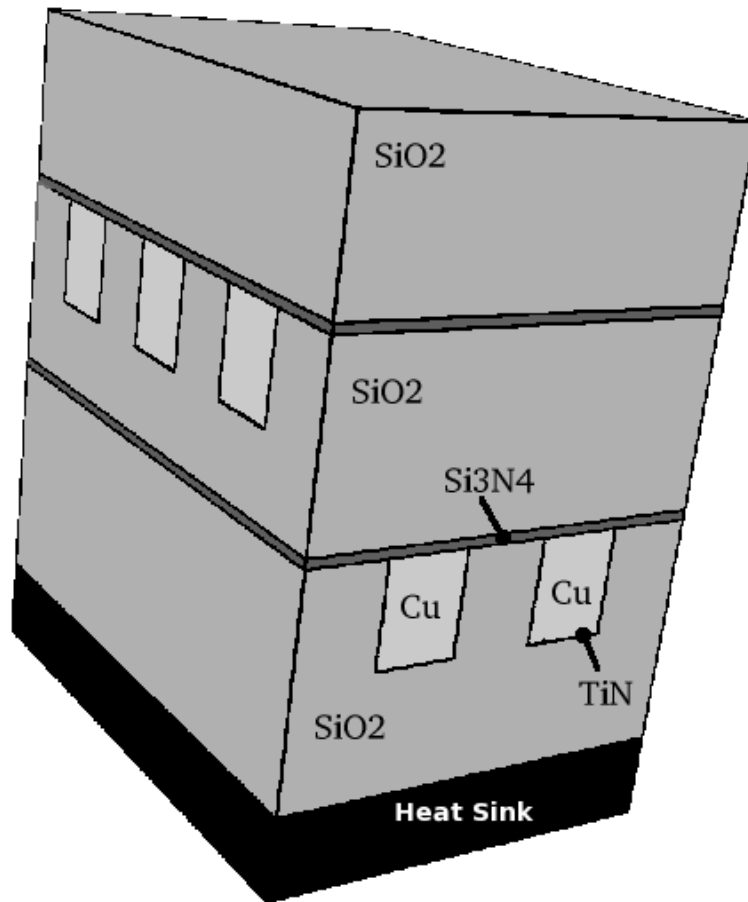
Figure 2: A typical interconnect structure consisting of several metal lines.

2.3. Material Parameters

To set-up the multi-layer interconnect problem the appropriate values for the different material parameters and the desired temperature ranges have to be considered. Due to the a-priori expected high temperature the appropriate values and models for the specific temperature range have to be selected carefully in each simulator.

For the electrical and the thermal conductivities of the different materials the three-dimensional interconnect simulator STAP uses an extended second order polygonal model[7, 11] as given in the following equations.

$$\gamma_{\text{E}}(T) \quad = \quad \frac{\gamma_{0,\text{E}}}{1 + \alpha_{\text{E}}(T - T_0) + \beta_{\text{E}}(T - T_0)^2} \ , \tag{10}$$

$$\gamma_{\text{T}}(T) \quad = \quad \frac{\gamma_{0,\text{T}}}{1 + \alpha_{\text{T}}(T - T_0)} \ . \tag{11}$$

The structure of these formulae is used for both the electrical conductivity $\gamma_{\text{E}}(T)$ and the thermal conductivity $\gamma_{\text{T}}(T)$, where γ_0 is the conductivity at the reference temperature $T_0 = 300\,\text{K}$, α denotes the first order temperature coefficient, and β the second-order temperature coefficient. Depending on the process technology the values can vary by orders of magnitude.

Unknown material parameters can be derived by inverse modeling[14, 15] or parameter extraction[11]. These methods assume a physical or a compact model and specify the unknown parameters as the optimization target.

With a sophisticated optimization and simulation framework like the *Simulation Environment for Semiconductor Analysis* (SIESTA)[16] the optimization can be performed via automatic parameter variation in order to minimize the specified target, for example the mismatch between the simulation result and measurement. Furthermore, a sensitivity analysis[17] can be attached using special features of SIESTA. Additional collections of material parameters can be found in documentations of device and process simulators[7, 18], papers concerning measurements[19, 20], and in databases[21].

In the interconnect simulation package SAP the temperature-dependence of the material specific heat capacitance $c_\mathrm{p}(\tau)$ is modeled using the Shomate equation[22]:

$$c_\mathrm{p}(\tau) = A + B\tau + C\tau^2 + D\tau^3 + \frac{E}{\tau^2} \; , \tag{12}$$

where $\tau = T/1000\,\mathrm{K}$ represents the normalized temperature. The values of the coefficients for the materials in this equation are empirical but well known and confirmed. We have chosen the values mainly from published thermo-chemical tables[21].

3. SIMULATION RESULTS

The electro-thermal simulation has been performed with STAP in the transient electro-thermal mode. The subsequent simulation step for the local stress analysis has been performed with the stress calculation module of FEDOS.

We have investigated the interconnect structure shown in Figure 1 in which the copper interconnect lines are embedded in silicon dioxide SiO_2, silicon nitride Si_3N_4 passivation layers, and titanium nitride TiN barrier layers. The lower and the upper interconnect lines are connected with vias in the middle of the structure. Also these vias consist of copper Cu and the corresponding barrier of titanium nitride TiN at the interfaces between copper and every other material. On the bottom is a heat sink (bulk silicon), which is stabilized at a constant temperature[23] ($T = 330\,\mathrm{K}$).

For the electrical boundary conditions we have applied positive voltages at the lower copper lines which are switched on at the beginning of the simulation time ($t = 0$). At the upper metal lines we have applied zero bias.

The temperature distribution for the materials SiO_2 and Si_3Ni_4 at $t = 25\,\mu\mathrm{s}$ is depicted in Figure 3. This temperature distribution is mainly determined by Joule heating of the interconnect lines. This figure shows only the passivation layers' silicon oxide, silicon nitride, and titanium nitride, because the temperature gradient inside the copper line is negligible compared to the gradients in the other materials.

Figure 3 shows large temperature gradients in SiO_2 between the lower lines of the interconnect. Between the upper copper lines and the top above the upper interconnect lines there is only a small temperature gradient. This phenomenon results from the high thermal conductivity of copper compared to all other materials used in this structure. The thermal conductivity in copper is twice as large as the thermal conductivity in aluminum. Moreover, the simulations show that Joule heating has a stronger impact on the temperature distribution as previously expected from the well-known data from aluminum interconnects.[11]

Using this resulting temperature distribution we can determine the distribution of the pressure in order to obtain the corresponding hydrostatical stress distribution caused by self-heating of the interconnect lines. We have to calculate the pressure by the following equation[12]:

$$p = -\frac{\mathrm{trace}[\sigma]}{3} = -\frac{\sigma_{11} + \sigma_{22} + \sigma_{33}}{3}. \tag{13}$$
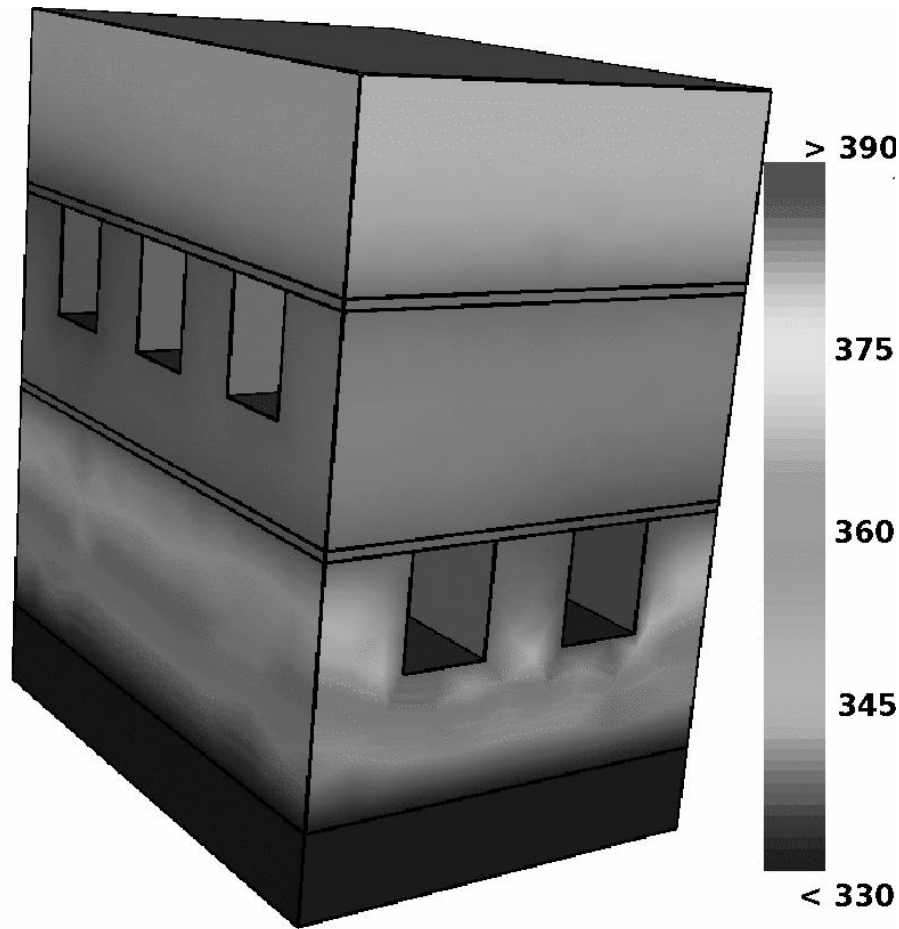
Figure 3: The temperature distribution [K] in the barrier TiN, the passivation layers SiO_2, and Si_3Ni_4. The large temperature gradients near the lower metal lines result from the temperature difference between the heat sink and the self-heated metal lines.

We obtain the pressure distribution inside the interconnect lines which is shown in Figure 4. As expected, the areas with the highest peak values are located either at edges of the surface, at material interfaces inside the interconnect, or at locations where the current density exhibits large gradients.

Over wide ranges in the interconnect materials we have an expanding behavior of the interconnect metal and therefore a positive, compressive pressure which is quite small compared to the peak values in the vias. At the regions of the critical parts like vias and edges of the interconnect structure we can see a compressive behavior as shown in Figure 4. The pressure reaches large values at the well-known high risk areas. This phenomenon can be explained by the different thermal expansion coefficients of the materials used in this structure.

4. CONCLUSION

We demonstrated the coupling of three-dimensional transient electro-thermal simulations with self-heating and three-dimensional thermo-mechanical simulation for a realistic interconnect structure. Thereby we obtained the appropriate input data for the analysis of electromigration in order to reasonably estimate reliability and to construct interconnect design rules.
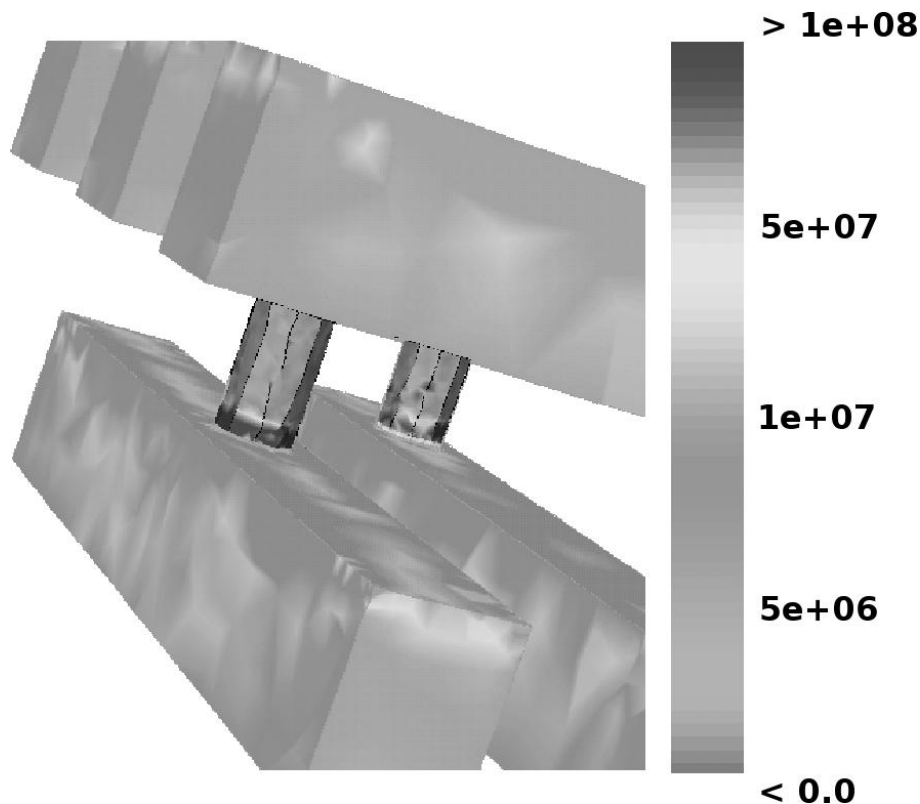
Figure 4: The pressure distribution [Pa] in the interconnect lines and vias shows large gradients at the material interfaces. The regions most affected are the bottom of the vias.

The results from Figure 4 show that a peak pressure is generated at the bottom of the copper interconnect vias, which depicts this area as the one with the highest risk for electromigration.

The vias in general and the edges of interconnect are also highly stressed due to the temperature increase during operation via Joule heating and the stress induced due to the thermal mismatch of the interconnect materials which is caused by the temperature gradient and the different thermal volume expansion coefficients. In addition, also areas with high current densities have to be considered. In combination with large temperature gradients these areas show also large vacancy concentrations due to high ion current densities[5] which cause a higher mass flux of copper atoms and therefore also an increase of one of the promoting factors for electromigration.

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