A Method for Generating Structurally Aligned Grids for Semiconductor Device Simulation

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***Abstract*—The quality of the numeric approximation of the partial differential equations governing carrier transport in semiconductor devices depends particularly on the grid. The method of choice is to use structurally aligned grids since the regions and directions therein that determine device behavior are usually straightforward to find as they depend on the distribution of doping. Here, the authors present an algorithm for generating structurally aligned grids including anisotropy with resolutions varying over several orders of magnitude. The algorithm is based on a level set approach and permits to define the refined resolutions in a flexible manner as a function of doping. Furthermore, criteria on grid quality can be enforced. In order to show the practicability of this method, the authors study the examples of a trench gate metal–oxide–semiconductor field-effect transistor (TMOSFET) and a radio frequency silicon-on-insulator lateral double diffused metal–oxide–semiconductor (RF SOI LDMOS) power device using the device simulator MINIMOS NT, where simulations are performed on a grid generated by the new algorithm. In order to resolve the interesting regions of the TMOSFET and the RF SOI LDMOS power device accurately, several regions of refinement were defined where the grid was grown with varying resolutions.**

***Index Terms*—Grid generation, level set method, semiconductor device simulation, structurally aligned grids.**

I. Introduction

THE QUALITY of the numeric approximation of the solution of semiconductor device equations by the finite-element or the finite-volume method is governed by the quality of the underlying mesh, and thus structurally aligned grids are a crucial premise for accurate device simulation. In addition to aligning the meshes within the structures, it is also desirable to enforce quality criteria like the Delaunay criterion or the minimum angle criterion [1].

In this paper, a new method for generating structurally aligned triangulations, including anisotropy if desired, is presented. The main idea is to first construct a suitable unconnected set of edges by advancing a front through the simulation domain using a level set algorithm. After extracting and reworking the boundaries, these edges are used in the second step as the input to a specialized grid generator that enforces the quality criteria. Although a technique based on the level set method has been used for generating structurally aligned grids [2], that method cannot generate anisotropic grids and no condition concerning the quality of the grid, e.g., minimum angles or the Delaunay criterion, can be guaranteed. However, the approach outlined above has been successfully applied to semiconductor device simulation using the generated grids and the simulator MINIMOS NT [3].

The partial differential equations that have to be solved in order to simulate charge transport in semiconductor devices are discussed in Section II and will be used for the presented examples. If the dependence of the solution on the doping and the operating conditions can be estimated in advance, the grid can be suitably constructed before attempting the numerical solution.

After the description of the grid generation algorithm in Section III, it is applied to two examples—which are interesting by themselves—in order to show that the method is applicable to real world tasks.

The first example, in Section IV, is a trench gate metal–oxide–semiconductor field-effect transistor (TMOSFET). TMOSFETs are useful for power switching at high voltages [4]–[8]. They also provide advantages because of their geometric layout, i.e., because their inversion and accumulation channel regions are perpendicular to the wafer surface. Hence, they enable to maximize the ratio of cell perimeter to area and thus to increase packing density. The TMOSFET considered is a 120-V trench gate U-shaped MOS (UMOS) transistor (cf. Fig. 2). After generating the structurally aligned grid, the authors present the simulated characteristics.

The second example, in Section V, is the simulation of a radio frequency silicon-on-insulator lateral double diffused metal–oxide–semiconductor (RF SOI LDMOS) power transistor. Here, several areas of refinement were chosen and the grid was generated to take the specific structure of the device and location of the junctions into account. SOI is a promising technology for the monolithic integration of digital, analog, and RF devices. The reduced capacitance and the low leakage current of SOI devices are highly desirable characteristics for RF power applications. Here, the two-dimensional (2-D) device simulation of a 110-V RF SOI lateral double diffused MOSFET (LDMOSFET) is presented.

II. Semiconductor Equations

The basic semiconductor equations [9]–[11] are the Poisson equation and the continuity equations for electrons and holes, i.e.,

$$\nabla(\epsilon\nabla\psi) = q(n - p - C)$$
$$\nabla J_n = q\left(R + \frac{\partial n}{\partial t}\right)$$
$$\nabla J_p = -\,q\left(R + \frac{\partial p}{\partial t}\right).$$

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The unknown quantities are the electrostatic potential ψ and the electron and hole concentrations n and p. C denotes the net concentration of the ionized dopants, ϵ is the dielectric permittivity of the semiconductor, and R is the net recombination rate.

The default carrier transport model in MINIMOS NT [3] is the drift diffusion model that will be used in the following. However, all the considerations are also valid for the hydrodynamic model. The drift diffusion current relations can be derived from the Boltzmann equation by the method of moments. The electron and hole current densities are given by

$$J_n = q\mu_n n \left(\nabla\left(\frac{E_C}{q} - \psi\right) + \frac{k_B T_L}{q}\frac{N_{C,0}}{n}\nabla\left(\frac{n}{N_{C,0}}\right)\right)$$
$$J_p = q\mu_p p \left(\nabla\left(\frac{E_V}{q} - \psi\right) + \frac{k_B T_L}{q}\frac{N_{V,0}}{p}\nabla\left(\frac{p}{N_{V,0}}\right)\right).$$

These current relations account for position-dependent band edge energies, E_C and E_V, and position-dependent effective masses, which are included in the effective density of states, $N_{C,0}$ and $N_{V,0}$. The index 0 means that $N_{C,0}$ and $N_{V,0}$ are evaluated at an arbitrary and constant reference temperature.

Some of the main difficulties in the numerical treatment of these equations are the very large differences in the magnitudes of the involved variables. Because of these differences, the drift diffusion equations show an almost singular type of behavior and can be treated well by singular perturbation analysis [10]. It is known that the solutions of the drift diffusion equations exhibit an extreme layer structure, i.e., they show locally large gradients [12]. The steep gradients occur locally across p–n junctions and in channel regions, e.g., in the narrow regions underneath semiconductor–oxide interfaces. If a numerical method is adapted to this layer behavior, its performance can be drastically improved [10, Ch. 3].

This information about the layer structure of the solutions is vital when generating grids from *a priori* information. In contrast, grid refinement techniques are of course based on *a posteriori* information from error estimators. The solutions of the device equations depend on the location of the junctions, the iso-lines and the distribution of the doping, and the operating conditions. Because of the layer behavior in the vicinity of junctions, the grid can be suitably constructed for certain operating conditions based on the extracted iso-lines before attempting the numerical solution.

This procedure will be described in the next section. The solutions of the hydrodynamic model are similar to those of the drift diffusion equations concerning the previous argument, although additional refinement may be beneficial to accurately model carrier temperatures. Thus, the demands on grid generation are similar when solving the hydrodynamic semiconductor equations.

III. Grid Generation Method

In this section, the details of the algorithm devised for generating structurally aligned grids are presented after an overview of the level set method in two spatial dimensions [13]–[16].

In recent years, the level set method has received lots of attention as a means for tracking moving boundaries in areas like semiconductor process simulation, fluid dynamics, computational geometry, image enhancement and noise removal, shape detection and recognition, and electromigration. The main advantages of the level set method are the fine resolution that can be achieved, which is much finer than the resolution of the grid on which the level set equation is solved, and the precise and straightforward calculation of surface normals. Furthermore, joining surfaces are handled implicitly by the algorithm.

The idea behind all level set algorithms is to represent the curve or surface in question at a certain time t as the zero level set (with respect to the space variables) of a certain function $u(t, \mathbf{x})$, the so-called level set function. Thus, the initial surface is the set $\{\mathbf{x} | u(0, \mathbf{x}) = 0\}$. The speed of a point on the surface normal to the surface is called the speed function $F(t, \mathbf{x})$. For points on the zero level set, it is usually determined by physical models.

The surface at a later time t_1 is also the zero level set of the function $u(t, \mathbf{x})$, namely $\{\mathbf{x} \in \mathbb{R}^n | u(t_1, \mathbf{x}) = 0\}$. This leads to the level set equation

$$u_t + F(t, \mathbf{x})\|\nabla_{\mathbf{x}} u\| = 0$$
$$u(0, \mathbf{x}) = u_0(\mathbf{x}) \quad \text{given}$$

in the unknown variable u, where $u(0, \mathbf{x})$ determines the initial surface. Having solved this equation, the zero level set of the solution is the sought curve or surface at all later times. This equation relates the time change to the gradient via the speed function.

In the first step, the level set function must be initialized to the signed distance function. Since the level set algorithm will later work only in a narrow band around the current zero level set, it is sufficient to perform the distance calculations near the initial boundary. This can be achieved, e.g., by a recursive algorithm walking along the boundary.

In the numeric application, the level set function is represented by values on grid points. In order to find the coordinates of the current boundary, the surface must be extracted from this grid using linear interpolation.

A second-order space convex finite-difference scheme [17]–[20] was used in this paper to solve the level set equation. The spatial and temporal discretization steps Δx, Δy, Δz, and Δt are connected via a Courant–Friedrichs–Levy (CFL) condition that demands that the front must not cross more than one grid cell in each time step and ensures the stability of the scheme. The CFL condition is an information theoretic one and is fundamental in the sense that it is not affected by the choice of the numeric method, be it finite differences or finite elements, etc. The CFL condition requires that

$$\Delta t \max_{\text{domain}(F)} F \leq \min(\Delta x, \Delta y, \Delta z).$$

Advanced topics are narrow banding and extending the speed function from values at the boundary to the whole narrow band. The combination of these two concepts was described in [21]. The benefit of this algorithm is that it renders reinitialization superfluous. Frequent reinitialization that would be necessary

otherwise is generally considered critical since it introduces inaccuracies [22].

For generating grids, the underlying idea is to advance one or more fronts through the simulation domain using a level set algorithm and constant speed functions. For each moving front, a certain number of boundaries are extracted and reworked. The number of these front boundaries and the spacing between them can be arbitrarily defined and depend on the number of advancing level set steps and their time steps. Clearly, the spacing between the intermediate boundaries obtained by the level set algorithm will later determine the diameters of the triangles of the final grid.

Since the boundary segments of the intermediate boundaries obtained after surface extraction from the rectangular grid may be arbitrarily small, the boundary segments must be normalized. The segments are normalized by choosing points on the boundary that are equidistant when their distance is measured along the boundary. The normalized intermediate boundaries consist of straight lines that are the edges of the final grid to be respected in the second part of the algorithm. This first part of the grid generation is highly customizable and anisotropy can be introduced here by choosing the spacing between the intermediate boundaries and the distance between points of the normalized boundary accordingly.

For semiconductor device simulation, the direction of alignment is generally chosen along junctions. The distance between the parallel front boundaries is approximately proportional to the logarithm of the amount of doping, and if the doping is below a limit no special edges are prescribed.

In the second part of the algorithm, the set of edges constructed in the first part serves as input to the actual grid generator. The TRIANGLE program [23], [24] was used in this paper. It is written in C and computes 2-D Delaunay triangulations exactly. The minimum angle criterion is obeyed using a refinement algorithm for quality mesh generation [25] that allows to produce meshes with no small angles while using relatively few triangles. The mesh density can be increased if desired. After reworking the edges into the appropriate input format and running TRIANGLE, the output is translated into program information file (PIF) files [3] suitable for MINIMOS NT.

The benefits of this algorithm can be summarized as follows. The grid resolution is customizable and the areas of higher resolution can be chosen arbitrarily. The grid resolution may vary over several orders of magnitude. The algorithm can deal with arbitrary initial structures and an arbitrary number of starting fronts defining areas of high resolution. Anisotropy may be introduced by choosing appropriate parameters for the algorithm. At the same time, quality criteria like the Delaunay criterion and requiring that all angles of the triangulation are larger than a certain minimum angle are enforced. It is important to note that the algorithm works reliably since it is based on edges in contrast to just prescribing sets of points, and hence directional information is preserved.

In [26], a different approach to grid generation using a level set algorithm was presented. Previous work along these lines includes [27] and [28]. Compared to grid generation algorithms using iso-lines or iso-surfaces of solutions of a Poisson equation [29], the advantage of this algorithm is its flexibility. This is important, e.g., near the buried layers of silicon-on-insulator (SOI) devices. The initial boundaries where the advancing fronts start and the prescribed number of intermediate boundaries and their spacing determine the properties of the final grid in a straightforward manner in contrast to the Poisson equation approach.

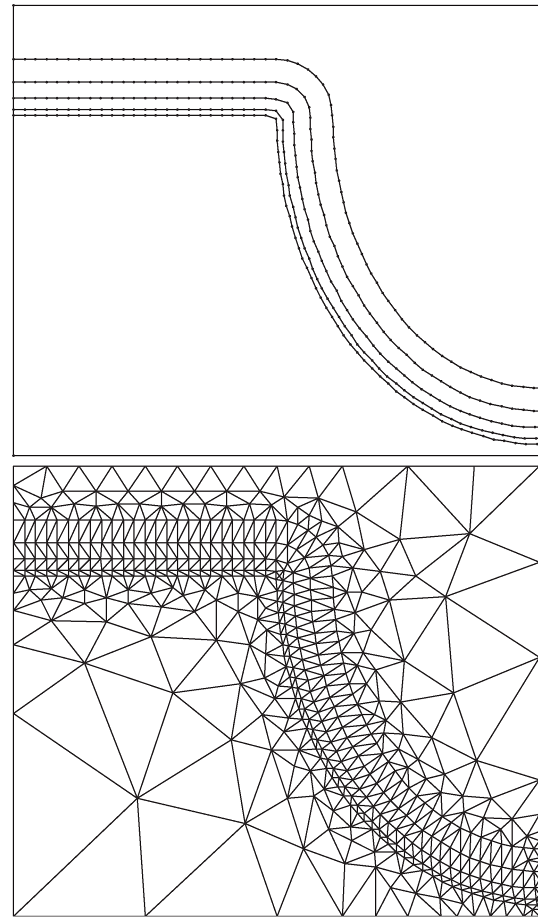

Fig. 1. Two main steps of the grid generation method: building parallel boundaries and finding a Delaunay triangulation.

Fig. 1 depicts an example. The first image shows the boundaries obtained by moving the bottom line using the level set algorithm and normalizing the length of the individual segments. The second image shows the final grid respecting the prescribed segments. Anisotropy is introduced by varying the distance between the boundaries. In the next section, two real world device simulation examples will be investigated.

IV. Grid Generation for a TMOSFET

The device structure of the trench gate UMOS transistor is shown in Fig. 2 and its parameters in Table I. Its trench depth is 3 μm and its gate oxide thickness is 0.1 μm. It is designed to achieve a forward blocking voltage of 120 V.

A. Grid Generation

For grid generation, the authors used four boundaries following the three junctions (cf. Fig. 2) and one in the p region

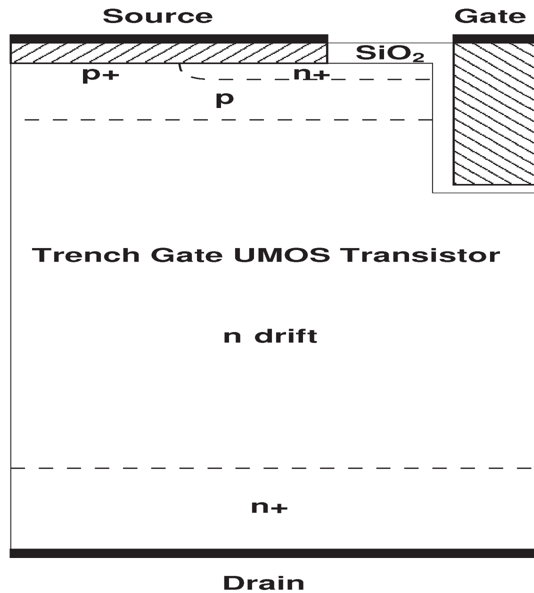

Fig. 2. Structure of the TMOSFET. The half cell pitch of the device is 2.5 μm and its n drift length is about 9.5 μm.

TABLE I
TECHNOLOGICAL AND GEOMETRICAL PARAMETERS CONSIDERED OF THE TMOSFET

Parameter	Value
n drift doping	1.5×10^{15} cm^{-3}
p well doping	1×10^{17} cm^{-3}
p well	$\approx$1.4 μm
p^+ buffer	5×10^{18} cm^{-3}
n^+ source depth	$\approx$0.38 μm
Gate oxide thickness	0.1 μm
Trench depth	3 μm
n drift length	$\approx$9.5 μm

near the gate oxide. First, at the n^+–p junction, the authors used three boundaries in each direction of the initial boundary following the junction with a distance of 0.02 μm between any two adjacent boundaries.

At the p–n junction, the authors used one boundary above and below the initial boundary and a distance of 0.02 μm. At the n–n^+ junction in the lower part of the device, the authors constructed two boundaries with a distance of 0.5 μm going downwards from the initial boundary following the junction. For the last prescribed edges, the authors started at the right hand side of the p region and moved to the left constructing three boundaries at a distance of 0.005 μm.

In the second step, the authors used the TRIANGLE program requiring a minimum angle of 25° with these prescribed edges as input. The grid produced two enlargements that are shown in Figs. 3 and 4. The junction areas are resolved very finely as demanded.

B. Device Simulation

The device simulations were performed using MINIMOS NT [3]. Fig. 5 shows typical on-state characteristics of the high voltage TMOSFET. The *I–V* curves of the figure show that good saturation current behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Fig. 6 for drain voltages of $V_d = 0.1$ V and 0.5 V. From this figure, a threshold voltage V_T of 2.5 V is obtained. It is important to note that the threshold voltage is independent of the drain voltage.

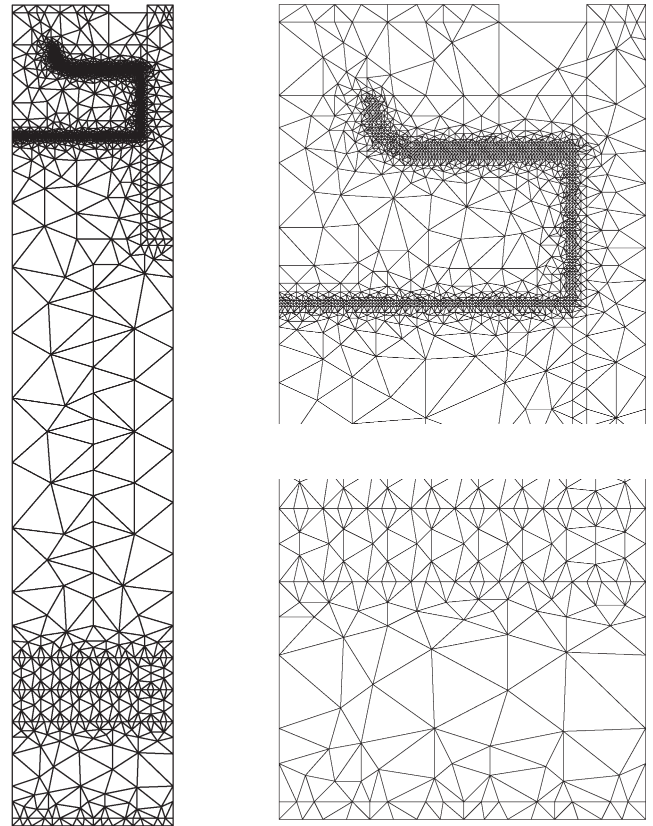

Fig. 3. Grid generated for the device in Fig. 2. Two enlargements are shown on the right hand side.

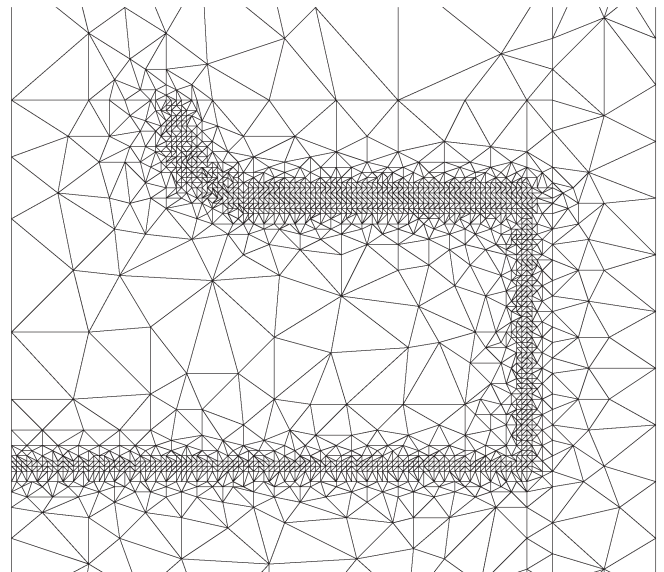

Fig. 4. Enlargement of the grid shown in Fig. 3.

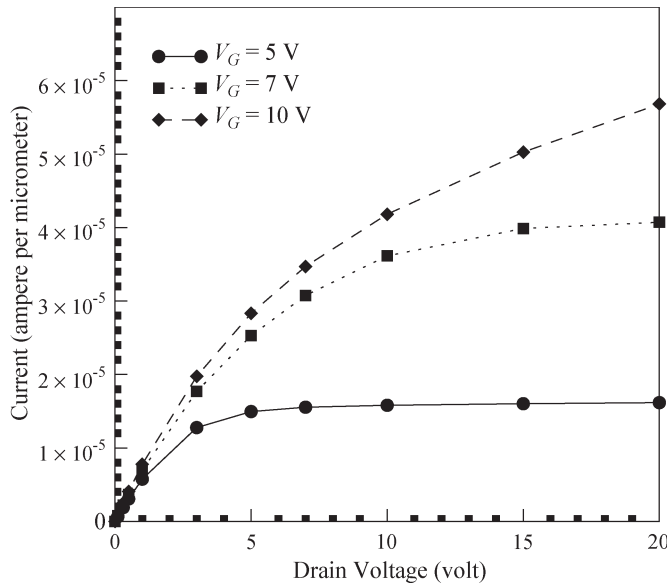

Fig. 5. On-state characteristics of the vertical TMOSFET for gate voltages of 5, 7, and 10 V.

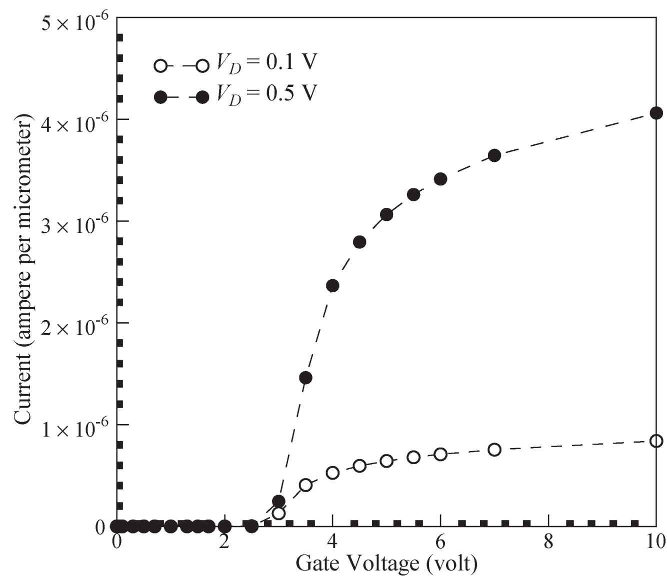

Fig. 6. Transfer characteristics of the high voltage TMOSFET for drain voltages of 0.1 and 0.5 V.

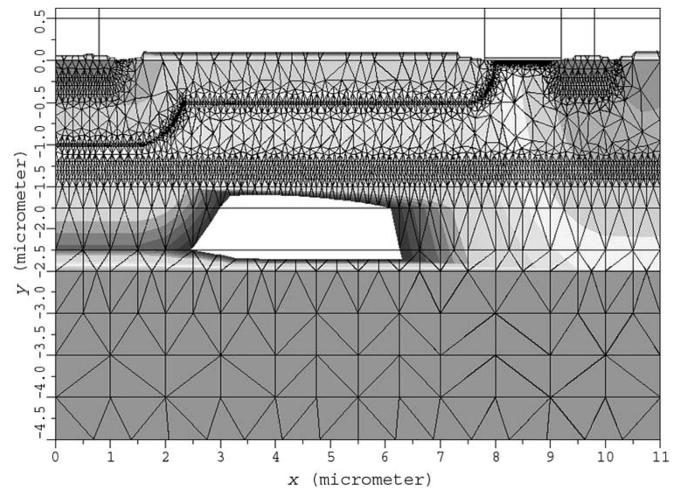

Fig. 7. Structure of the RF SOI LDMOS power transistor and the generated grid.

TABLE II
TECHNOLOGICAL AND GEOMETRICAL PARAMETERS OF THE RF SOI LDMOS POWER TRANSISTOR. THE LATERAL FACTOR OF ALL GAUSSIAN PROFILES IS 0.8

Parameter	Value
n drift length	6 μm
n drift doping (P)	3×10^{16} cm^{-3}
SOI thickness	15 μm
p epi doping (B)	1×10^{14} cm^{-3}
p+ buffer doping (B)	5×10^{18} cm^{-3}
p body doping (B)	7×10^{17} cm^{-3}
Sub doping (P)	1×10^{18} cm^{-3}
SiO_2 layer thickness	1 μm

V. Grid Generation for an SOI Power Device

The device structure of the RF SOI LDMOS power transistor is shown in Fig. 7 and its parameters in Table II. It is designed to achieve a forward blocking voltage of 110 V with an SOI thickness t_{soi} of 1.5 μm and with a buried oxide thickness t_{ox} of 1.0 μm. The doping of the device is given by analytic functions or, more precisely, Gaussian profiles (cf. Table II).

A. The Grid Generation

For the grid generation, the authors used six boundaries following four junctions (cf. Fig. 7), one in the channel and one at the silicon–insulator interface. First, at the p–body–n+ junction, the authors used one boundary in each direction of the initial boundary following the junction with a distance of 0.1 μm between any two adjacent boundaries.

Second, at the n–drift–p–epi junction, the authors used one boundary above and below the initial boundary and a distance of 0.02 μm. Third, at the n–buff–p–epi junction, the authors constructed one boundary above and below a distance of 0.02 μm. For the last junction boundary, the n+–n–buff boundaries, again one boundary above and below at a distance of 0.1 μm, were used.

In the channel region, the authors started at the interface and moved down constructing four boundaries at a distance of 0.005 μm. For the last prescribed edges, the authors started at the boundary between the silicon and the silicon dioxide layers and moved up and down at a distance of 0.1 μm.

Again, the final grid was obtained by TRIANGLE starting from these prescribed edges. The minimum required angle was 20°. The final grid is shown in Fig. 7 and an enlargement in Fig. 8.

B. Results and Discussion of Device Simulation

The optimum drift length and the doping concentration are considered by the reduced surface field (RESURF) principle. With the proposed grid generation algorithm, mesh structures suitable for device simulation can be obtained along the junctions (parallel to the junction) and at the buried oxide interface.

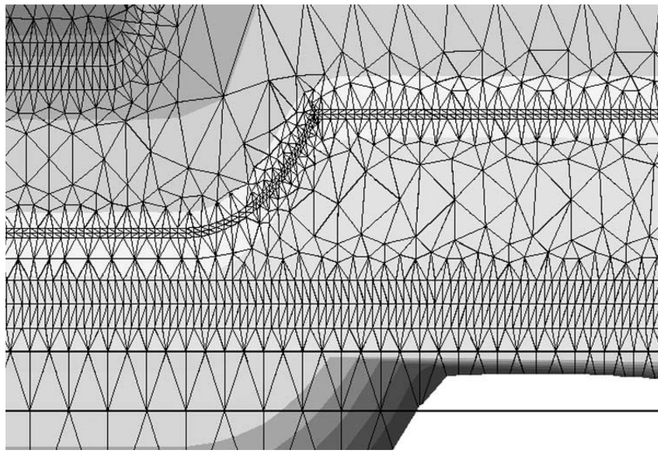

Fig. 8. Enlargement of the drain region (left) from Fig. 7.

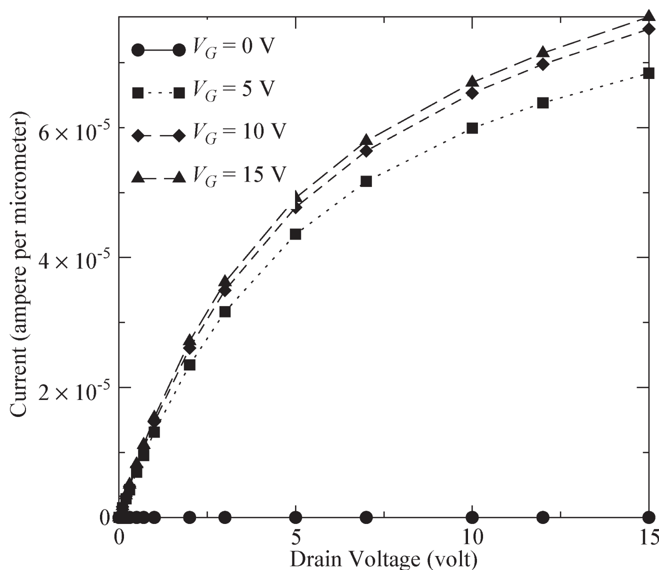

Fig. 9. On-state characteristics of the RF SOI LDMOS power transistor for gate voltages of 5, 10, and 15 V.

Again, the typical on-state characteristics were obtained using MINIMOS NT and are shown in Fig. 9. The *I–V* curves imply that good saturation current behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Fig. 10 for drain voltages of $V_d = 0.1$ V and 0.5 V. From this figure, a threshold voltage V_T of 1 V is obtained.

To validate these simulation results, they were compared to those obtained by Dessis using a very fine grid. Matching results were found and the same saturation behavior was obtained.

VI. Conclusion

A new method for generating structurally aligned grids and guaranteeing quality criteria on the triangulation was presented. It provides lots of flexibility, since the resolution and anisotropy of the grid are customizable and the diameter of the triangles may vary over several orders of magnitude within one simulation domain. Compared to the approach of using iso-

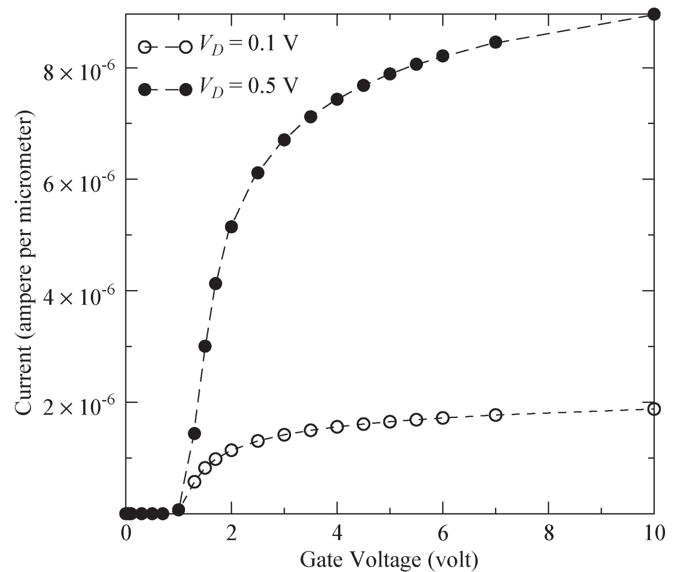

Fig. 10. Transfer characteristics of the RF SOI LDMOS power transistor for drain voltages of 0.1 and 0.5 V.

lines or iso-surfaces of solutions of a Poisson equation [29], this method allows to propagate several fronts through the simulation domain and thus to tailor the areas of high resolution precisely and in a straightforward manner.

Hence, it is well suited for semiconductor device simulation and especially, e.g., for the simulation of SOI devices, where high resolution is required in the vicinity of the buried layer.

Furthermore, the algorithm is robust since the generation of the final triangulation is based on edges that have to be respected (and not on single points). Finally, the grids generated satisfy the Delaunay criterion and the minimum angle criterion that ensures high grid quality with respect to numeric properties.

In two examples, the constructed meshes were used to obtain on-state and transfer characteristics. The grids generated for the nontrivial geometries of these devices increased the speed and accuracy of the simulations.

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