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Methodologies and Scientific Issues for the Modeling of Advanced Semiconductor Devices

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The breathtaking increase in computational power and speed of integrated circuits in the past decades has been supported by the aggressive size reduction of semiconductor devices. This trend is expected to continue in the coming decade as predicted and institutionalized by the International Technology Roadmap for Semiconductors, cf. <http://public.itrs.net>.

Today, when the so-called 90 nm technology node with physical transistor gate lengths in the range of 40 nm is in mass production, the challenge is to introduce the 65 nm technology node already within a year. A new technology node is expected to be introduced every 3 years, with a long-term projection of the 22 nm node to be in mass production by the year 2016. A possibility to build metal-on-insulator field effect transistors (MOSFETs) with even shorter gate lengths has been successfully established after the 6 nm gate length transistor has been demonstrated in various research laboratories. From a theoretical viewpoint even a few nm gate length device has been predicted to be functional.

Nevertheless, emerging outstanding technological challenges related to different aspects of MOSFET fabrication and reliability in mass production, as well as the rapidly increasing power dissipation may slow down the so far exponential scaling of Complimentary MOSFETs (CMOS). Besides, with the ongoing search for new technological solutions vital for CMOS downscaling, developing conceptually new devices and architectures is becoming increasingly important. New nano-electronic structures, such as carbon nano-tubes, nano-wires, and molecules, are considered to be the most prominent candidates for the post-CMOS era. Since conventional MOSFETs are already operating in the sub-100 nm range, new nano-electronic devices are expected to complement and substitute some of the current CMOS functions after being integrated into CMOS technology.

Technology CAD (TCAD) tools are designed to assist in development and engineering at all stages ranging from process simulation to device and circuit optimization. The main purpose of TCAD is the technology-development related cost reduction which currently amounts to 35% and is expected to rise to 40%, according to <http://public.itrs.net>.

Due to the aggressive downscaling of CMOS device feature sizes and newly emerging nano-electronic devices, various shortcomings of presently applied TCAD tools appear. These tools are frequently based on semi-classical macroscopic transport models. From an engineering point of view, classical models like the drift-diffusion model, have enjoyed an amazing success due to their relative simplicity, numerical robustness, and the ability to perform two- and three-dimensional simulations on large unstructured grids. Hot-carrier effects have motivated the development of higher-order transport models such as the hydrodynamic, energy-transport and six-moments models. However, inaccuracies originate from the non-local nature of carrier propagation in ultra-scaled devices.

Non-local effects may be of classical or quantum-mechanical nature, depending on the underlying physics relevant to the transport process. Classical non-localities appear, when the mobile carriers' mean-free path is comparable to the device feature size. Quantum mechanical non-local effects start to determine the transport properties, when the device size is of the order of the De-Broglie electron wave length. Size quantization of carrie motion in inversion layers of

MOSFETs and in ultra-scaled multi-gate devices as well as the tunneling current, including the gate leakage current, are the most important examples of quantum effects in MOSFETs.

Semi-classical transport models are based on the Boltzmann equation which includes scattering integrals describing realistic microscopic processes. These semi-classical models, augmented with quantum corrections, are still of great importance due to their relative computational simplicity, numerical stability, and an ability to provide reasonable quantitative results within seconds even for devices with gate length as short as 50 nm. A brief overview of the currently developed semi-classical transport models will be presented.

Quantum ballistic transport models describe a coherent propagation of carriers. They are based on the solution of the Schrödinger equation for the wave function, supplemented with the corresponding boundary conditions. This approach is efficient and provides accurate results, when carrier scattering is not relevant and can be neglected. The method will be illustrated with an example of transport in carbon nano-tubes.

Finally, dissipative quantum transport theory represents the most complete description of transport, which combines the coherent carrier motion between the scattering events with coherence (or phase) breaking due to carrier scattering. Different formalisms are currently used, based on the Dyson equation for the non-equilibrium Green's functions, the Liouville/Von-Neumann equation for the density matrix, or the Wigner transport equation. The main concepts for modeling quantum transport characterized by both, scattering and quantization, will be briefly explained.

A conclusion will summarize the main findings, and important directions for future research will be recommended.

Short Biography of Siegfried Selberherr

Siegfried Selberherr was born in Klosterneuburg, Austria, in 1955. He received the degree of "Diplomingenieur" in Electrical Engineering and the doctoral degree in Technical Sciences from the "Technische Universität Wien" in 1978 and 1981, respectively. Dr. Selberherr has been holding the "venia docendi" on "Computer-Aided Design" since 1984. Since 1988 he has been chair professor of the "Institut für Mikroelektronik" and from 1999 to 2005 he was Dean of the "Fakultät für Elektrotechnik und Informationstechnik". His current research interests are modeling and simulation of problems for microelectronics engineering. Prof.Selberherr is a Fellow of the IEEE, a Distinguished Lecturer of the IEEE Electron Devices Society, and Chapter Partner of the IEEE ED South Brasil Section.