VSP – A Gate Stack Analyzer

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I Introduction

Numerous technological innovations, including material and process changes such as high–k gate dielectrics and metal gate electrodes, are investigated to meet the upcoming scaling requirements while keeping the gate leakage current within tolerable limits [1, 2]. To overcome the technological problems, further theoretical and experimental research is needed which requires an extensive use of computer simulation. We present a software tool, the Vienna Schrödinger Poisson solver (VSP), for investigations of novel gate stacks with emphasis on reliability.

II Theory of Modeling

For investigations of the electrostatics in MOS inversion layers, a closed boundary Schrödinger Poisson has been applied. VSP includes models for interface traps and bulk traps in arbitrarily stacked gate dielectrics. The band structure for electrons and holes is given by an arbitrary number of valley sorts, defined by an anisotropic effective mass and a band edge energy. Also, the effects of substrate orientation and strain on the band structure are taken into account. The leakage current calculations are performed in a post processing step, since they have a negligible influence on the electrostatic device behavior.

Following [3], the direct tunneling current components from both, continuum J_{3D} and quasi bound states (QBS) J_{2D}, can be estimated by

$$J = \underbrace{\frac{\mathrm{k_B}T\mathrm{q}}{\pi\hbar^2}\sum_i \frac{g_\nu m_\parallel}{\tau_i}\ln\left(\frac{1+\exp\left(\frac{\mathcal{E}_{\mathrm{F\,bulk}}-\mathcal{E}_i}{\mathrm{k_B}T}\right)}{1+\exp\left(\frac{\mathcal{E}_{\mathrm{F\,gate}}-\mathcal{E}_i}{\mathrm{k_B}T}\right)}\right)}_{J_{\mathrm{2D}}} + \underbrace{\mathrm{q}\int\limits_{\mathcal{E}_{\mathrm{min},1}}^{\mathcal{E}_{\max}} TC(\mathcal{E}_x, m_{\mathrm{diel}})N(\mathcal{E}_x, m_{\mathrm{D}})\,\mathrm{d}\mathcal{E}_x}_{J_{\mathrm{3D}}} \;.$$

Here, the symbols g_ν, $m_\parallel$, and m_q denote the valley degeneracy, parallel mass, and quantization mass respectively. The Fermi energy in the bulk $\mathcal{E}_{\mathrm{F\,bulk}}$ and the gate $\mathcal{E}_{\mathrm{F\,gate}}$ determines the number of occupied states. The lifetimes τ_i of the QBS (see Fig. 1) are evaluated using the semiclassical round trip time [4] or a more sophisticated open boundary model [5]. Free states are considered by integration of the Tsu-Esaki formula with the transmission coefficient $TC(\mathcal{E}_x)$ and the number of occupied states $N(\mathcal{E}_x)$ starting at $\mathcal{E}_{\mathrm{min},1}$.

Trap assisted tunneling (TAT), which is a major issue regarding reliability in novel gate stacks [6], is taken into account in terms of an inelastic single step tunneling process[7] (see Fig. 2). The current density writes: $J_{\mathrm{tat}} = \mathrm{q}\sum_i R_i \Delta x_i$. Here, R_i denotes the capture and emission rates of each trap and Δx_i is the trap cross section. The model has been calibrated by measurement.

III Software Techniques

Our software is written in C++ using state-of-the-art software design techniques. Critical numerical calculations are performed with the stable and powerful numerical libraries Blas, Lapack, and Arpack. VSP holds a graphical user interface written in Java, as well as a text based interface. Furthermore, VSP has an open software application interface (API) for the integration within third party simulation environments. These features are used to perform tasks like parameter identification and model calibration, e.g for CV curves and gate stack optimization.

IV Applications and Results

VSP is suitable for the investigation of conventional as well as novel device designs like fully depleted DG-MOS structures. The capacitance voltage characteristic of various MOS structure including a $\mathrm{Si_3N_4}$ layer has been evaluated and plotted in Fig. 3. The corresponding leakage currents are shown in Fig. 4. Furthermore, structures including a layer of $\mathrm{HfO_2}$ can be analyzed. The CV characteristics using a metal and a poly silicon gate are shown in Fig. 5. The effect of poly depletion can be clearly seen. Hence, the use of metal gate is reasonable for further down scaling the EOT to the sub 1.0 nm. Fig. 6 depicts the leakage characteristics of these structures. The properties are considerable improved due the increased physical thickness using high–k dielectrics. Our tool is available for Linux, Windows, IBM AIX 5, and MacOs upon request.

References

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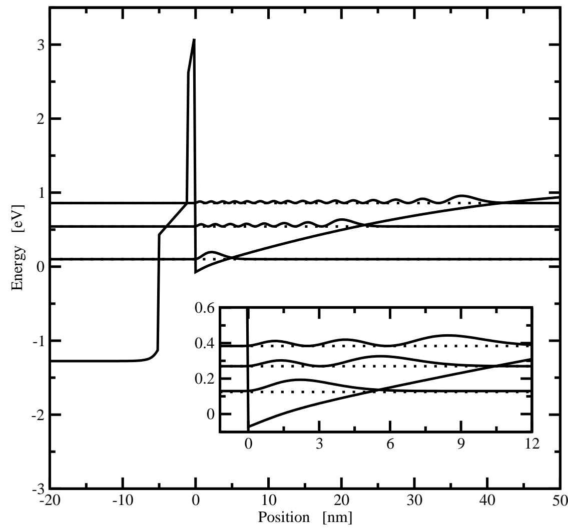

Fig. 1: The wavefunctions and the energy levels of some QBS in the inversion layer of an nMOS device with a stacked gate dielectric.

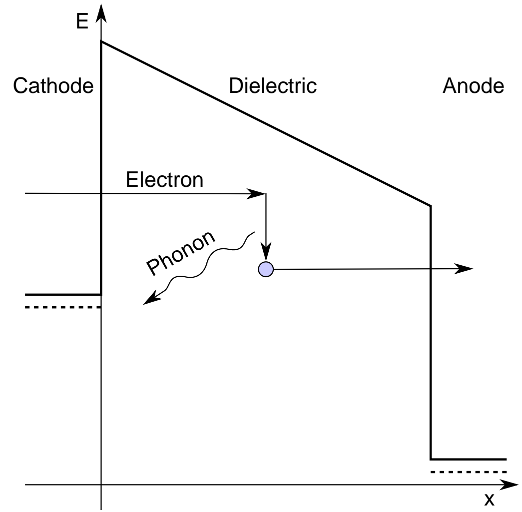

Fig. 2: The trap-assisted tunneling process where the excess energy of the tunneling electrons is released by means of phonon emission.

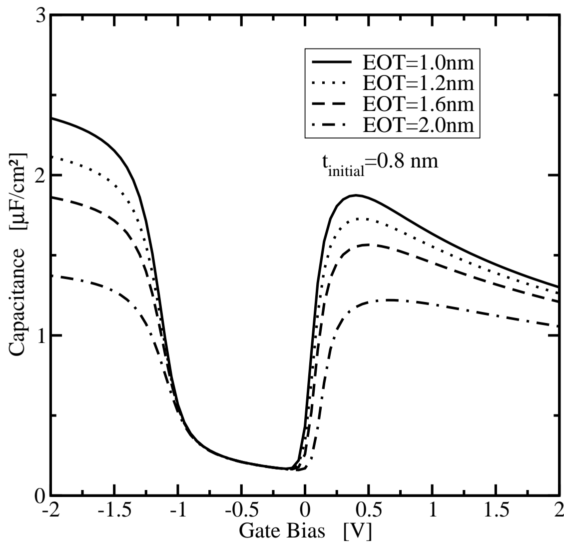

Fig. 3: The CV characteristic of SiO_2 Si_3N_4 stacked gate dielectric for different EOTs. An initial SiO_2 layer of 0.8 nm has been assumed.

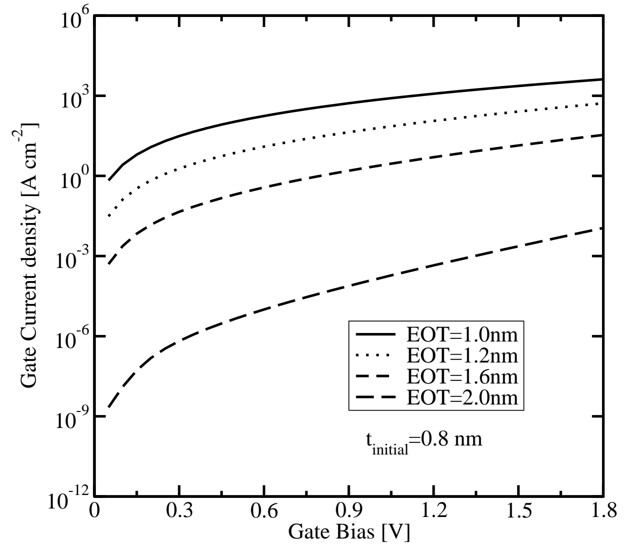

Fig. 4: The gate current density of SiO_2 Si_3N_4 stacked gate dielectric at several EOTs.

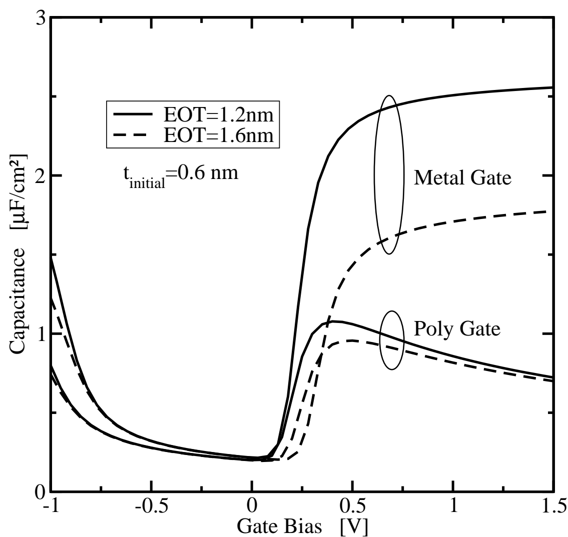

Fig. 5: The CV curve of a SiO_2 HfO_2 gate stack with a poly-Si and a metal gate.

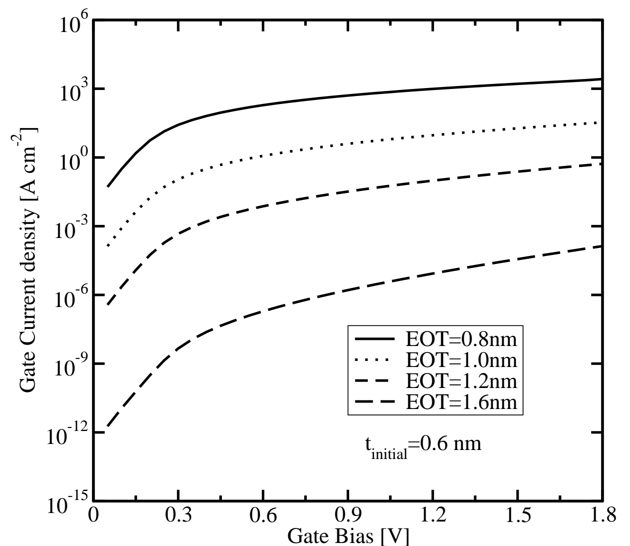

Fig. 6: The simulated leakage current density of a SiO_2 HfO_2stacked gate dielectric.