Optimization Issue in Interconnect Analysis

Stefan Holzer and Siegfried Selberherr

Abstract— **State-of-the-art semiconductor devices with feature sizes in the deca nanometer regime require extremely shrinked geometries for their interconnect structures. Since various physics-based limits are already reached or, at least, rapidly approached, new materials are considered. The arrangements of these new materials can often not yet be rigorously described due to limited knowledge and limited resources, such as time and money. For practical applications, the uncertainty of material parameters and the limited knowledge of material interactions can be compensated by the introduction of parameterized models to describe the global behaviour sufficiently. In this work, such models are used to calibrate and optimize complete interconnect structures for enhanced applications.**

I. Introduction

New integrated circuits' designs require high quality analysis for their sophisticated interconnect structures as well as for the devices. Therefore, new models and methods need to be developed to allow a sufficiently accurate description of the observed behavior. Interconnect structures have already reached a level of complexity where the behavior of the included materials and their interactions cannot be rigorously described by simple and basic equations because of limited knowledge of fundamental material parameters or by limited time. Therefore, parameterized models are required which allow a sufficient description of the observed behavior with reasonable computational effort in the desired range of interest and within a reasonable amount of time. Using sophisticated simulation and optimization tools new information can be obtained to develop new models and to adjust the parameters by calibration and optimization methods for appropriate needs. To exemplify this procedure we consider a complex fusing structure consisting of several polycrystalline interconnect materials. In the following section, the principle for obtaining uncertain or unknown parameters is presented. Afterwards the simulation models are sketched and the necessary equations are explained, where we introduce the adoptions for our simulation tools to obtain the temperature-dependent equation systems. Furthermore, for the investigated fusing structure a comparison between measurements and simulation results is carried out.

Stefan Holzer is with the Christian Doppler Laboratory for TCAD in Microelectronics, Faculty of Electrical Engineering and Information Technology, TU Wien, Gußhausstraße 27-29 / E360, 1040 Wien, Austria, E-mail: Holzer@iue.tuwien.ac.at

Siegfried Selberherr is with the Institute for Microelectronics, Faculty of Electrical Engineering and Information Technology, TU Wien, Gußhausstraße 27-29 / E360, 1040 Wien, Austria, E-mail: Selberherr@iue.tuwien.ac.at

II. Optimization and Calibration Tools

State-of-the-art simulation and optimization frameworks [1–4] offer a wide range of optimization strategies and interfaces to various simulation tools. The *Simulation Environment for Semiconductor Technology Analysis* (Siesta) [4] provides numerous optimizers and interfaces to simulators which can be appropriately chosen for a particular problem. An overview of the data flow in Siesta for parameter extraction is shown in Fig. 1. The core part for parameter extraction is the optimizer and a tool which compares the simulation result with a reference under certain user-defined constraints in order to calculate a score value for the quality of the currently available simulation result. With the calculated score value the optimizer tries to improve the simulation result by varying the unknown parameters in order to optimize the score value using different strategies. The other parts of the data processing blocks which are located in the upper half of Fig. 1 are related to the evaluation of the models and their parameters required to obtain the corresponding simulation result.

For achieving best results for the optimization of uncertain and unknown parameters, different optimization strategies can be chosen from gradient-based [5, 6], genetic, evolutionary [7, 8], and heuristic approaches [9–11]. If there are good initial guesses available, the gradient-based algorithms work best compared to genetic algorithms in terms of time efficiency.

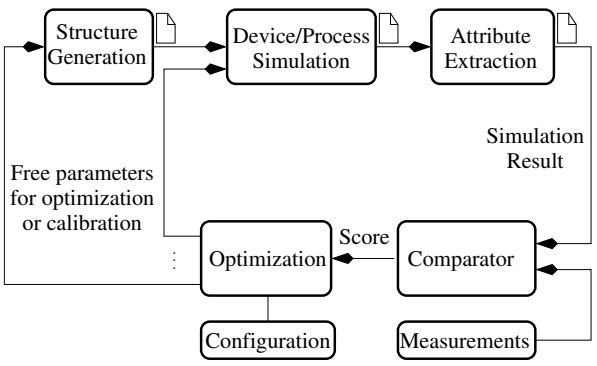

Fig. 1. Data flow for the optimization and calibration of Siesta.

1-4244-0116-X/06/$20.00 © 2006 IEEE

The blocks in Fig. 1 symbolically depict important parts of typical simulation steps: structure generation which means geometry composition and mesh generation to generate the interconnect device structure, the actual underlying device and process simulation, and the necessary post processing steps to extract attributes which can be compared to measurements or to other reference data.

For our example device the shown steps have to be particularly adopted. The following section presents the corresponding models and mathematical equations, which we selected.

III. Simulation Models

For the simulation of the transient temperature evolution the three-dimensional interconnect simulator Stap [12, 13] has been used. Stap calculates Joule self-heating by solving Euler's equation (1) and the heat conduction equation (2) which is coupled with the power loss equation through the heat source term p:

$$\nabla \cdot (\sigma \nabla \varphi) = 0 \tag{1}$$

$$c_\mathrm{p}\, \rho_\mathrm{m} \frac{\partial T}{\partial t} - p = \nabla \cdot (\lambda \nabla \mathrm{T}) \tag{2}$$

$$p = \sigma (\nabla \varphi)^2 \tag{3}$$

Here, φ denotes the electrical scalar potential and σ and λ the electrical and the thermal conductivities. c_p represents the specific heat capacitance, ρ_m the mass density, and T the temperature. The heat source p is assumed to be the Joule power loss [12] due to negligible time changes in carrier concentrations as well as negligible inter-material heating effects [14, 15].

For our investigation we have assumed that the material parameters of the thermal and the electrical conductivity are temperature-dependent and follow the polynomial models

$$\sigma(T) = \frac{\sigma_0}{1 + \alpha_\sigma (T - T_0) + \beta_\sigma (T - T_0)^2} \tag{4}$$

$$\lambda(T) = \frac{\lambda_0}{1 + \alpha_\lambda (T - T_0)}, \tag{5}$$

where σ_0 and λ_0 are the conductivities at a certain reference temperature T_0 and α_σ, β_σ, and α_λ are the corresponding first- and second-order temperature coefficients.

The temperature-dependence of the heat capacitance c_p is modeled with the Shomate equation [16]

$$c_\mathrm{p}(\tau) = A + B\tau + C\tau^2 + D\tau^3 + \frac{E}{\tau^2}, \tag{6}$$

where $\tau = T/1000\,\mathrm{K}$ represents the normalized temperature.

As a solution from the transient electro-thermal simulation we obtain the evolution of the resistance of the fusing structure due to the internal temperature distribution.

IV. Example Device

For processing technologies with feature sizes smaller than 350 nm, the fuses made of polycrystalline interconnect materials became an interesting option for programmable memory cells and one-time programmable switches. In technology nodes with larger feature size fusing can cause damage to the passivation layers and it is thus rated as critical [17, 18]. Arrangements of integrated fuses can be used as one-time programmable memory blocks in a range of several kilobits. Thus, they provide a cheap and efficient alternative to standard non-volatile programmable memory cells, because

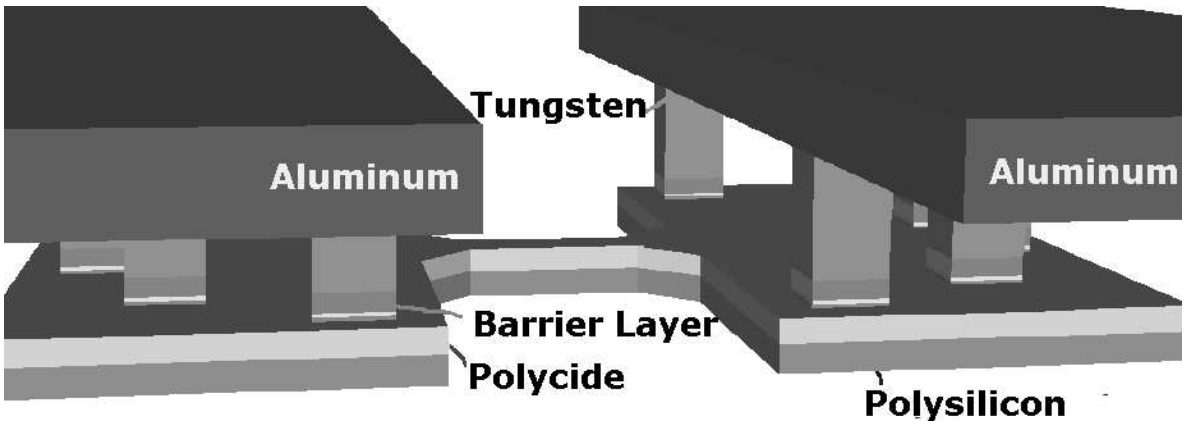

Fig. 2. An overview of the fusing structure showing the variety of different interconnect materials.

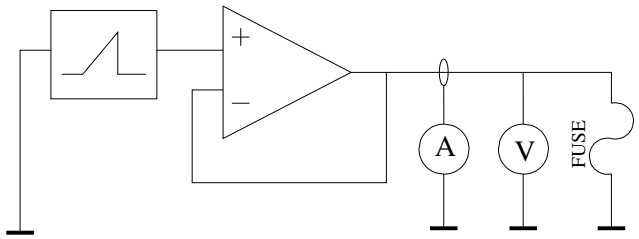

Fig. 3. Schematic of the test circuit for the poly crystalline fuse.

the additional process costs are very low [17]. Moreover, approaches have been reported to increase the memory density by using multi-layered tri-state fuses [19]. Another important application type is to use these fuses in field programmable gate arrays for trimming circuits to obtain a certain analog or digital performance [20]. These fuse applications can be used as elements for trimable resistors and capacitor arrays [21]. Furthermore, the fuses can also act as classic protective elements for critical circuit components [22].

The structure of a typical interconnect fusing device is shown in Fig. 2 which also displays the complex material composition. This fusing structure is used in a surrounding silicon dioxide layer [17].

The dual-layered rod in the region between the two aluminum pads is the actual fusing region which consists of stacked polycide and polysilicon layers. Compared to the polysilicon layer, the polycide layer has a high electrical conductivity. Hence, this layer is intended to be the hottest region and to be removed first.

The fuse is programmed by sending a current pulse through the fuse at an appropriate bias. This performs that the polycide layer is removed by electromigration [18]. Hence, the remaining polycrystalline silicon film is opened due to thermal second-breakdown. The final transition takes place when parts of the polycrystalline silicon layer reach the melting point. The molten silicon is transported from the negative biased side to the positive side through the drift of ions [23].

In terms of power and area consumption, fuses made of available interconnect materials are attractive compared to hybrid technologies [24] with other materials. Moreover, the programming is more time-efficient than that of laser fuses which also require much more additional space on the chip and additional processing steps during the fabrication [25].

However, scaling down to smaller feature sizes requires also a decreased supply voltage [26]. This constraint demands a careful design and a rigorous optimization of the fusing structure to ensure the reliability of the programming mechanism [27] and to minimize the power consumption during the fusing process.

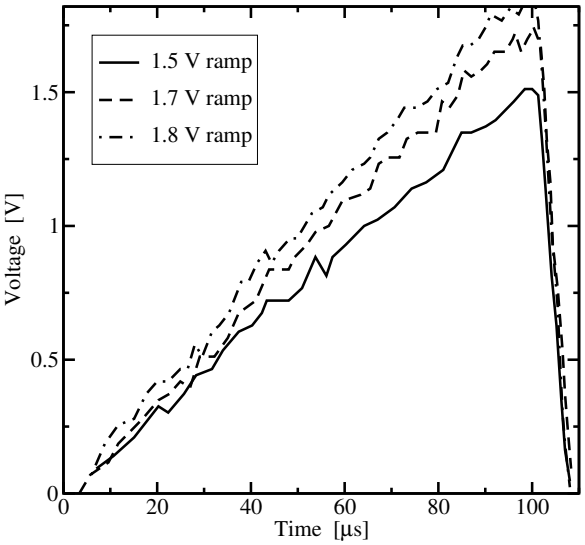

Fig. 4. Different voltage ramps applied to the fuse.

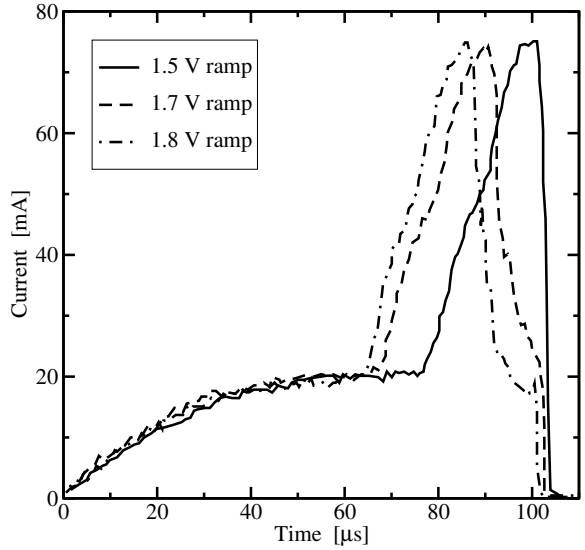

Fig. 5. Measurements of the currents due to the different applied voltages.

Since the fusing mechanism takes place within a couple of 10 ns for a voltage step and several micro seconds for a voltage ramp, direct measurements are hard to obtain [17]. Previous work [28] already brought some new insights into the physics of the fusing mechanism. In addition, an optimization of the fusing structure is required for a fast fusing process and to ensure the reliability. Obtaining these required measurements was only possible through costly experiments using test chips.

We focus on achieving a better insight into the electrical and thermal characteristics of the materials used in the structure shown in Fig. 2. In particular, we are

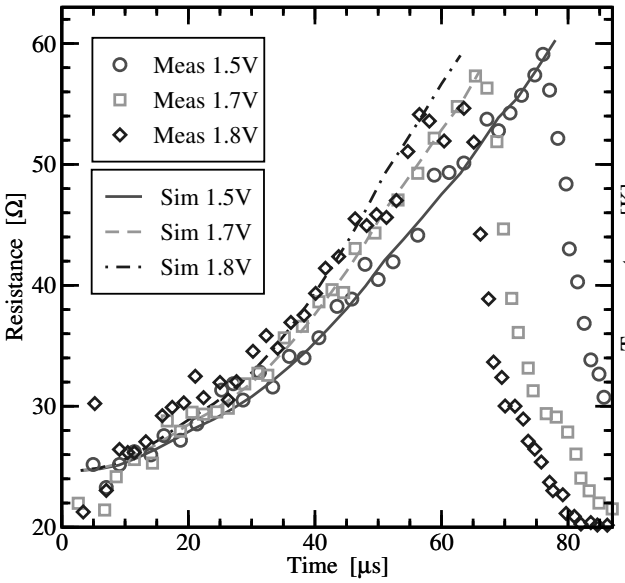

Fig. 6. The simulated fusing resistance compared with the measurements for the different applied voltages.

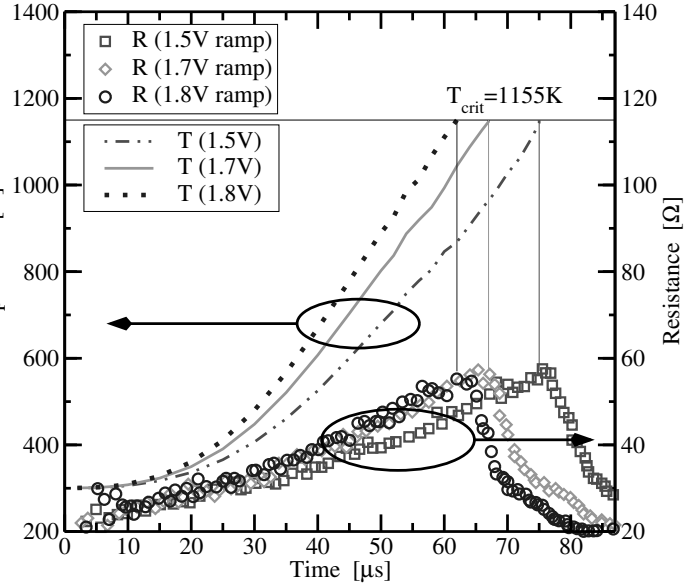

Fig. 7. Comparison of the simulation results with the measurements.

interested in the temperature dependence of the thermal and the electrical conductivity of the key materials polysilicon and the polycide (WSi_x). Better knowledge of these parameters allows to perform a layout optimization for higher reliability of the fusing procedure and a faster fusing operation. With the parameter identification procedure shown in Fig. 1 and the given mathematical models we are able to identify values for certain models within user-defined constraints. In order to obtain reasonable results from the simulation we need accurate information on the test circuit of the fusing device [29] which is depicted in Fig. 3.

Since the measurements of the fusing mechanism have to be carried out within a couple of 10 ns for several μs we prolongated the fusing time by applying a voltage ramp with a rising slope period of 100 μs, which allows to measure the fusing current with reasonable accuracy (cf. Fig. 4 and 5).

These measurement results serve as reference data for the parameter identification procedure. Fig. 5 shows the non-linear behaviour of the fuse current during the heat-up period of the fuse. After a certain time the current jumps to a value which is only constrained by the parasitics of the fuse and the test circuit. Therefore, this point will confine our currently available capability for the simulation and prediction with the introduced models (4) and (5).

For the parameter identification, initial values for the thermal and electrical conductivity of polysilicon and polycide obtained from literature [30–32] were used. The gradient-based optimization algorithm DONLP [5] and the heuristic approach using variants of the simulated annealing approach [10, 33] served well to improve the initial values. Since the constraints were set appropriately to our particular problem, the convergence of the optimization was quite fast. Hence, we obtained very good agreement with the reference data from the measurements with fairly small computational effort.

V. Results and Discussion

The temperature coefficients of the electrical and thermal conductivities of polysilicon and polycide have been computed by minimizing the difference between the reference data obtained from the measurements and the simulation results. In order to achieve that in reasonable time, we had to include several consistency checks to ensure that also the intermediate simulation data are physically reasonable.

After the completion of the optimization (minimization) task we obtained excellent agreement with the measurements as shown in Fig. 6 and 7. The different voltage ramps shown (cf. Fig. 4) result in different points of time, where the thermal run-away starts, visible as discontinuities of the currents in Fig. 5. Moreover, reducing the programming voltages may result in lower programming reliability. According to Fig. 5 the corresponding current for the voltage ramp with 1.5 V seems to be the worst case for a successful programming of this fusing structure. Lowering the programming voltage results in structures not completely shortened, because the heat-up of the fusing region is not sufficient to cause the thermal run-away.

Despite of the different applied voltages, and since the measurements were not averaged, the observed discrepancies between measurement and simulation

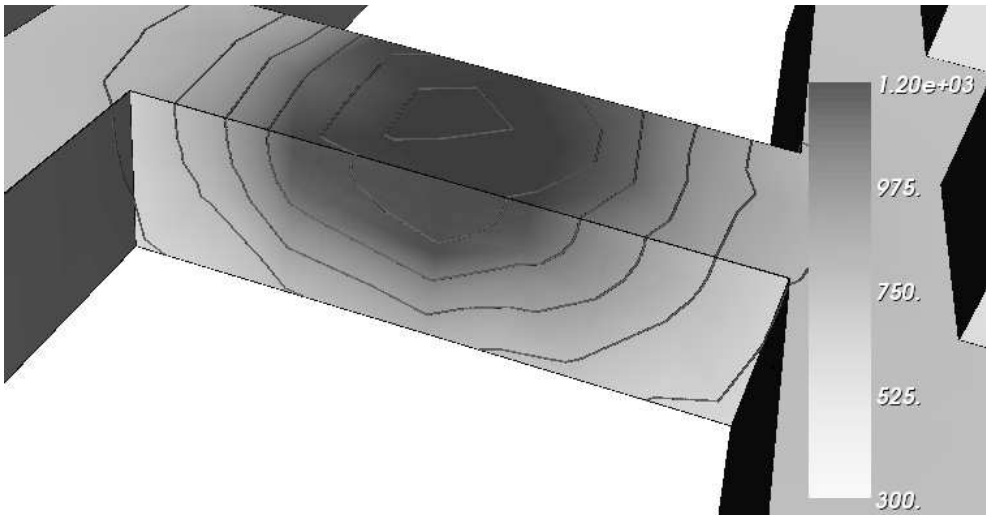

Fig. 8. The temperature distribution [K] at the hottest spot in the fusing area.

in Fig. 6 can be partially traced back to the different measurement methods for obtaining the reference data. However, the overall agreement is still within the accuracy of the simulation results.

The corresponding model coefficients are shown in Tab. I and Tab. II where the extracted and optimized values are compared to data found in the literature [31, 32, 34, 35]. In different technologies, polysilicon is used with different doping concentrations. Therefore, available literature data for the coefficients of the polysilicon model highly depend on the technology used.

Another interesting outcome of our investigation was that the temperature $T_{\mathrm{crit}} = 1155\,\mathrm{K}$, at which the resistance drops, is the same for all applied voltage ramps. Therefore, we can assume that this particular temperature corresponds to a material-specific phenomenon which is related to the thermal run-away due to the starting electromigration process of the polycide layer [18]. When the electromigration process in the polycide region has formed a void, the high conductivity path is disconnected and the whole current flows through the polysilicon layer. Therefore, the polysilicon layer starts to heat up very rapidly towards its melting point. As expected, the area with the highest local temperature is located in the polycide layer of the fusing area in between the two interconnect pads as shown in Fig. 8.

The extracted parameters can be used for investigation of local temperature distributions and self-heating effects in other interconnect structures with similar materials.

VI. Conclusion

We presented an optimization application to obtain important electrical and thermal material parameters of a complex interconnect structure only from electrical measurements. For this purpose, we have tailored our simulation and optimization environment Siesta [3, 4] to achieve fast and automatic parameter adaptations following the chosen gradient-based and heuristic optimization strategies.

These thereby identified parameters have been used to describe the programming operation of fusing structures until the electromigration process and melting of the materials take place in the fusing region of the investigated device.

Further investigations of optimizing the geometry of such fusing structures have been recently shown in [18] to increase the reliability of the electromigration processes. In particular, a lifetime study for polyfuses in $0.35\,\mu$m cmos process has been presented in [36], which shows the lifetime drift and yield as functions of the applied programming conditions. The obtained tempera-

TABLE I
Extracted parameters for polysilicon compared to literature.

Quantity		Poly Si	Literature
σ_0	$[1/\mu\Omega\mathrm{m}]$	0.12	-
α_σ	$[1/\mathrm{K}]$	9.1×10^{-4}	10^{-3}
β_σ	$[1/\mathrm{K}^2]$	7.9×10^{-7}	-
λ_0	$[\mathrm{W/Km}]$	45.4	40
α_λ	$[1/\mathrm{K}]$	2×10^{-2}	10^{-2}

TABLE II
Extracted parameters for polycide compared to literature.

Quantity		Polycide	Literature
σ_0	$[1/\mu\Omega\mathrm{m}]$	1.25	$0.1 - 18.8$
α_σ	$[1/\mathrm{K}]$	8.9×10^{-4}	$5 - 10 \times 10^{-3}$
β_σ	$[1/\mathrm{K}^2]$	8.1×10^{-7}	3.5×10^{-7}
λ_0	$[\mathrm{W/Km}]$	119.4	$100 - 179$
α_λ	$[1/\mathrm{K}]$	2.98×10^{-2}	-

ture coefficients of the electrical and thermal conductivities are used to investigate fusing structures for faster and more reliable programming processes under different operational conditions. These are two major design issues for the possible use of such fusing structures in existing semiconductor device applications. The newly obtained information is also used to determine the electrical and thermal behavior of more complex interconnect systems to support thermo-mechanical investigations for stress analysis [37] which can be used for electromigration analysis [38] in critical interconnect components.

References

[1] Synopsys, *Taurus Work Bench User Manual*, Synopsys, 2003.

[2] ISE Integrated Systems Engineering, *ISE TCAD Manuals*, Integrated Systems Engineering, 2003.

[3] S. Holzer, A. Sheikoleslami, S. Wagner, C. Heitzinger, T. Grasser, and S. Selberherr, "Optimization and Inverse Modeling for TCAD Applications", in *SNDT 2004, Symposium on Nano Devices Technology 2004*, Hsinchu, Taiwan, May 2004, pp. 113–116.

[4] Institute for Microelectronics, *SIESTA – The Simulation Environment for Semiconductor Technology Analysis, Version 1.1std*, Technische Universität Wien, Austria, 2003.

[5] P. Spellucci, "An SQP Method For General Nonlinear Programs Using Only Equality Constrained Subproblems", *Mathematical Programming*, vol. 82, no. 3, pp. 413–448, 1998.

[6] R. Plasun, *Optimization of VLSI Semiconductor Devices*, Dissertation, Technische Universität Wien, 1999, http://www.iue.tuwien.ac.at.

[7] J. Holland, "Adaption in Natural and Artificial Systems", *University of Michigan Press, Ann Arbor, MI*, 1975.

[8] D. E. Goldberg, *Genetic Algorithms in Search and Optimization*, Addison-Wesley, 1989.

[9] V. Ĉerny, "Thermodynamical Approach to the Traveling Salesman Problem: an Efficient Simulation Algorithm", *J. Opt. Theory Appl.*, vol. 45, pp. 41–45, 1985.

[10] L. Ingber, "Very Fast Simulated Re-Annealing", *Mathematical Computer Modelling*, vol. 12, pp. 967–973, 1989, `http://www.ingber.com/asa89_vfsr.ps.gz`.

[11] L. Ingber, "Genetic Algorithms and Very Fast Simulated Re-Annealing: A Comparision", *Mathematical and Computer Modelling*, vol. 16, pp. 87–100, 1992, `http://www.ingber.com/asa92_saga.ps.gz`.

[12] R. Sabelka and S. Selberherr, "A Finite Element Simulator for Three-Dimensional Analysis of Interconnect Structures", *Microelectronics Journal*, vol. 32, pp. 163–171, 2001.

[13] Institute for Microelectronics, *The Smart Analysis Programs*, Technische Universität Wien, Austria, 2003.

[14] G.K. Wachutka, "Rigorous Thermodynamic Treatment of Heat Generation and Conduction in Semiconductor Device Modeling", *IEEE Trans.Computer-Aided Design*, vol. 9, no. 11, pp. 1141–1149, Nov. 1990.

[15] R. Sabelka, *Dreidimensionale Finite Elemente Simulation von Verdrahtungsstrukturen auf Integrierten Schaltungen*, Dissertation, Technische Universität Wien, 2001.

[16] A. Cezairliyan, *Specific heat of solids*, Hemisphere Publishing Corp., 1988.

[17] R. Minixhofer, S. Holzer, C. Heitzinger, J. Fellner, T. Grasser, and S. Selberherr, "Optimization of Electrothermal Material Parameters Using Inverse Modeling", in *Proc. 33rd European Solid-State Device Research Conference (ESSDERC 2003)*, José Franca and Paulo Freitas, Eds., Estoril, Portugal, Sept. 2003, pp. 363–366, IEEE.

[18] W. R. Tonti, J. A. Fifield, J. Higgins, W. H. Guthrie, W. Berry, and C. Narayan, "Reliability and Design Qualification of A Sub-Micron Tungsten Silicide E-Fuse", in *Proc. 42nd Annual Intl. Reliability Physics Symposium*, Apr. 2004, pp. 152–156.

[19] A. Doyle, "A Thick Polysilicon Three-State Fuse", *Motorola Technical Developements 3*, pp. 31–32, 1993.

[20] O. Kim, "CMOS Trimming Circuit Based on Polysilicon Fusing", *Electr.Lett.*, vol. 34, no. 4, pp. 355–356, 1998.

[21] D. J. Nickel, "Element Trimmable Fusible Link", *IBM Technical Disclosure Bulletin*, vol. 26, no. 8, pp. 4415, 1984.

[22] J. R. Lloyd and M. R. Polcari, "Polysilicon Fuse", *IBM Technical Disclosure Bulletin*, vol. 24, no. 7A, pp. 3442, 1981.

[23] D. W. Greve, "Programming Mechanism of Polysilicon Resistor Fuses", *IEEE Trans.Electron Devices*, vol. 29, no. 4, pp. 719–724, 1982.

[24] Y. Fukada, S. Kohda, K. Masuda, and Y. Kitano, "A New Fusible-Type Programmable Element Composed of Aluminum and Polysilicon", *IEEE Trans.Electron Devices*, vol. 33, no. 2, pp. 250–253, 1986.

[25] K. Arndt, C. Narayan, A. Brintzinger, W. Guthrie, D. Lachtrupp, J. Mauger, D. Glimmer, S. Lawn, B. Dinkel, and A. Mitwalsky, "Reliability of Laser Activated Metal Fuses in DRAMs", in *Proc. Twenty-Fourth IEEE/CPMT Electronics Manufacturing Technology Symposium*, Oct. 1999, pp. 389–394.

[26] A. Kalnitsky, I. Saadat, A. Bergemont, and P. Francis, "$CoSi_2$ Integrated Fuses on Poly Silicon for Low Voltage 0.18 μm CMOS Applications", in *Proc.IEDM Tech.Dig*, 1999, pp. 765–768.

[27] D. W. Greve, "Programming Mechanism of Polysilicon Fuse Links", *IEEE Trans.Electron Devices*, vol. 17, no. 2, pp. 349–354, 1982.

[28] S. Das and S.K. Lahiri, "Transient Response of Polysilicon Fuse-Links for Programmable Memories and Circuits", in *SPIE's Semiconductor Devices*, May 1996, vol. 2733, pp. 232–234.

[29] S. Holzer, R. Minixhofer, C. Heitzinger, J. Fellner, T. Grasser, and S. Selberherr, "Extraction of Material Parameters Based on Inverse Modeling of Three-Dimensional Interconnect Fusing Structures", *Microelectronics Journal*, vol. 35, no. 10, pp. 805–810, 2004.

[30] W. Harth, *Halbleitertechnologie*, Teubner, 1981.

[31] C. Vahlas, P.-Y. Chevalier, and E. Blanquet, "A Thermodynamic Evaluation of Four Si-M (M = Mo, Ta, Ti, W) Binary Systems", *Computer Coupling of Phase Diagrams and Thermochemistry*, vol. 13, no. 3, pp. 273–292, 1989.

[32] A. D. McConnell, S. Uma, and K. E. Goodson, "Thermal Conductivity of Doped Polysilicon Layers", in *Proc. of the Intl. Conference on Heat Transfer and Transport Phenomena in Microscale Structures*, G. P. Celata *et al.*, Ed., New York, 2000, pp. 413–419, Begell House.

[33] M. M. Ali, A. T orn, and S. Viitanen, "A Direct Search Variant of the Simulated Annealing Algorithm for Global Optimization Involving Continuous Variables", *Computers and Operations Research*, vol. 29, no. 1, pp. 87–102, 2002.

[34] K. Kells, *General Electrothermal Semiconductor Device Simulation*, Hartung-Gorre Verlag, Konstanz, 1994.

[35] D. C. Katsis and J. D. van Wyk, "Experimental Measurements and Simulation of Thermal Performance Due to Aging in Power Semiconductor Devices", in *Proc. Industry Applications Conference, 2002, 37th IAS Annual Meeting*, Pittsburgh, USA, 2002, pp. 1746–1751.

[36] J. Fellner, P. Boesmueller, and H. Reiter, "Lifetime Study for a Poly Fuse in a 0.35μm Polycide CMOS Process", in *Proc. 43rd Annual Intl. Reliability Physics Symposium*, Apr. 2005, pp. 446–449.

[37] C. Hollauer, S. Holzer, H. Ceric, S. Wagner, T. Grasser, and S. Selberherr, "Investigation of Thermo-Mechanical Stress in Modern Interconnect Layouts", in *Sixth International Congress on Thermal Stresses*, Wien, Austria, May 2005, pp. 637–640.

[38] H. Ceric, C. Hollauer, S. Holzer, T. Grasser, and S. Selberherr, "Comprehensive Analysis of Vacancy Dynamics Due to Electromigration", *Proceedings of the 13th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, pp. 100–103, June 2005.