Impact of NBTI-Driven Parameter Degradation on Lifetime of a 90nm p-MOSFET

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ABSTRACT

NBTI has emerged as a major reliability concern for the electrical stability of advanced CMOS technology. We report an experimental and simulation study for the NBTI mechanism in a high-performance p-MOSFET. Various stress experiments were performed in order to analyze the degradation of the key device parameters, V_T and I_{Dsat}. The presently leading reaction-diffusion (R-D) model is used to study the interface trap generation based on the diffusion and accumulation of released hydrogen in the gate oxide. The long-time degradation was simulated in order to estimate the NBTI lifetime which depends on the applied gate voltages and frequencies. The lifetime extension under higher frequency operation was analyzed at a typical supply voltage of 1.45V with a tolerance of $\pm 50\mathrm{mV}$. An unexpected long lifetime extension between six times and twenty times of the DC lifetime was found for an operation with a 10MHz gate signal.

INTRODUCTION

Although the degradation of the Si/SiO_2 interface in p-MOSFETs caused by negative bias temperature instability (NBTI) has been known for a long time, NBTI has become a serious reliability problem for newer CMOS technologies. Nitrogen is incorporated in thinner gate oxides for the 90nm technology and beyond mainly to reduce the gate leakage current, to avoid boron penetration into the dielectric, and to improve the hot carrier injection (HCI) reliability. However, it turned out that nitrided gate oxides (SiON) exhibit a significantly higher NBTI degradation compared to pure SiO_2 for the same physical oxide thickness and voltage condition [1]. Experimental studies revealed that the thermal activation energy of interface trap generation decreases steadily with increasing the nitrogen concentration at the interface [2].

It is well known that the NBTI mechanism in p-MOSFETs depends on the applied gate voltage, temperature, and stress time. Since indirect measuring techniques have to be applied, it is difficult to correlate measurement results to NBTI induced interface degradation associated with bond breaking and chemical species. While the exact nature of the NBTI phenomenon is still unknown, it is widely accepted that interface traps are generated by breaking of hydrogen-passivated silicon bonds at the interface and subsequent diffusion of hydrogen [3, 4]. Charge pumping and gate leakage current measurements revealed that NBTI under moderate oxide fields occurs mainly due to interface traps N_{it} and that the generated oxide traps N_{ot} can be neglected [5]. The NBTI-induced interface charges cause a parameter degradation of the MOSFET firstly due to a reduction in inversion layer holes and secondly due to a mobility degradation by Coulomb scattering. NBTI degradation affects the key parameters of the MOSFET, V_T and I_{Dsat}, and therefore it is very interesting to study the impact of NBTI-driven parameter degradation on the device lifetime.

Under dynamic operation of the transistor the interface traps which are generated during the on-state are partially annealed in the off-state. Therefore the AC degradation is significantly lower than the DC degradation for any given stress time. The magnitude of the NBTI-driven parameter shift over time is significantly reduced for higher frequencies or smaller "on" duty cycles [6, 7]. In this paper we analyze mainly the impact of an operation at higher frequencies in the MHz-range at slightly different supply voltages on the AC lifetime of the transistor.

EXPERIMENTAL DETAILS

The investigated device is a p-MOSFET fabricated in a 90nm process technology with shallow trench isolation (STI). The high-performance transistor is applied in six-transistor SRAM cells. The gate oxide was annealed in an NO_x gas ambient and has a physical oxide thickness of 24Å and an equivalent oxide thickness (EOT) of 20.5Å.

Figure 1 depicts the used configuration for NBTI measurements under DC and pulsed stress conditions at a constant temperature of 125° C. Various stress experiments were performed in order to analyze the gate voltage, duty cycle, and frequency dependence of the NBTI degradation behavior. Frequency measurements were performed in the range from DC to 1 MHz and "on" duty cycles in the range of 30% to 70% were used. Voltages were applied from -1.5 V up to -2.7 V to the gate of the transistor. The MOSFET parameters were monitored for a maximum stress time of 10^5s. The collected NBTI data were then used to calibrate the numerical simulations for the 90nm device.

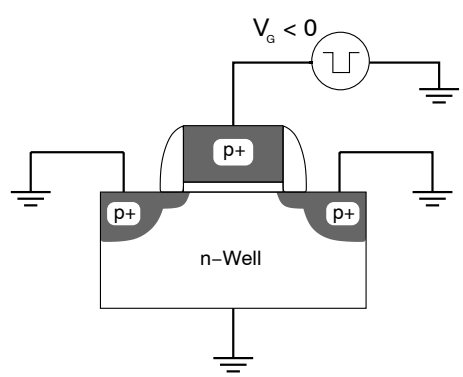

Fig. 1: Configuration for DC and pulsed NBTI stress.

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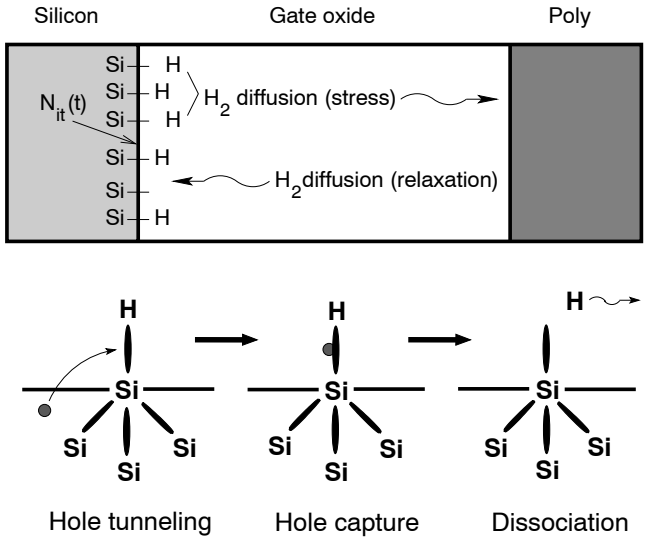

Fig. 2: Possible mechanism of breaking interfacial Si–H bonds by interaction with inversion-layer holes. The degradation is controlled by the forth-and-back motion of released hydrogen in the gate oxide.

REACTION-DIFFUSION MODEL

A reaction-diffusion (R-D) model was used for the simulation of NBTI degradation, because this model can predict static and dynamic NBTI data [8, 9]. Figure 2 shows a schematic description of the R-D model. A possible scenario for the generation of interface traps is that Si–H bonds break by interacting with holes at elevated temperatures. The upper sketch shows that released hydrogen diffuses into the gate oxide and returns back to the interface when the stress is removed [5]. In the R-D model the formation of interface traps is described by two coupled differential equations according to

$$\frac{\partial N_{it}(t)}{\partial t} = k_f\,[N_0 - N_{it}(t)] - k_r\,N_{it}(t)\,C_H(x{=}0,t) \quad (1)$$

$$\frac{\partial N_{it}(t)}{\partial t} = -D\,\frac{\partial C_H(x,t)}{\partial x}\Big|_{x=0} + \frac{\delta}{2}\frac{\partial C_H(x,t)}{\partial t} \quad (2)$$

Equation (1) states that the N_{it} generation is determined by a chemical hydrogen release reaction (const. dissociation rate k_f) and simultaneous self-annealing (rate k_r), when the p-MOSFET is biased in inversion. When the transistor is switched off, the forward rate k_f becomes zero and the reverse rate k_r stays unchanged. The parameter N_0 denotes the total Si–H bond density at the interface before stress. Equation (2) is obtained by integration of the standard diffusion equation across the silicon/oxide interface with a thickness δ. The diffusion coefficient D is the average diffusivity of the assumed atomic and molecular hydrogen diffusing species. Note that $N_{it}(t)$ is equal to the number of released hydrogen atoms at any given time t.

The discretization of the differential equations is based on a one-dimensional finite differences method. The simulation domain is the gate oxide with the boundary condition of a partially absorbing wall at the oxide/poly interface. The differential quotients are approximated using the spatial and temporal increments h and Δt. Grid points (x_i, t_j) with resolution $m = \frac{T_{ox}}{h}$ are used for an oxide thickness T_{ox}, and $x_i = ih$ for $i = 0, 1, \ldots, m$ and $t_j = j\,\Delta t$ for $j = 0, 1, \ldots$

We are solving for the next time step $(n+1)$ in order to calculate the hydrogen diffusion profile $C^j_{H,i} = C_H(x_i, t_j)$ and the interface trap concentration $N^j_{it} = N_{it}(t_j)$ at the next instant according to

$$C^{n+1}_{H,0} = C^n_{H,0} + \frac{2\Delta t\gamma^n}{\delta} + \frac{2\lambda h}{\delta}\left(C^n_{H,1} - C^n_{H,0}\right) \quad (3)$$

$$N^{n+1}_{it} = N^n_{it} + \gamma^n\,\Delta t \quad (4)$$

$$\gamma^n = k_f\,(N_0 - N^n_{it}) - k_r\,N^n_{it}\,C^n_{H,0} \quad (5)$$

$$\lambda = \frac{D\Delta t}{h^2} \quad (6)$$

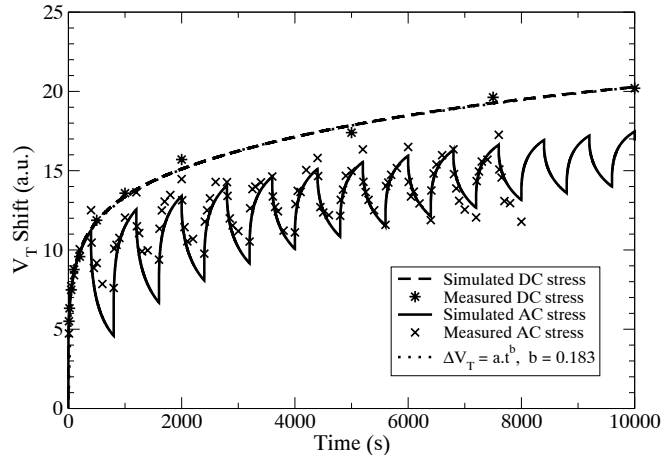

Fig. 3: The numerical solution of the R-D model is compared to NBTI data under DC and AC stress (stress: 400s, relaxation: 400s).

Figure 3 compares the numerical solution of the calibrated R-D model for DC and AC operation to experimental data of the investigated MOSFET. The V_T degradation under static and dynamic NBTI stress was simulated with the same model parameter set.

Chakravarthi et al. found that the atomic hydrogen model exhibits the typical power-law time dependence $V_T \propto t^{0.25}$ whereas the molecular hydrogen model predicts a time dependence of $t^{0.165}$ [4]. We found a time exponent of 0.183 for our measurement data, which supports that both atomic and molecular hydrogen is present. The hydrogen distribution in the oxide is calculated for every time step. The final simulation result is the defect density N_{it} and the corresponding shift $\Delta V_T \propto N_{it}$. The left diagram in Figure 4 shows four snapshots of hydrogen profiles $C_H(x, t_i)$ during the first stress phase. After 400s the transistor is switched off. The right diagram shows the corresponding profiles during relaxation. When relaxation starts the free hydrogen near the interface can now rapidly anneal broken Si–H bonds. The consumption

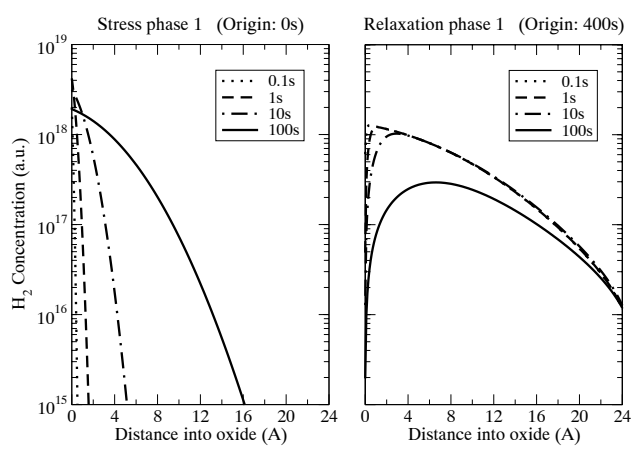

Fig. 4: Snapshots of hydrogen diffusion profiles in the gate oxide during the first stress-relaxation cycle.

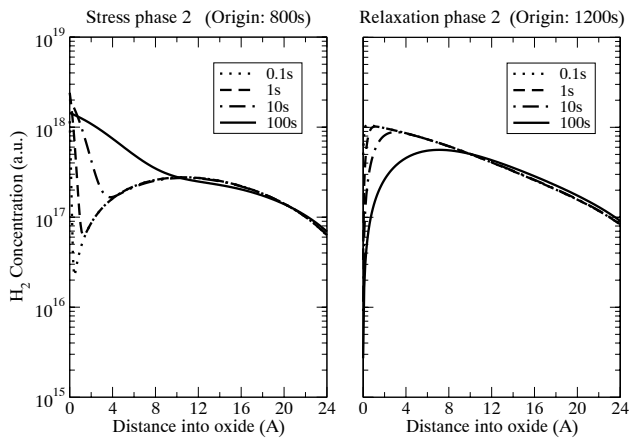

Fig. 5: Hydrogen distributions corresponding to the second stress-relaxation cycle.

of hydrogen near the interface creates a diffusion hole. Figure 5 shows the second stress-relaxation cycle. When stress is applied again a rapid generation of interface traps starts. After the diffusion hole is filled the generation slows down due to diffusion limited transport. In the relaxation phase hydrogen moves back to the interface again. This forward and backward movement continues in subsequent cycles.

Interface traps are built up quickly during the first seconds of a stress phase (reaction-limited regime). With increasing time the hydrogen diffusion front moves towards the oxide-poly interface (diffusion-limited regime). After long times, free and bounded hydrogen densities at the silicon-oxide interface become very low corresponding to a high level of generated interface defects. Recently, Tsujikawa et al. have investigated released hydrogen atoms from the substrate interface during NBTI stress in a p-MOSFET with a 1.85nm thick NO-oxynitride gate dielectric [11]. Although it was expected that hydrogen can easily diffuse out in the case of ultra-thin gate dielectrics, it was found that much of the released hydrogen remains in the gate dielectric. The used boundary condition of a partially absorbing wall at the oxide/poly interface takes the accumulation of hydrogen in the oxide into account.

Figure 6 demonstrates that the calibrated R-D model can be used to study the evolution of transistor parameter degradation over time under DC and AC operation. However, the dynamic NBTI effect guarantees even for a very slow switching operation that the NBTI lifetime is improved by at least a factor of 2.

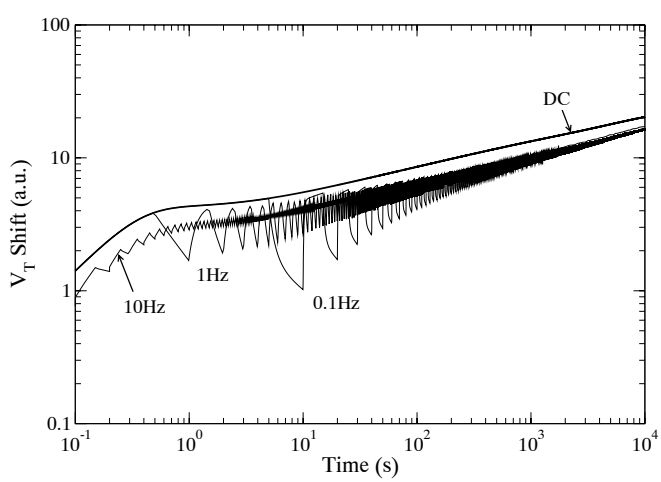

Fig. 6: Simulation of static and dynamic NBTI for the 90nm p-MOSFET in the very low frequency range from DC – 10Hz.

LIFETIME SIMULATIONS

Currently there is no clear specification for the characterization of the NBTI lifetime across industry. Companies use various stress conditions for NBTI measurements as well as different electrical stability requirements for their lifetime projections. A reasonable failure criterion for the 90nm CMOS technology is, for instance, to tolerate a maximum shift of 10% for the key device parameters V_T and I_{Dsat} at 125° C. For our investigated p-MOSFET we found at a V_T shift of 10% an equal shift of 10% for the I_{Dsat} parameter.

At first we analyze the gate voltage and frequency dependence of the NBTI degradation. The dissociation rate k_f is determined by the available surface hole density p which is controlled by the oxide field E_{ox}. Surface holes can tunnel to the Si–H bonds governed by E_{ox}. It can be speculated that the amount of Si–H bonds N_0 at the interface which can be reached by this stochastic tunneling process increases with the electrical field. Therefore the parameters k_f and N_0 of the R-D model depend on the gate voltage [12]. Figure 7 shows good agreement between simulation results and experimental data in the whole measurement range from -1.5V up to -2.7V. Note that the diffusion-limited regime is reached rapidly which is characterized by a reduced slope of the V_T shift over time. Figure 8 demonstrates that the NBTI induced V_T shift is significantly reduced for higher frequencies and/or smaller "on"

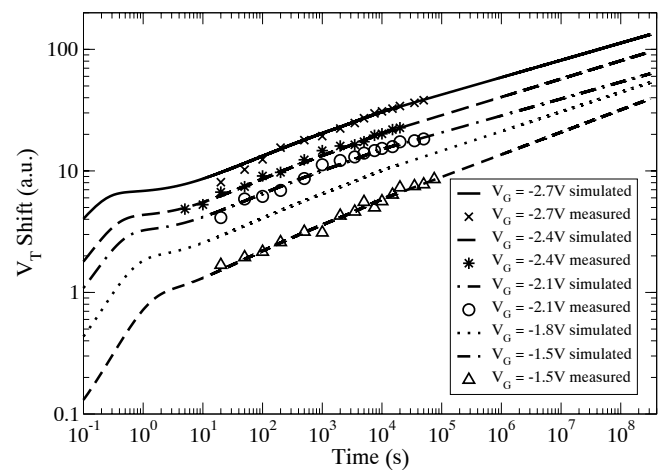

Fig. 7: Gate voltage dependence of NBTI.

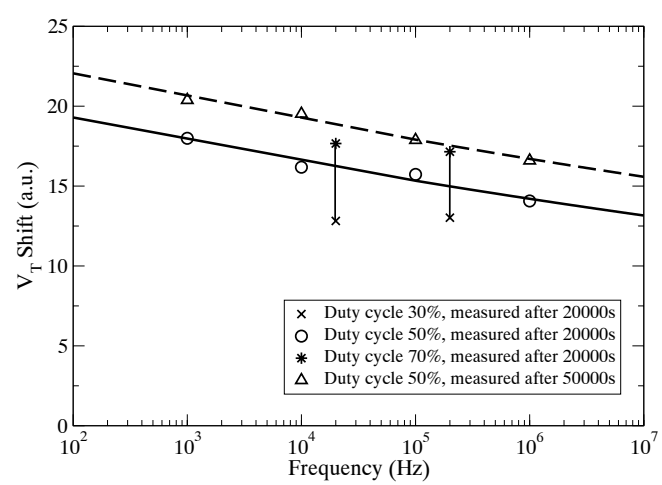

Fig. 8: Frequency dependence of NBTI.

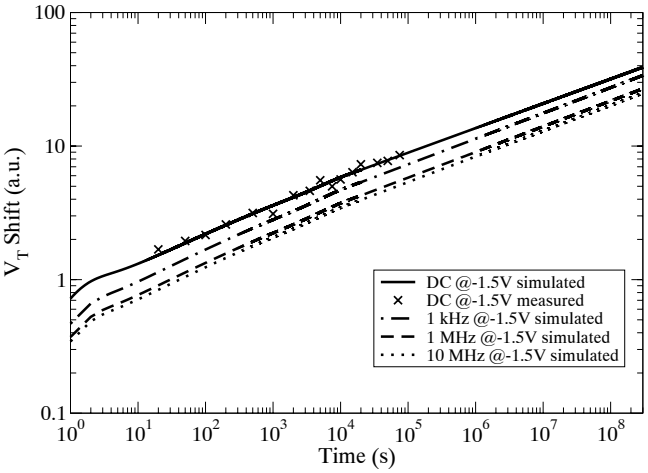

Fig. 9: Long-time simulations for the V_T shift at typical chip frequencies in the MHz range at a power supply of 1.5V.

duty cycles. The measured frequency dependence can be described by using a reference frequency $f_0 \in [1\text{kHz}, 1\text{MHz}]$ according to:

$$V_T(f) \;=\; V_T(f_0)\,\left(\frac{f}{f_0}\right)^{-0.03323} \tag{7}$$

The R-D model assumes a dissociation process with constant rate k_f which is switched on and off without a delay by the edges of the gate voltage signal. Therefore this first order model predicts that the V_T shift does not depend on frequency. The simulation of a higher frequency signal is performed at a low reference frequency and the result is then corrected with the measured relative NBTI shift as function of the frequency according to (7). Figure 9 shows long-time simulations for the lifetime estimation at a supply voltage of 1.5V under DC and AC stress up to 10MHz. Figure 10 analyzes quantitatively the lifetime extension of the p-MOSFET under higher frequency operation at a typical supply voltage of 1.45V with a tolerance of $\pm 50\text{mV}$. The lifetime is defined here by a V_T shift of 80mV. The simulation predicts that the AC lifetime at 10MHz lies between six times (for 1.5V supply) and twenty times (for 1.4V supply) of the DC lifetime at 1.45V operation.

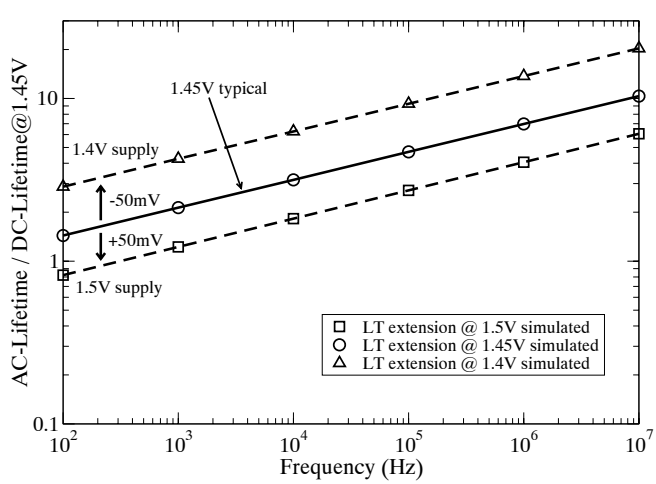

Fig. 10: Simulated lifetime extension under AC operation.

CONCLUSION

The NBTI mechanism was systematically investigated for a 90nm CMOS technology. Experiments for different gate voltages, frequencies, and duty cycles were performed to analyze the device parameter degradation of the p-MOSFET. It turned out that the R-D model is well suited to explain static and dynamic experimental data. The gate voltage and frequency dependence of NBTI was included by means of an empirical relationship. All measured data could be well reproduced by the performed numerical simulations. The presented simulation approach allows, on a physically rigorous basis, to predict the p-MOSFET lifetime which depends strongly on the applied stress conditions.

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