Geometry-dependence of the DC and AC Response of Ohmic Contact Carbon Nanotube Field Effect Transistors

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***Abstract*— In this work the DC and AC responses of ohmic contact carbon nanotube field effect transistors are investigated. To account for ballistic transport in these devices, the coupled system of Poisson and Schrödinger equations was solved. Good agreement between simulation and experimental results confirms the validity of this model. For AC analysis the quasi static approximation was assumed. Simulation results indicate the both the DC and AC response are effectively dependent on the device geometry. Therefore by careful device design, optimized device characteristics can be achieved.**

I. INTRODUCTION

Exceptional electronic and mechanical properties together with nanoscale diameter make carbon nanotubes (CNTs) a candidate for nanoscale field effect transistors (FETs). While early devices have shown poor device characteristics, high performance devices were achieved recently [1, 2].

The contact between metal and CNT can be of Ohmic [3] or Schottky type [4]. In this work we focus on Ohmic contact CNTFETs which theoretically [5] and experimentally [2] show better performance than Schottky type devices. In a p-type ohmic contact device holes see no barrier while the barrier height for electrons is the band gap of the CNT. By changing the gate voltage the transmission coefficient of holes through the device is modulated and as a result the total current changes [3].

In short devices (less than 100 nm) the carrier transport through the device is nearly ballistic [2, 3], therfore we solved the coupled Poisson and Schrödinger equations self-consistently to investigate the behavior of theses devices. In agreement with experimental results, simulations indicate unwanted ambipolar behavior of these devices, which limits the DC characteristics by reducing the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio. We show that by increasing the gate-drain spacer the ambipolar behavior is suppressed and improved DC characteristics is achieved. By increasing the gate-drain spacer the parasitic capacitances between the gate-drain contact are reduced and the AC response also improves. Therefore by careful geometry design the device characteristics can be well optimized.

II. APPROACH

In order to account for the ballistic transport we have solved the coupled Poisson and Schrödinger equations.

$$-\frac{\hbar^2}{2\mathrm{m}^*}\frac{\partial^2\Psi^{n,p}_{s,d}}{\partial z^2}+(U^{n,p}-E)\Psi^{n,p}_{s,d}=0 \qquad (1)$$

$$\nabla^2\epsilon\phi=-\mathrm{q}(p-n) \qquad (2)$$

In (2) $n = n_s + n_d$ and $p = p_s + p_d$, where $n_{s,d}$ and $p_{s,d}$ represent the contributions of the source and drain to the electron and hole concentrations, which are calculated as (3):

$$n_s=\frac{4}{2\pi}\int f_s|\Psi_s|^2 dk_s=\int\frac{\sqrt{2\mathrm{m}^*}}{\pi\mathrm{h}\sqrt{E_s}}f_s|\Psi_s|^2 dE_s \qquad (3)$$

We have considered a cylindrical symmetric structure, in which the gate surrounds the CNT and carriers were taken into account by means of a sheet charge distributed uniformly over the surface of the CNT [6]. The Schrödinger equation is solved on the surface of the tube, and is restricted to one-dimension because of cylindrical symmetry. In (1) superscripts denote the type of the carriers. Subscripts denote the contacts, where s stands for the source contact and d for the drain contact. For example, Ψ^n_s is the wave function associated with electrons that have been injected from the source contact, and U^n is the potential energy that is seen by electrons.

The drain current is calculated using the Landauer-Büttiker formula (4).

$$I_d=\frac{4\mathrm{q}}{\mathrm{h}}\int[f_s(E)-f_d(E)]TC(E)dE \qquad (4)$$

All our calculations assume a CNT with 0.5 eV band gap, corresponding to a diameter of 1.7 nm [2].

The coupled Schrödinger and Poisson equations are solved iteratively [7], by using an appropriate numerical damping factor α, where $0 < \alpha < 1$. Successive iteration continues until a convergence criterion is satisfied. It is also possible to make the self-consistent loop more stable, by providing the derivate of carrier concentration with respect to the electrostatic potential for the Poisson solver [8, 9]. In general there is no exact form for this term, but as proposed in [8], $\partial n/\partial\phi \approx$ q $\partial n/\partial E_F$ can be considered as a good approximation.

To study the dynamic behavior of CNTFETs, the quasi static approximation was assumed. Generally, in this method device capacitances are given by the derivatives of the various charges with respect to the terminal voltages,

$$C_{ij} = \chi_{ij} \frac{\partial Q_i}{\partial V_j}\Bigg|_{V_{k \neq j}=0} \tag{5}$$

where the indices i, j, k represent terminals (gate, source or drain), and $\chi_{ij} = -1$ for $i \neq j$ and $\chi_{ij} = +1$ for $i = j$. The differentiation of these expressions is performed numerically over steady state charges [10]. This method is widely used for the analysis of conventional semiconductor devices, where the charge in the semiconductor device is partitioned into two parts indicating the contribution of the source and drain contacts [10, 11]. For example, the gate-source capacitance is calculated by

$$C_{sg} = \frac{\partial Q_{se}}{\partial V_{gs}} + \frac{\partial Q_{sq}}{\partial V_{gs}} = C_{se} + C_{sq} \tag{6}$$

where Q_{se} is the total charge on the source contact and Q_{sq} is the total charge on the tube injected from the source contact. As shown in (6) the total gate-source capacitance is split into two components, the first term indicates the electrostatic gate-source capacitance and the second term is usually referred to as quantum capacitance [12]. Therfore the capacitance matrix has a rank of 3, and due to quantum capacitances the matrix is not symmetric ($C_{ij} \neq C_{ji}$). In this work we assumed that only the gate voltage changes, whereas the voltages of the other terminals are kept constant. Therfore, the capacitance matrix simplifies to three components, and an equivalent circuit as shown in Fig. 1 is achieved [13]. In Fig. 1, g_m is the differential transconductance calculated by

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{7}$$

Based on the equivalent circuit in Fig. 1, the cutoff frequency of the device can be derived as

$$f_T = \frac{g_m}{2\pi C_{sg}\sqrt{1 + 2\frac{C_{dg}}{C_{sg}}}} \tag{8}$$

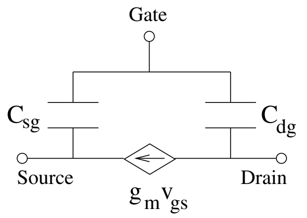

Figure 1: Simplified equivalent circuit model for the dynamic response of CNTFETs. The model is based on the assumption that only the gate voltage changes.

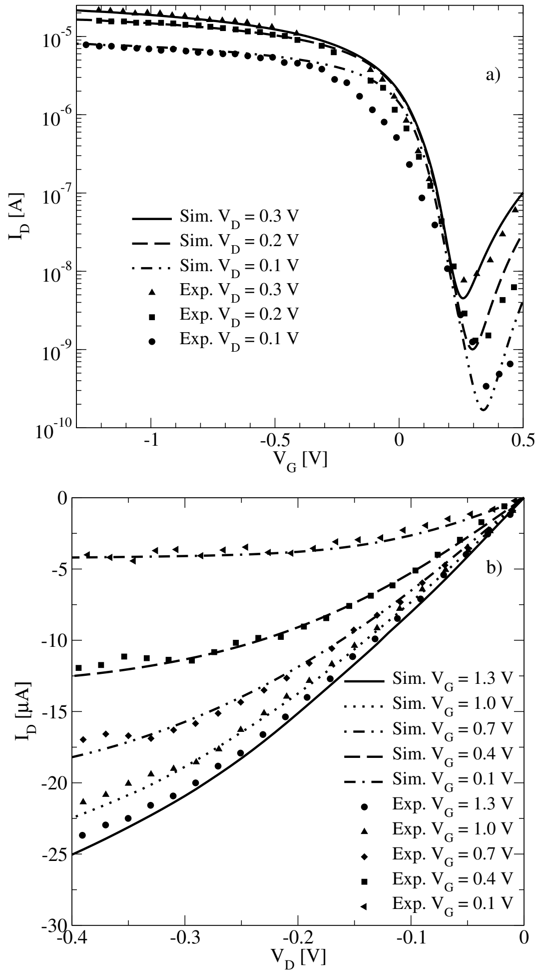

Figure 2: Comparison of the experimental and simulation results a) Transfer characteristics, b) Output characteristics.

III. SIMULATION RESULTS AND DISCUSSIONS

For a fair comparison with experimental results, we used the same material and geometrical parameters as reported in [2]. Although unlike the real device a cylindrical symmetry for simulations was assumed, there is a good agreement between simulation and experimental results, see Fig. 2. The ambipolar behavior is clearly observed in the off regime,

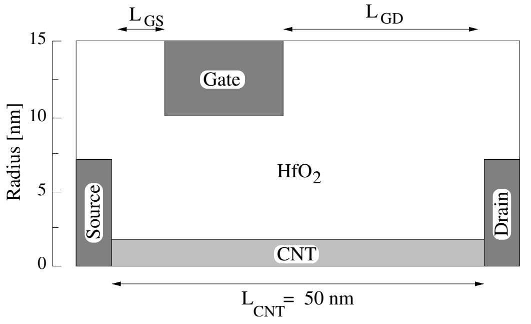

Figure 3: Sketch of the cylindrical device.

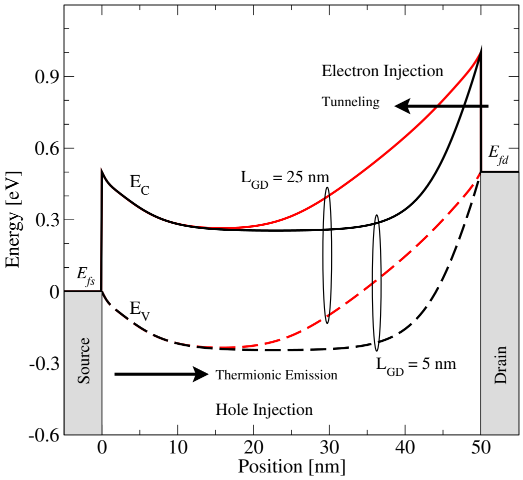

Figure 4: The effect of $\mathrm{L_{GD}}$ on the band-edges profile of the device. $\mathrm{V_G} = 0.5\mathrm{V}$ and $\mathrm{V_D} = -0.5\mathrm{V}$.

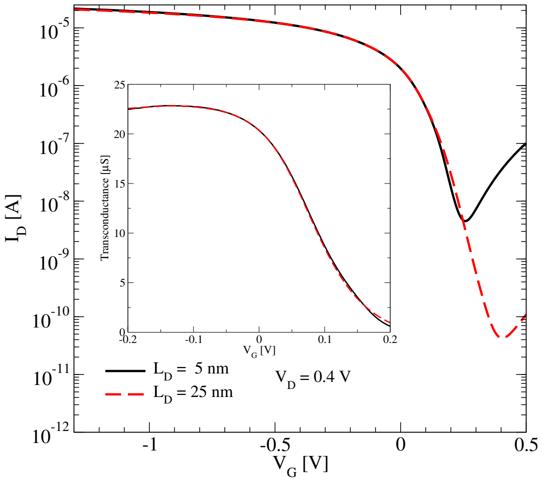

Figure 5: The effect of $\mathrm{L_{GD}}$ on the transfer characteristics. The inset shows the differential transconductance

see Fig. 2-a. This behavior can be well understood by considering the band edge profiles of the device. The device structure is sketched in Fig. 3. As shown in Fig. 4, if the drain voltage becomes higher than the gate voltage the barrier thickness for electrons at the drain contact is reduced and the tunneling current of electron increases. This behavior is more apparent in Schottky contact devices [14]. We have shown that a double gate structure can be used to suppress the ambipolar behavior of Schottky contact devices [15]. In a double gate device the carrier injection at the source and drain contacts are controlled separately. In ohmic contact devices because of asymmetric barrier heights, even a single gate device can reduce the ambipolar behavior. As shown in Fig. 4, by increasing $\mathrm{L_{GD}}$ the band edge profile near the drain contact is less affected by the gate voltage. Therfore, when the potential difference between the gate and drain contacts increases the barrier thickness for electrons near the drain contact is less reduced and as a results the tunneling current of electrons is suppressed. In Fig. 5 the the effect of increasing spacer thickness on the transfer characteristics of the device is shown. By increasing $\mathrm{L_{GD}}$ the off current decreases, while the on current remains unchanged. The Inset of Fig. 5 shows that the differential transconductance remains also unchanged.

Note that this method can not be applied to conventional MOSFETs, because they are charge controlled devices. By changing the gate voltage the channel conductivity is modulated. In contrast the channel of CNTFETs exhibits a constant conductivity ($\mathrm{G} = 2\mathrm{q}^2/\mathrm{h}$ per mode) and the gate voltage modulates the transmission coefficient of carriers through the device. The band edge profile near the source contact plays an important role in determining the total current, since at high drain voltages all the carriers which cross the barrier near the source contact will be absorbed by the drain contact (neglecting minor quantum mechanical reflections).

Fig. 6 shows the effect of increasing of $\mathrm{L_{GD}}$ on the mutual capacitances between terminals. As seen in both cases the electrostatic capacitances dominate the quantum capacitances. By increasing $\mathrm{L_{GD}}$ the electrostatic capacitance between gate and drain contacts is reduced. In general, the model (8) suggests that for a better frequency response the differential transconductance of a device should increase and the parasitic capacitances should decrease. We showed that by increasing $\mathrm{L_{GD}}$, the differential transconductance of the device is not affected, while the gate drain parasitic capacitance is decreased. Based on (8) for the device with $\mathrm{L_{GD}} = 5\mathrm{nm}$ the cutoff frequency is $f_T \approx$ 160 GHz, but for the device with $\mathrm{L_{GD}} = 25\mathrm{nm}$ the cutoff frequency is $f_T \approx$ 210 GHz. The comparison of output characteristics and cutoff frequencies indicates that by increasing $\mathrm{L_{GD}}$ both the DC and AC response of the device are improved.

IV. CONCLUSION

By appropriately selecting the gate-drain spacer thickness both the DC and AC response of ohmic contact CNTFETs are improved. By increasing the gate-drain spacer the ambipolar behavior is suppressed and the parasitic capacitance between the gate and drain contacts is reduced. By suppressing the ambipolar behavior the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio increases by three-orders of magnitude, and by reducing the parasitic capacitances the cutoff frequency increases about 30%. As opposed to CNTFETs, this method is not applicable to conventional MOSFETs because of different mechanisms in controlling the current flow through the device.

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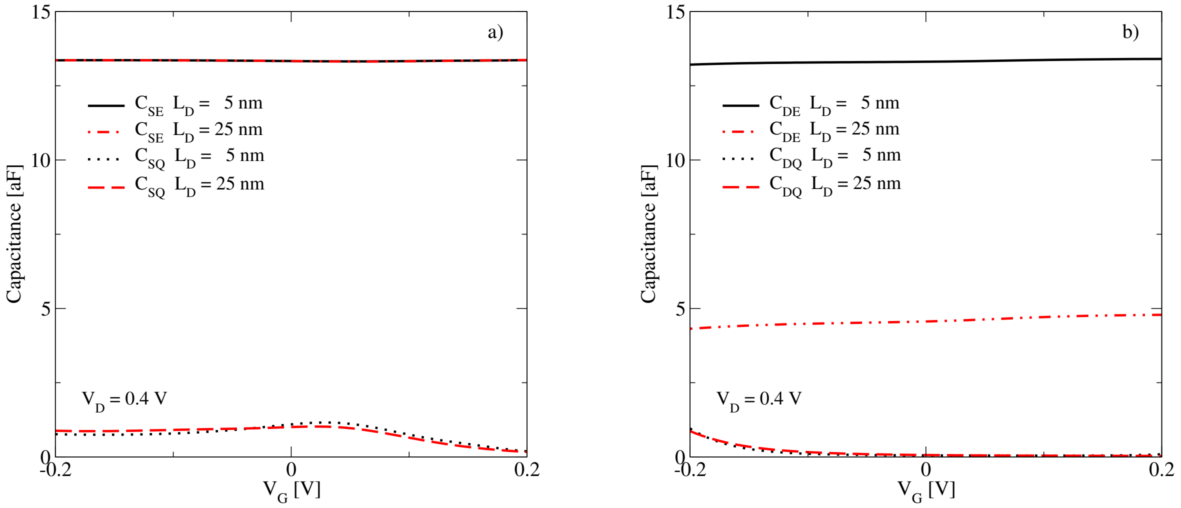

Figure 6: The effect of L_{GD} on the electrostatic and quantum capacitances associated with the a) Source contact, and b) Drain contact

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