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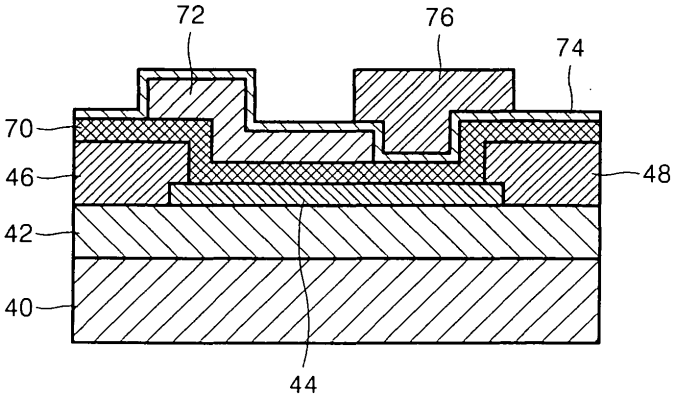
(54) Transistor with carbon nanotube channel and method of manufacturing the same

(57) A transistor with a carbon nanotube channel and a method of manufacturing the same are provided. At least two gate electrodes are formed on a gate insulating layer formed on a carbon nanotube channel and are insulated from each other. Thus, the minority carrier is prevented from flowing into the carbon nanotube channel. Accordingly, it is possible to prevent a leakage current that is generated when both the majority carrier and the minority carrier flow into the carbon nanotube channel. Therefore, characteristics of the transistor can be prevented from being degraded due to the leakage current.

FIG. 4



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Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a semiconductor device with a carbon nanotube channel and a method of manufacturing the same, and more particularly, to a transistor with a carbon nanotube channel and a method of manufacturing the same.

[0002] Carbon nanotubes have a diameter ten thousand times smaller than the diameter of a human hair but are stronger than steel, have both semiconductor and metal properties, and have better performance than silicon. Also, since the carbon nanotubes have mobility seventy times higher than the mobility of silicon at room temperature, the carbon nanotubes can overcome disadvantage of silicon materials, for example, the high noise level of the silicon materials.

[0003] Due to these characteristics, the carbon nanotubes are widely used in semiconductor devices, flat panel displays, batteries, super powerful fibers, biosensors, TV cathode ray tubes (CRTs), and so on. The carbon nanotubes are also used as a nanotweezer that can pinch and release a nano-object.

[0004] A typical application of the carbon nanotubes is a carbon nanotube transistor of which channel is formed of carbon nanotubes.

[0005] In a conventional carbon nanotube transistor (hereinafter, referred to as a conventional transistor), a source electrode and a drain electrode form a Schottky junction together with a carbon nanotube channel.

[0006] Therefore, the conventional transistor can be implemented to have the advantages of the carbon nanotubes by forming the channel of the carbon nanotubes.

[0007] Hereinafter, the problem of the conventional transistor will be described.

[0008] FIG. 1 is a graph illustrating a voltage-current characteristic of a conventional transistor.

[0009] In FIG. 1, first and second graphs G1 and G2 represent simulation results at drain voltages of 1.5 V and 0.9 V, respectively. Symbols O and • represent test results at the drain voltages of 1.5 V and 0.9 V, respectively. It is easily seen that the simulation results and the test results are substantially identical to each other.

[0010] It can be seen that the voltage-current characteristic according to the voltage applied to the drain electrode of the conventional transistor are not different from that of the graph illustrated in FIG. 1.

[0011] FIG. 2 is a graph illustrating voltage-current characteristics of the conventional transistor at the drain voltages of 0.3 V and 0.6 V. In FIG. 2, first and second graphs G11 and G22 represent the voltage-current characteristic at the drain voltages of 0.3 V and 0.6 V, respectively.

[0012] In both of the graphs illustrated in FIGS. 1 and 2, the drain current increases from both sides of a gate voltage at which the drain current is minimal.

[0013] The drain current at the left side of the gate voltage at which the drain current is minimal is caused by holes, while the drain current at the right side of the gate voltage is caused by electrons.

[0014] In the case of a normal transistor, the drain current of a measurement range is caused by the majority carrier, and the drain current caused by the minority carrier can be ignored because it is much lower than the measurement range. For this reason, in the normal transistor, the drain current does not increase at the gate voltage exceeding the voltage at which the drain current is minimal, but has a minimal value.

[0015] In the conventional transistors of FIGS. 1 and 2, however, the drain current again increases at the gate voltage exceeding the voltage at which the drain current is minimal.

[0016] This result indicates the coexistence of the drain currents in the measurement range, which is caused by the holes and electrons. The existence of the drain current caused by the carriers of the opposite polarities within the measurement range means that the current caused by the minority carrier has a large value that cannot be neglected. The drain current caused by the minority carrier is a current caused by a carrier, which must not be measured at the gate voltage at which the drain current is minimal.

[0017] In the conventional transistor, the electrons and the holes flow into the channel as the majority carrier. Therefore, the leakage current may increase and the characteristics of the semiconductor device may be degraded.

SUMMARY OF THE INVENTION

[0018] The present invention provides a transistor with a carbon nanotube channel, which is capable of preventing a minority carrier from flowing into the carbon nanotube channel.

[0019] The present invention also provides a method of manufacturing the transistor.

[0020] According to an aspect of the present invention, there is provided a transistor including: a substrate; a first insulating layer formed on the substrate; first and second metal layers formed on the first insulating layer and spaced apart from each other by a predetermined distance; a nanotube channel formed on the first insulating layer between the first metal layer and the second metal layer, the nanotube channel having one side contacting the first metal layer and the other side contacting the second metal layer; a second insulating layer covering the first and second metal layers and the nanotube channel; and first and second gate electrodes formed on the second insulating layer formed on the nanotube channel, the first and second gate electrodes being electrically insulated from each other.

[0021] The second insulating layer may be a dielectric layer having a dielectric constant higher than that of the first insulating layer.

[0022] The first and second gate electrodes may be

spaced apart from each other by a predetermined distance.

[0023] A third insulating layer is further formed on the second insulating layer to cover the first gate electrode, and the second gate electrode may be formed on the third insulating layer. The first and second gate electrodes may be partially overlapped with each other.

[0024] A third gate electrode may be further formed on the second insulating layer, the third gate electrode being insulated from the first and second gate electrodes.

[0025] According to another aspect of the present invention, there is provided a method of manufacturing a transistor, including: forming a first insulating layer on a substrate; forming a nanotube channel on the first insulating layer; forming first and second metal layers on the first insulating layer, the first metal layer contacting one side of the nanotube channel and the second metal layer contacting the other side of the nanotube channel; forming a second insulating layer on the first and second metal layers and the nanotube channel; and forming first and second gate electrodes on a region of the second insulating layer which contacts the nanotube layer, the first and second gate electrodes being insulated from each other.

[0026] The first and second gate electrodes may be formed with spaced apart from each other by a predetermined distance.

[0027] The forming of the first and second gate electrodes may further include:

> forming the first gate electrode on the second insulating layer; forming a third insulating layer on the second insulating layer such that the first gate electrode is covered; and forming the second gate electrode on the third insulating layer such that the second gate electrode is overlapped with a portion of the first gate electrode.

[0028] A third gate electrode may be further formed on the region of the second insulating layer which contacts the nanotube channel, the third gate electrode being insulated from the first and second gate electrodes.

[0029] According to the present invention, it is possible to prevent the minority carrier from flowing into the nanotube channel. Accordingly, it is possible to prevent the leakage current that is generated when both the majority carrier and the minority carrier flow into the nanotube channel. Therefore, characteristics of the transistor can be prevented from being degraded due to the leakage current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a graph illustrating simulation and experiment results of a voltage-current characteristic of a conventional carbon nanotube transistor;

FIG. 2 is a graph illustrating a voltage-current characteristic of a conventional carbon nanotube transistor based on the result of FIG. 1;

FIG. 3 is a sectional view of a carbon nanotube transistor according to a first embodiment of the present invention;

FIG. 4 is a sectional view of a carbon nanotube transistor according to a second embodiment of the present invention;

FIG. 5 is a graph illustrating a voltage-current characteristic of the carbon nanotube transistor illustrated in FIGS. 3 and 4;

FIGS. 6 through 9 are sectional views illustrating sequential procedures of manufacturing the carbon nanotube transistor of FIG. 3 according to the first embodiment of the present invention; and

FIGS. 10 through 12 are sectional views illustrating sequential procedures of manufacturing a carbon nanotube transistor of FIG. 4 according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0031] A transistor with a carbon nanotube channel and a method of manufacturing the same will now be described in detail with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. In the drawings, the thicknesses of layers and regions are exaggerated for clarity.

[0032] First, a transistor according to the present invention will be described below.

Embodiment 1

[0033] FIG. 3 is a sectional view of a carbon nanotube transistor according to a first embodiment of the present invention.

[0034] Referring to FIG. 3, the carbon nanotube transistor (hereinafter, referred to as a first transistor) includes a substrate 40, and a first insulating layer 42 is formed on the substrate 40. Preferably, the first insulating layer 42 is formed of a material having a lower dielectric constant than that of a second insulating layer 50 (which will be described later). The first insulating layer 42 may be formed of SiO_2. Also, a first metal layer 46, a second metal layer 48, and a carbon nanotube channel 44 are formed on the first insulating layer 42. The first and second metal layers 46 and 48 serve as a source and a drain, respectively. The carbon nanotube channel 44 is formed on the first insulating layer 42 between the first metal layer 46 and the second metal layer 48, and contacts the first and second metal layers 46 and 48. Also, the first transistor includes a second insulating layer 50 and first and second gate electrodes 52 and 54. The second insulating layer 50 serves as a gate insulating layer. Pref-

erably, the second insulating layer 50 is formed of a material having a dielectric constant higher than that of the first insulating layer 42. For example, the second insulating layer 50 may be formed of ZrO_3. The second insulating layer 50 is formed on the first and second metal layers 46 and 48 and the carbon nanotube channel 44. The first and second gate electrodes 52 and 54 are disposed above the carbon nanotube channel 44 and spaced apart from each other by a predetermined distance.

[0035] When predetermined voltages are applied to the first and second gate electrodes 52 and 54 of the first transistor, a potential leakage occurs. That is, even though the first and second gate electrodes 52 and 54 are spaced apart from each other by the predetermined distance, an electric potential generated by the first and second gate electrodes 52 and 54 leaks to boundaries between the second insulating layer 50 and the first and second gate electrodes 52 and 54 because the second insulating layer 50 is formed of a material with a high dielectric constant. Due to this potential leakage, the second insulating layer 50 disposed between the first gate electrode 52 and the second gate electrode 54 is also influenced by the electric potential generated by the first and second gate electrodes 52 and 54. Accordingly, this electric potential is not concentrated only on one region of the carbon nanotube channel 44, but is uniformly distributed over the entire carbon nanotube channel 44.

[0036] In this state, the voltages applied to the first and second gate electrodes 52 and 54 are differently changed to control transmission coefficients of Schottky barriers between the first and second gate electrodes 52 and 54 and the carbon nanotube channel 44. In this manner, an amount of a minority carrier (e.g., a hole in the case of an N-channel transistor) flowing from the second metal layer 48 into the carbon nanotube channel 44 can be controlled.

Embodiment 2

[0037] Like reference numerals in FIGS. 3 and 4 refer to like elements.

[0038] FIG. 4 is a sectional view of a carbon nanotube transistor according to a second embodiment of the present invention.

[0039] Referring to FIG. 4, the carbon nanotube transistor (hereinafter, referred to as a second transistor) includes first and second metal layers 46 and 48 and a carbon nanotube channel 44 on a first insulating layer 42. The first insulating layer 42 may be formed of a silicon oxide layer or a nitride layer. The first and second metal layers 46 and 48 and the carbon nanotube channel 44 are covered with a second insulating layer 70. The second insulating layer 70 may be formed of a dielectric layer (e.g., a zirconium oxide layer) having a dielectric constant higher than that of the first insulating layer 42, or may be formed of a dielectric layer (e.g., a silicon oxide layer) having a dielectric constant equal to or lower than the first insulating layer 42. A first gate electrode 72 is formed on a predetermined region of the second insulating layer 70. The first gate electrode 72 covers a portion of the carbon nanotube channel 44. The first gate electrode 72 can have the same configuration as the first gate electrode 52 in the first embodiment. A third insulating layer 74 is formed on the second insulating layer 70 such that it covers the first gate electrode 72. The third insulating layer 74 is a dielectric layer with a predetermined dielectric constant. Although the third insulating layer 74 is preferably made of the same dielectric layer as the second insulating layer 70, it can also be different from the second insulating layer 70. The second insulating layer 70 between the second metal layer 48 and the first gate electrode 72 is covered with the third insulating layer 74. A second gate electrode 76 is formed on the third insulating layer 74. The first and second gate electrode 72 and 76 constitute a dual gate electrode. Preferably, the second gate electrode 76 is formed between the first gate electrode 72 and the second metal layer 48. Also, the second gate electrode 76 extends over the first gate electrode 72, so that a portion of the second gate electrode 76 is overlapped with a portion of the first gate electrode 72. Thus, the carbon nanotube channel 44 is all covered with the first and second gate electrodes 72 and 76. Consequently, the entire surface of the carbon nanotube channel 44 faces the gate electrodes 72 and 76. Therefore, even when the second insulating layer 70 does not have a dielectric constant higher than the first insulating layer 42, like in the first embodiment, a uniform electric potential can be applied to the carbon nanotube channel 44.

[0040] In this state, the voltages applied to the first and second gate electrodes 72 and 76 are independently controlled. In this manner, it is possible to prevent a minority carrier from flowing into the carbon nanotube channel 44 from the second metal layer 48 serving as the drain.

[0041] Next, the voltage-current characteristics of the first and second transistors will now be described.

[0042] The first and second transistors were configured with N-channel transistors and their voltage-current characteristics were measured. The measurement result is illustrated in FIG. 5.

[0043] In FIG. 5, first and second graphs G31 and G32 represent the voltage-current characteristics when the voltage (V_{g2}) (hereinafter, referred to as a second gate voltage) applied to the second gate electrode 54 or 76 is equal to the drain voltage (V_d), for example V_d = 0.3 V and V_d = 0.6. This case will be referred to as a first case. Third and fourth graphs G33 and G34 represent the voltage-current characteristics when the second gate voltage (V_{g2}) is different from the drain voltage (V_d). This case will be referred to as a second case. Specifically, the third graph G33 represents the voltage-current characteristic when the second gate voltage (V_{g2}) and the drain voltage (V_d) are 0.8 V and 0.3 V, respectively. The fourth graph represents the voltage-current characteristic when the second gate voltage (V_{g2}) and the drain volt-

age (V_d) are 0.8 V and 0.6 V, respectively.

[0044] In the first case, as can be seen from the first and second graphs G31 and G32, the drain current increases as the voltage (hereinafter, referred to as a first gate voltage) applied to the first gate electrode 52 or 72 becomes higher than 0 V, and the drain current decreases as the first gate voltage becomes lower than 0 V. However, when the first gate voltage is lower than 0 V, the drain current does not decreases any more, but maintains a predetermined value as the first gate voltage becomes lower than a predetermined voltage.

[0045] In the second case, as can be seen from the third and fourth graphs G33 and G34 the drain current decreases as the first gate voltage becomes lower than 0 V. As the first gate voltage becomes lower than a predetermined voltage, the drain current does not decrease any more, but maintains a predetermined value.

[0046] In both of the cases, the drain current does not increase when the first gate voltage decreases. These results show that the minority carrier (i.e., the hole) is prevented from flowing into the carbon nanotube channel from the drain. Therefore, the probability that the leakage current can be generated is much , reduced.

[0047] When the first and second transistors are P-channel transistors, the opposite results can be obtained.

[0048] That is, in the case of the P-channel transistors, when predetermined negative voltages are applied to the second gate electrodes 54 and 76 and the drain, the drain current gradually increases as the first gate voltage becomes lower than 0 V. On the contrary, the current decreases as the first gate voltage becomes higher than 0 V, and the drain current maintains a predetermined value as the first gate voltage becomes higher than a predetermined voltage. These results show that the minority carrier (i.e., an electron) is prevented from flowing into the carbon nanotube channel from the drain.

[0049] Next, methods of manufacturing the first and second transistors will be described below.

[0050] First, the method of manufacturing the first transistor will now be described with reference to FIGS. 6 through 9.

[0051] Referring to FIG. 6, a first insulating layer 42 is formed on a substrate 40. The first insulating layer 42 may be formed of a silicon oxide layer, or a dielectric layer with a low dielectric constant. A carbon nanotube channel 44 is formed on a predetermined region of the first insulating layer 42.

[0052] Referring to FIG. 7, first and second metal layers 46 and 48 are formed on the first insulating layer 42. The first metal layer 46 contacts one side of the carbon nanotube channel 44 and the second metal layer 48 contacts the other side of the carbon nanotube channel 44. The first metal layer 46 and the second metal layer 48 serve as a source and a drain, respectively.

[0053] Referring to FIG. 8, a second insulating layer 50 is formed on the first and second metal layers 46 and 48 and the carbon nanotube channel 44. Preferably, the second insulating layer 50 is formed of a dielectric layer having a higher dielectric constant than that of the first insulating layer 42. For example, the second insulating layer 50 may be formed of a zirconium oxide layer (ZrO_3).

[0054] Referring to FIG. 9, first and second gate electrodes 52 and 54 are formed on the second insulating layer 50 by using a photolithography. Both of the first and second gate electrodes 52 and 54 are disposed above the carbon nanotube channel 44 and can be spaced apart from each other by a predetermined distance. Even when the first and second gate electrodes 52 and 54 are separated from each other, since the second insulating layer 50 has a high dielectric constant, electric potential applied to the carbon nanotube channel 44 exposed between the first and second gate electrodes 52 and 54 is equal to electric potential applied to below the first and second gate electrodes 52 and 54.

[0055] Next, the method of manufacturing the second transistor will now be described with reference to FIGS. 10 through 12.

[0056] Referring to FIG. 10, first and second metal layers 46 and 48 and a carbon nanotube channel 44 are formed on a first insulating layer 42 by using the method of manufacturing the first transistor. Then, a second insulating layer 70 is formed to cover the first and second metal layers 46 and 48 and the carbon nanotube channel 44. The second insulating layer 70 may be formed of a silicon oxide layer. Also, the second insulating layer 70 may be formed of a dielectric layer having a dielectric constant equal to or higher than that of the first insulating layer 42. Further, the second insulating layer 70 may be formed of a nitride layer. Then, a first gate electrode 72 is formed on the second insulating layer 70. The forming of the first gate electrode 72 can include depositing a conductive material on the second insulating layer 70, planarizing a surface of the deposited conductive layer, and patterning the planarized conductive layer using a photolithography. Therefore, although the top surface of the first gate electrode 72 is stepped in FIG. 10, the top surface of the first gate electrode 72 can also be flat. Preferably, the first gate electrode 72 is formed above the carbon nanotube channel 44 such that a portion of the carbon nanotube channel 44 is covered.

[0057] Referring to FIG. 11, a third insulating layer 74 is formed to cover the resulting structure, that is, to cover the second insulating layer 70 and the first gate electrode 72. The third insulating layer 74 may be formed of a material layer equal to the second insulating layer 70, or may be other material layers.

[0058] Referring to FIG. 12, a second gate electrode 76 is formed on a predetermined region of the third insulating layer 74. The second gate electrode 76 can be formed using the same manner as in the case of the first gate electrode 72. Preferably, the second gate electrode 76 may be formed to cover the carbon nanotube channel 44 between the first gate electrode 72 and the second metal layer 48. Also, the second gate electrode 76 may be overlapped with a portion of the first gate electrode 72.

[0059] The first and second gates 72 and 76 can be

formed in a reverse sequence. That is, the second gate electrode 76 can be formed on the second insulating layer 70 and the first gate electrode 72 can be formed on the third insulating layer 74. Also, more than two gate electrodes can be provided.

[0060] As described above, the carbon nanotube transistor according to the present invention includes at least two gate electrodes insulated from each other and thus it has a uniform electric potential in the entire region of the channel due to different dielectric constants of the insulating layer between the substrate and the channel and the insulating layer between the channel and the gate electrode. Also, the transmission coefficients of the Schottky barriers between the carbon nanotube channel and the source and drain can be adjusted by applying independent voltages to the gate electrodes. Accordingly, the minority carrier is prevented from flowing into the carbon nanotube channel. Consequently, it is possible to prevent the occurrence of the leakage current that is generated when both the majority carrier and the minority carrier flow into the channel. Therefore, it is possible to prevent characteristic degradation of the transistors due to the leakage current.

[0061] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope of the present invention as defined by the following claims.

Claims

1. A transistor comprising:

a substrate;
a first insulating layer formed on the substrate;
first and second metal layers formed on the first insulating layer and spaced apart from each other by a predetermined distance;
a nanotube channel formed on the first insulating layer between the first and second metal layers, the nanotube channel having one side contacting the first metal layer and the other side contacting the second metal layer;
a second insulating layer covering the first and second metal layers and the nanotube channel; and
first and second gate electrodes formed on the second insulating layer formed on the nanotube channel, the first and second gate electrodes being electrically insulated from each other.

2. The transistor of claim 1, wherein the second insulating layer is a dielectric layer having a dielectric constant higher than that of the first insulating layer.

3. The transistor of claim 1 or 2, wherein the first and second gate electrodes are spaced apart from each other by a predetermined distance.

4. The transistor of claim 1, 2 or 3, further comprising a third insulating layer formed on the second insulating layer to cover the first gate electrode.

5. The transistor of claim 4, wherein the second gate electrode is disposed on the third insulating layer, the first and second gate electrodes being partially overlapped with each other.

6. The transistor of any preceding claim, further comprising a third gate electrode formed on the second insulating layer, the third gate electrode being insulated from the first and second gate electrodes.

7. A method of manufacturing a transistor, comprising:

forming a first insulating layer on a substrate;
forming a nanotube channel on the first insulating layer;
forming first and second metal layers on the first insulating layer, the first metal layer contacting one side of the nanotube channel, the second metal layer contacting the other side of the nanotube channel;
forming a second insulating layer on the first and second metal layers and the nanotube channel; and
forming first and second gate electrodes on a region of the second insulating layer which contacts the nanotube layer, the first and second gate electrodes being insulated from each other.

8. The method of claim 7, wherein the second insulating layer is formed of a dielectric layer having a dielectric constant higher than that of the first insulating layer.

9. The method of claim 7 or 8, wherein the first and second gate electrodes are formed with spaced apart from each other by a predetermined distance.

10. The method of claim 7, 8 or 9, wherein the forming of the first and second gate electrodes further comprises:

forming the first gate electrode on the second insulating layer;
forming a third insulating layer on the second insulating layer such that the first gate electrode is covered; and
forming the second gate electrode on the third insulating layer such that the second gate electrode is overlapped with a portion of the first gate electrode.

11. The method of claim 7, 8, 9 or 10, further comprising forming a third gate electrode on the region of the second insulating layer which contacts the nanotube channel, the third gate electrode being insulated from the first and second gate electrodes.

FIG. 1 (PRIOR ART)

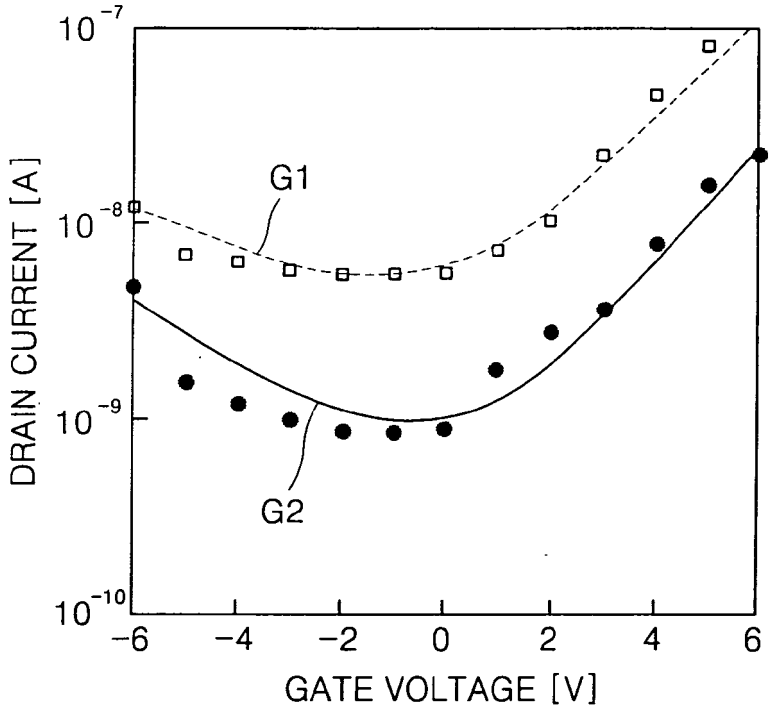


FIG. 2 (PRIOR ART)

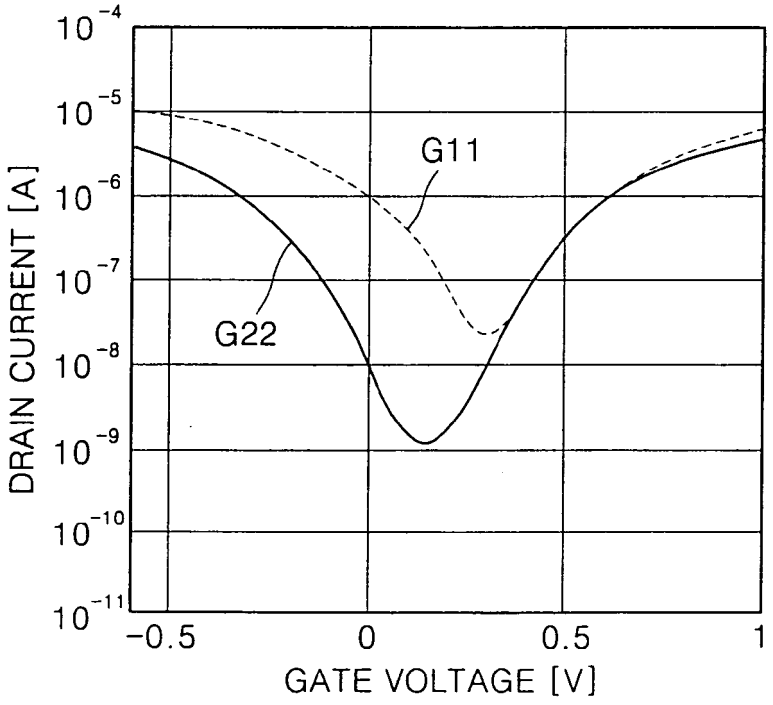


FIG. 3

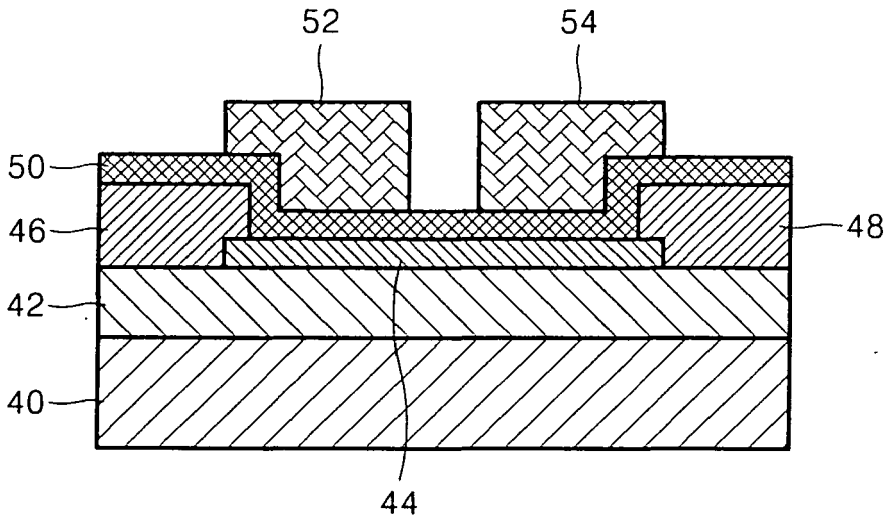


FIG. 4

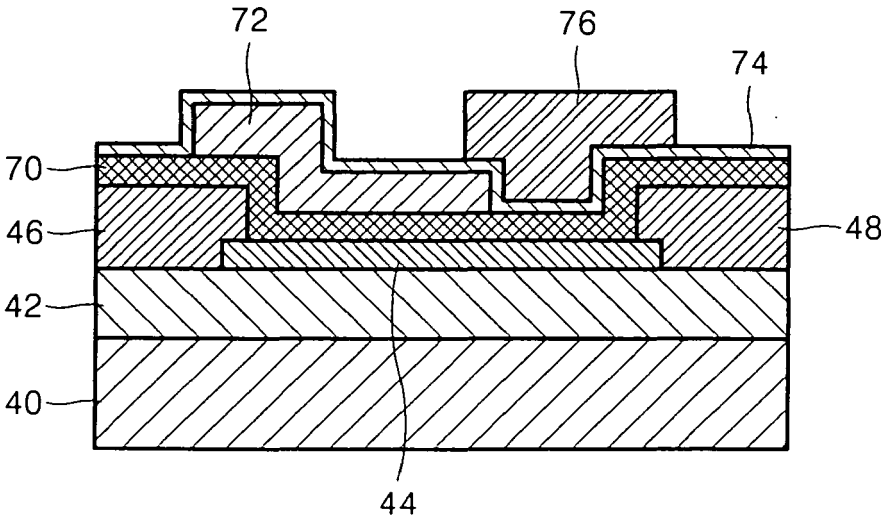


FIG. 5

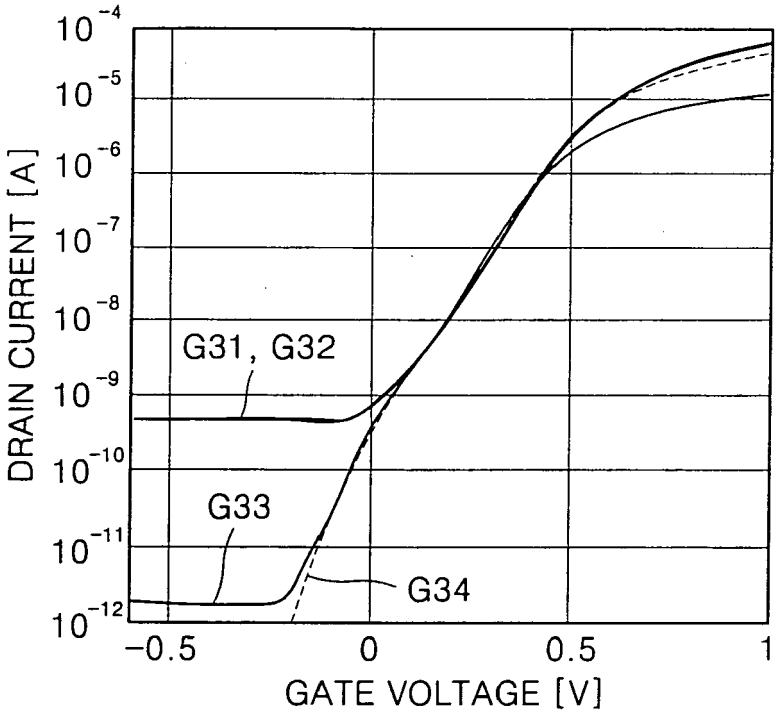

DRAIN CURRENT [A]
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
G31, G32
G33
G34
−0.5
0
0.5
1
GATE VOLTAGE [V]

FIG. 6

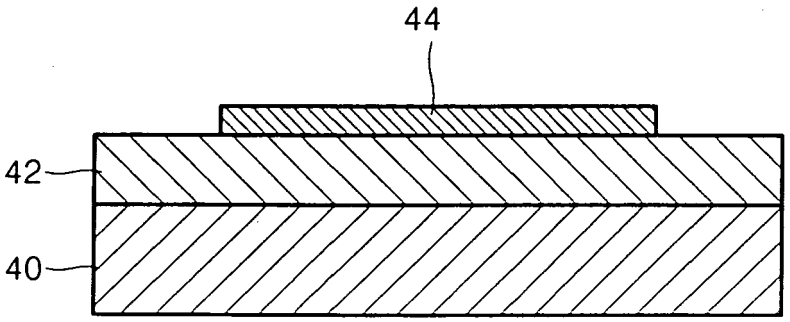

44
42
40

FIG. 7

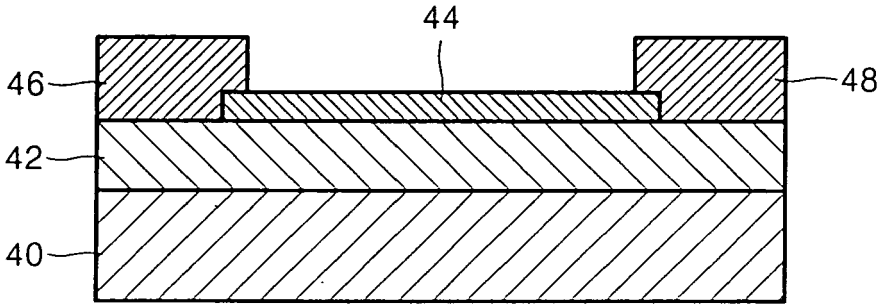


FIG. 8

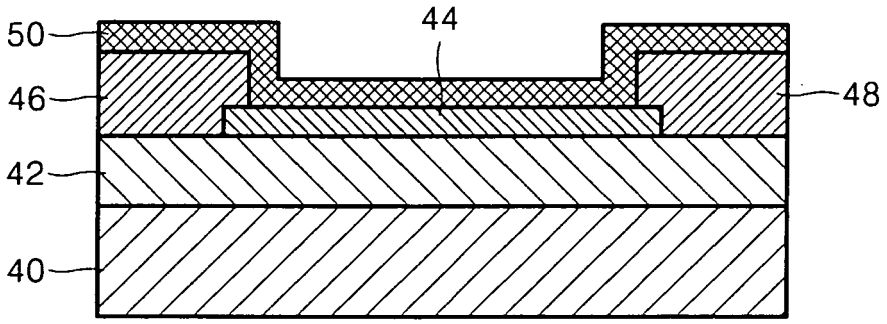


FIG. 9

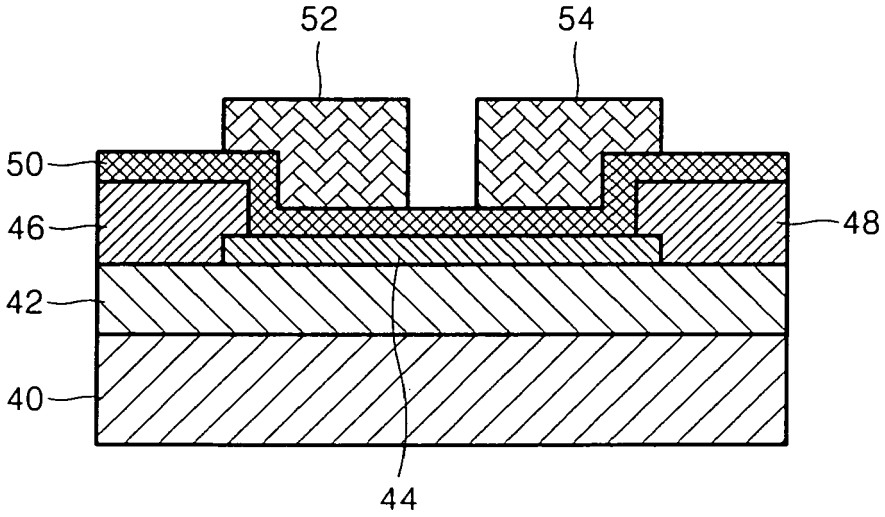


FIG. 10

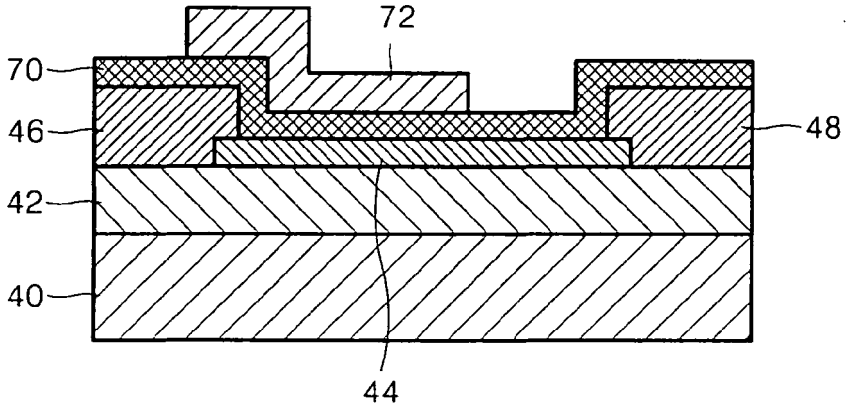


FIG. 11

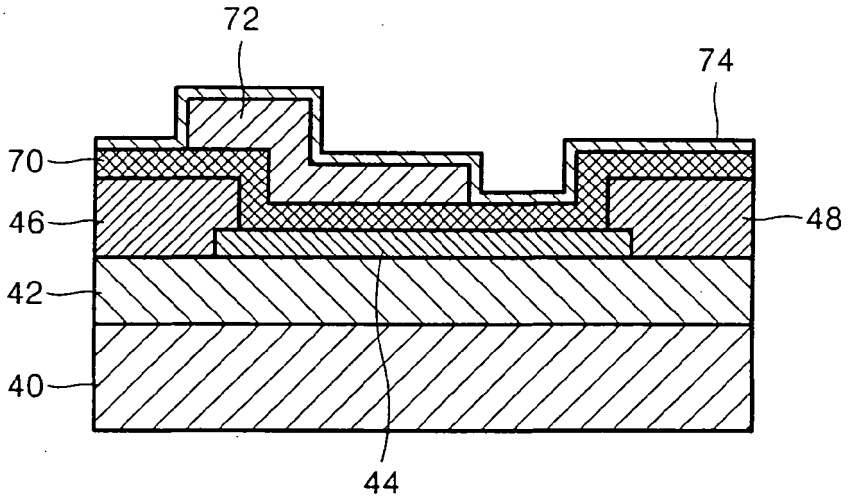
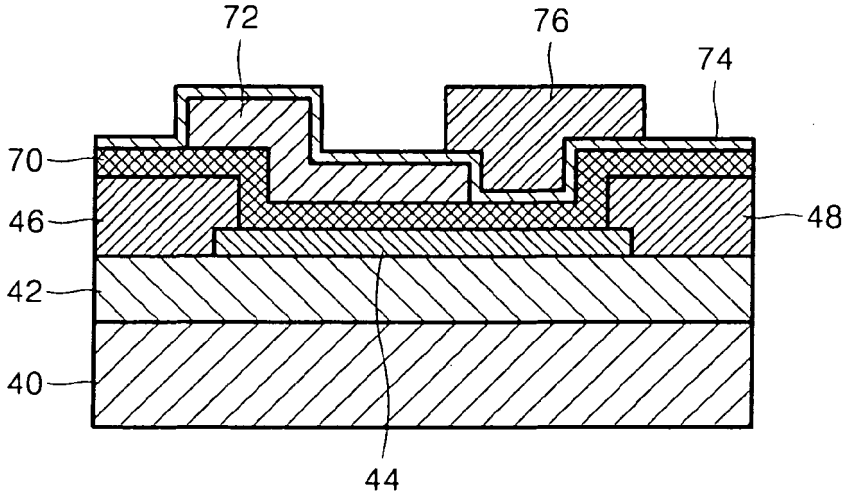


FIG. 12



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