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Microelectronic Engineering 81 (2005) 428–433

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Optimization of Schottky barrier carbon nanotube field effect transistors

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Available online 7 April 2005

Abstract

Carbon nanotube field-effect transistors (CNTFETs) have been studied in recent years as a potential alternative to CMOS devices, because of the capability of ballistic transport. CNTFETs can be fabricated with Ohmic or Schottky type contacts. We focus here on Schottky barrier CNTFETs which operate by modulating the transmission coefficient of carriers through the Schottky barriers at the interface between the metal and the carbon nanotube (CNT). The behavior of these devices has been studied by solving the coupled Schrödinger–Poisson equation system. In agreement with experimental results, simulations indicate the ambipolar behavior of these devices. However, the ambipolar behavior limits the performance of these devices in both on and off regimes. To suppress this effect a double gate structure is proposed. Simulations demonstrate that this structure exhibits improved device characteristics.

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Keywords: Carbon nanotube field effect transistor; Ambipolar behavior; Schottky barrier; Ballistic transport

1. Introduction

Carbon nanotubes (CNTs) have emerged as promising candidates for nanoscale field effect transistors. While early devices have shown poor

device characteristics, high performance devices were achieved recently [1,2]. The contact between metal and CNT can be of Ohmic [3] or Schottky type [4–6]. Schottky contact CNTFETs operate by modulating the transmission coefficient of carriers through the Schottky barriers at the metal–CNT interface [6,7]. A CNTFET can be operated as an n-type or p-type device just by applying positive or negative voltages to the gate and drain contacts [8].

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Two important figures of merit of FETs are the subthreshold slope and the $I_{\text{on}}/I_{\text{off}}$ ratio. To improve these parameters the coupling between gate and CNT should be increased. This can be achieved by using thin high- κ materials as a gate dielectric [2]. The well-known ambipolar behavior of Schottky barrier CNTFETs limits the performance of these devices [8–10]. Due to the ambipolar behavior, the off-current is often intolerably high. The reason of this behavior is that the carrier injection at the source and drain contacts are controlled by the same gate, hence by increasing the coupling between the gate and the CNT the off-current also increases. To suppress the ambipolar behavior a double gate (DG) structure for CNT-FETs has been proposed. Using this structures the carrier injection at the source and drain contacts can be separately controlled. We show that for an n-type device electron injection at the source contact can be controlled via the first gate while the detrimental hole injection at the drain contact can be reduced by the second gate. Thus, the ambipolar behavior of CNTFETs can be completely compensated.

2. Modeling

In order to account for the ballistic transport we solved the coupled Poisson and Schrödinger equations for the Schottky barrier CNTFET [11]:

$$\frac{\partial^2 V}{\partial \rho^2} + \frac{1}{\rho} \frac{\partial V}{\partial \rho} + \frac{\partial^2 V}{\partial z^2} = -\frac{Q}{\epsilon}, \quad (1)$$

$$-\frac{\hbar^2}{2m^*} \frac{\partial^2 \Psi_{s,d}^{n,p}}{\partial z^2} + (U^{n,p} - E) \Psi_{s,d}^{n,p} = 0. \quad (2)$$

We considered an azimuthal symmetric structure, in which the gate surrounds the CNT, such that the Poisson equation (1) is restricted to two-dimensions. In (1), $V(\rho, z)$ is the electrostatic potential, and Q is the space charge density.

In the Schrödinger equation (2), the effective mass was assumed to be $m^* = 0.06m_0$ [7] for both electrons and holes [12]. In (2), superscripts denote the type of the carriers. Subscripts denote the contacts, where ‘s’ stands for the source contact and ‘d’ for the drain contact. For example, Ψ_s^n is the wave

function associated with electrons that have been injected from the source contact, and U^n is the potential energy that is seen by electrons. The Schrödinger equation is only solved on the surface of the tube, and because of azimuthal symmetry, (2) is restricted to one-dimension. By assuming that the electrostatic potential just shifts the CNT band structure, the potential energies for electrons and holes can be written as

$$U^n(z) = -qV(\rho_{\text{CNT}}, z) - \chi_{\text{CNT}}, \quad (3)$$

$$U^p(z) = -U^n(z) + E_g, \quad (4)$$

where E_g , χ_{CNT} and $V(\rho_{\text{CNT}}, z)$ are the CNT band gap, the CNT electron affinity and the electrostatic potential along the surface of the CNT. All our calculations assume a CNT with 0.6 eV band gap, corresponding to a diameter of 1.4 nm [7].

The space charge density in (1) is calculated as

$$Q = \frac{q(p-n)\delta(\rho - \rho_{\text{CNT}})}{2\pi\rho}, \quad (5)$$

where n and p are total electron and hole concentrations per unit length. In (5), δ is the Dirac delta function in cylindrical coordinates. Including the source and drain injection components, the total electron concentration in the CNT is calculated as

$$n = \frac{4}{2\pi} \int f_s |\Psi_s^n|^2 dk_s + \frac{4}{2\pi} \int f_d |\Psi_d^n|^2 dk_d, \quad (6)$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts. In this work, we focus on ambipolar devices, where the metal Fermi level is located in the middle of the CNT band gap at each contact. The total hole concentration in the CNT is also calculated analogously. Carriers were taken into account by means of a sheet charge distributed uniformly over the surface of the CNT [11]. For considering the effect of this sheet charge in a applicable way for simulations, the matching condition (7) across the CNT surface was used:

$$\epsilon_{\text{ins}} \left. \frac{\partial V}{\partial \rho} \right|_{\rho_{\text{CNT}}^+} - \epsilon_{\text{CNT}} \left. \frac{\partial V}{\partial \rho} \right|_{\rho_{\text{CNT}}^-} = -\frac{q(p-n)}{2\pi\rho_{\text{CNT}}}. \quad (7)$$

The CNT is presumed to have a free-space relative permittivity [13].

Carriers current is calculated by means of the Landauer–Büttiker formula [14]:

$$I^{n,p} = \frac{4q}{h} \int [f_s^{n,p}(E) - f_d^{n,p}(E)] TC^{n,p}(E) dE, \quad (8)$$

where $TC^{n,p}(E)$ are the transmission coefficients of electrons and holes through the device. The factor 4 in (6) and (8) stems from the twofold band and twofold spin degeneracy [6].

MINIMOS-NT is a semiclassical device simulator [15] which has been enhanced to perform quantum simulations [16] by solving the coupled Schrödinger–Poisson equation system. Since a simple iteration by itself does not converge, a damping parameter α is introduced. At the $(k + 1)$ th iteration the Schrödinger equation is solved using the electrostatic potential from the last iteration V^k and the new space charge density Q^{k+1} is calculated. The Poisson equation is then solved by using Q^{k+1} and an intermediate new electrostatic potential is calculated V_{int}^{k+1} . Finally V^{k+1} is calculated as

$$V^{k+1} = \alpha V_{int}^{k+1} + (1 - \alpha)V^k, \quad (9)$$

where $0 < \alpha < 1$. Successive iteration continues until appropriate convergence is reached.

3. Single gate structure

A single gate structure (SG) is shown in Fig. 1. Current–voltage characteristics of this structure

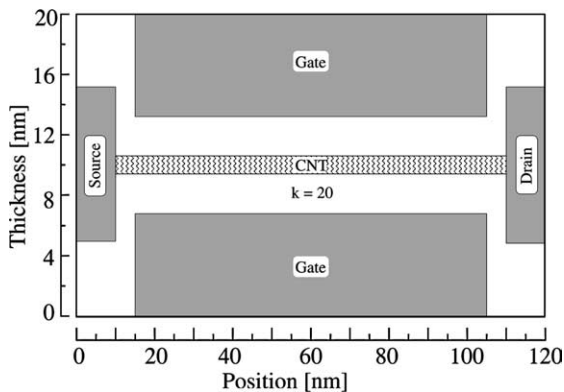


Fig. 1. 2D sketch of the SG structure.

are shown in Figs. 3 and 4. The ambipolar behavior of this structure is clearly observed, in agreement with experimental [4,9] and theoretical [10,17] results. To understand this behavior the band edge profile is shown in Fig. 5. In n-type devices, applying a positive drain voltage higher than the gate voltage suppresses the Schottky barrier at the drain contact and consequently increases hole injection at this contact. In the off regime this results in a high off-current, as seen in Fig. 4. In the on regime the drain current increases with increasing the drain voltage, rather than showing saturation, as shown in Fig. 3. This ambipolar

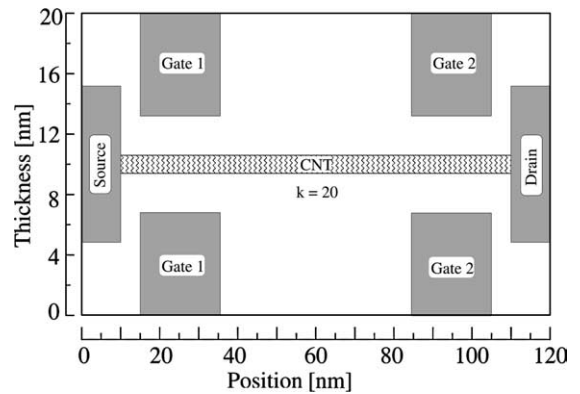


Fig. 2. 2D sketch of the DG structure.

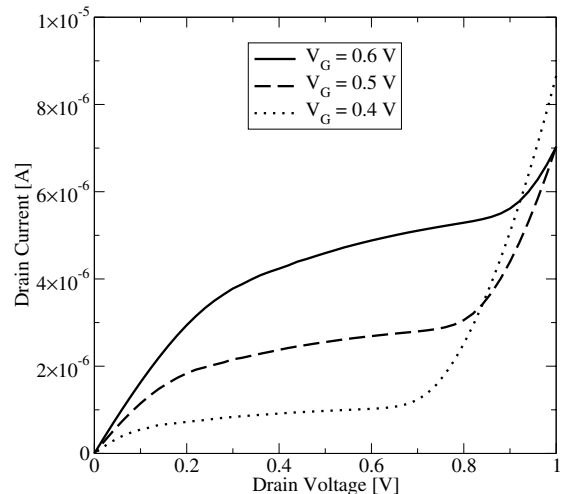


Fig. 3. I – V characteristics of the SG structure.

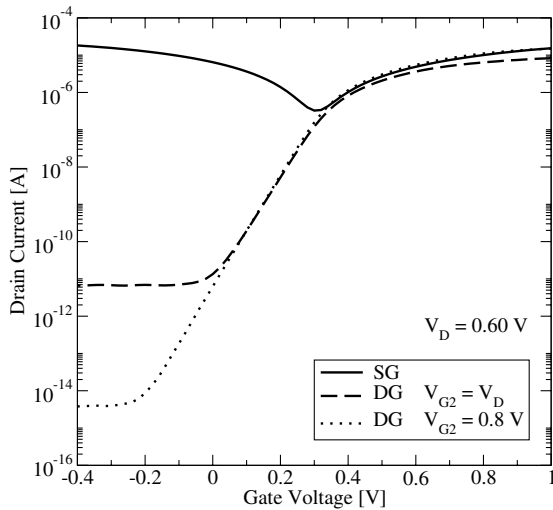


Fig. 4. *I*–*V* characteristics of the SG and DG structures.

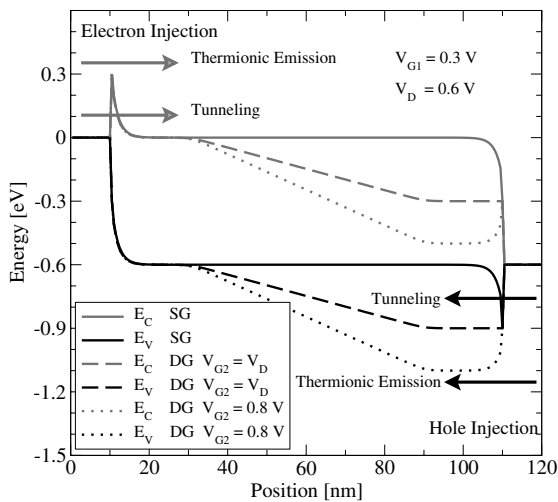


Fig. 5. Band edge profile of the SG and DG structures.

behavior limits the performance of the device in both on and off regimes.

Due to the ambipolar behavior of CNTFETs the off-current is intolerably high. The origin of the ambipolar behavior is that the carrier injection at the source and drain contact is controlled by the same gate. This implies that if the coupling between the gate and the CNT increases—by using thin high- κ materials as gate dielectric [2]—not only the subthreshold slope and the on-current, but also the off-current increases.

4. Double gate structure

To avoid the ambipolar behavior of CNTFETs and improve the performance of these devices, we propose a double gate structure (DG) as shown in Fig. 2. The first gate controls the carrier injection at the source contact, which determines the on-current, and the second one controls the carrier injection at the drain contact, which determines the off-current. This implies that in DG structures by increasing the coupling between the gates and the CNT the on-current will increase while the off-current will decrease.

If the drain voltage is applied to the second gate, at any drain voltage the band edge profile near the drain contact will be flat, as shown in Fig. 5. In consequence the tunneling current of holes at the drain contact is suppressed and there is only some negligible thermionic emission current of holes, see Fig. 4. While electron injection at the source contact can be controlled through the first gate, the second gate suppresses parasitic hole current at the drain contact. The same discussion holds for p-type devices. By applying negative voltages to the first gate, hole injection at the source contact can be controlled and the second gate suppresses parasitic electron current at the drain contact.

By applying a voltage higher than the maximum drain voltage to the second gate, see Fig. 5, thermionic emission of holes at the drain contact will decrease exponentially and consequently a lower off current can be achieved, see Fig. 4.

As seen in Fig. 6, if the second gate is biased at the drain voltage, the drain current will not increase considerably until the drain voltage reaches the first gate voltage. The reason of this behavior is that the injected carriers at the source contact see a thick barrier near the drain contact until the drain voltage reaches a voltage higher than the first gate voltage, see Fig. 7. If the second gate is biased at a voltage higher than the maximum drain voltage, the injected carries at the source contact see a thin barrier even at low drain voltages while holes at the drain contact see a thick barrier.

Regarding the separation between the two gates several parameters should be considered: By decreasing this separation, the parasitic capacitance

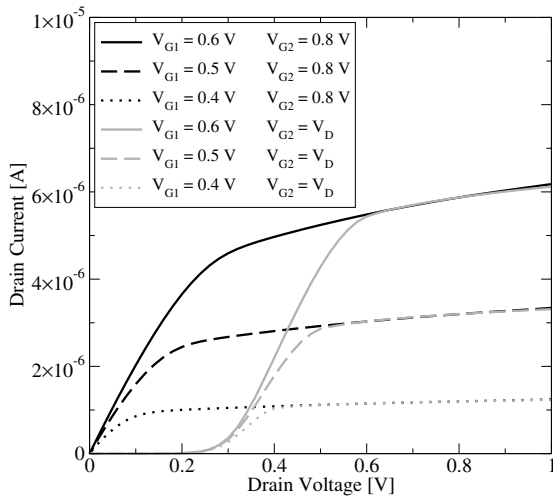


Fig. 6. I - V characteristics of the DG structure.

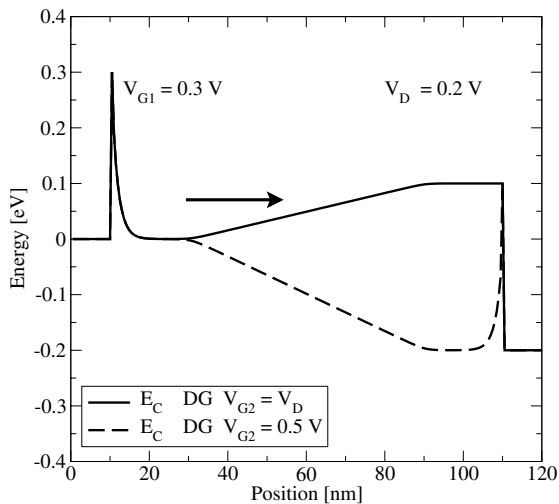


Fig. 7. Conduction band edge profile of the DG structure.

between the gates increases which deteriorates the frequency response of the device. Also because of narrow band gap in CNTs, at the certain operating voltages by decreasing this distance the band to band tunneling current will increase which affects the off current.

The comparison of current–voltage characteristics of the SG and DG structures, shows that the proposed DG structure has excellent device characteristics, which is necessary for future nano-electronic applications.

In [18] an split gate structure has been implemented. Although this structure was used as a pn diode, it shows that by controlling the band edge profile near the source and drain contacts better device characteristics can be achieved.

5. Conclusion

To improve the performance of CNTFETs, the ambipolar behavior of these devices should be suppressed. For this purpose a DG structure was proposed. In the DG structure, the first gate controls the carrier injection at the source contact and the second gate controls parasitic carrier injection at the drain contact. In fact the first gate controls the on-current and the second gate controls the off-current. Either the drain voltage or a voltage higher than the maximum drain voltage can be applied to the second gate. It is of advantage to apply the drain voltage to the second gate, because parasitic capacitances between the second gate and the drain contact are avoided, no separate voltage source for the second gate is needed, and the fabrication is more feasible. The minimum off-current is limited to the thermionic emission current over the Schottky barrier. The drain current will not increase considerably until the drain voltage reaches a voltage higher than the first gate voltage. By applying a voltage higher than the maximum drain voltage to the second gate, a very high I_{on}/I_{off} ratio can be obtained. However, for both of these methods the I_{on}/I_{off} ratio exceeds five orders of magnitude which is satisfactory for conventional logic applications.

Acknowledgement

This work was partly supported by the National Program for Tera-level Nano-devices of the Korea Ministry of Science and Technology as one of the 21st Century Frontier Programs.

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