Optimization of Single-Gate Carbon-Nanotube Field-Effect Transistors

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***Abstract*—The performance of Schottky-barrier carbon-nanotube field-effect transistors (CNTFETs) critically depends on the device geometry. Asymmetric gate contacts, the drain and source contact thickness, and inhomogenous dielectrics above and below the nanotube influence the device operation. An optimizer has been used to extract geometries with steep subthreshold slope and high I_{on}/I_{off} ratio. It is found that the best performance improvements can be achieved using asymmetric gates centered above the source contact, where the optimum position and length of the gate contact varies with the oxide thickness. The main advantages of geometries with asymmetric gate contacts are the increased I_{on}/I_{off} ratio and the fact that the gate voltage required to attain minimum drain current is shifted toward zero, whereas symmetric geometries require $V_g = V_d/2$. Our results suggest that the subthreshold slope of single-gate CNTFETs scales linearly with the gate–oxide thickness and can be reduced by a factor of two reaching a value below 100 mV/dec for devices with oxide thicknesses smaller than 5 nm by geometry optimization.**

***Index Terms*—Carbon nanotubes (CNTs), field-effect transistors (FETs), nanoelectronics, optimization methods.**

I. Introduction

SEMICONDUCTOR device technology using nanocarbon materials in semiconductor chip wiring is receiving accelerated development. This trend is mainly caused by their overall properties and not only by their small size. The electrical properties of carbon nanotubes (CNTs) can rival, or even exceed, the best metals or semiconductors known. The electrical behavior is a consequence of the electronic band structure, which depends on the chiralty and radius of the nanotube. Metallic nanotubes are promising for interconnects and vias [1] in integrated circuits because of their high electrical and thermal conductivity, whereas semiconducting tubes have emerged as possible candidates for nanoscale carbon-nanotube field-effect transistors (CNTFETs) with the potential for ultra-large scale integration (ULSI) [2]–[5].

A critical issue for conventional CNTFET geometries is the required scaling of the drain voltage V_d as the gate–oxide thickness (T_{ox}) is decreased. The off-current (I_{off}) rises significantly when the absolute value of the drain current is increased leading to a decrease of I_{on}/I_{off}. This effect can be understood within the Schottky band model, where the subthreshold characteristics of CNTFETs with symmetric geometries, i.e., symmetric gate, source, and drain contacts, is symmetric around the gate voltage $V_{g,off} = V_d/2$ [6]. At this point, the barrier for electrons is the same as for holes and the minimum current will flow through the nanotube. The electron current rises with V_g, whereas the hole current rises with $V_d - V_g$. For a large V_d, the resulting gate voltage $V_{g,off}$ is large enough to suppress the Schottky barriers at the nanotube contacts and, thus, large I_{off} currents can flow. This effect will occur whenever the devices are scaled to smaller size, or high-κ gate oxides increase the electric field at the metal nanotube contacts.

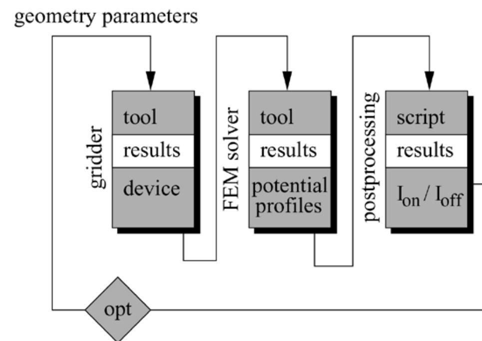

Fig. 1. Diagram of the optimization tool flow.

Surprising effects regarding to the scaling of the performance of CNTFETs have been recently observed [7]–[10]. It was shown that dielectrics with different permittivity above and below the nanotube influence the device operation. Furthermore, it was demonstrated that asymmetric geometries with gate contacts located only in the vicinity of the source contact can enhance device performance. These unexpected scaling trends can be well understood, assuming that the transistor action is caused by the modulation of Schottky barriers at the metal–nanotube contact. The barriers can be thinned by applying gate voltages sufficiently large to allow tunneling of electrons or holes.

In this study, an optimization setup (see Fig. 1) is used to study the scaling behavior of CNTFETs. The device geometry and permittivity of the dielectric material surrounding the nanotube is optimized to extract structures with a steep subthreshold slope $S = (d\log_{10} I/dV_g)^{-1}$ and a high I_{on}/I_{off} ratio. The one-dimensional transport model based on the Landauer–Büttiker formula and the simulation setup are discussed in Section II. The influence of the contact geometry and the effect of

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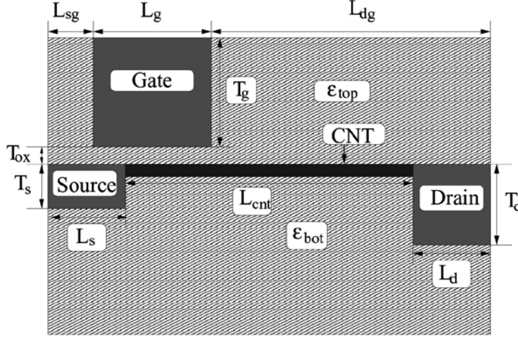

Fig. 2. Device geometry with simulation parameters.

dielectrics on device performance are addressed and the results from geometry optimization are presented in Section III.

II. Device Optimization

This paper focuses on single-gated device geometries, comparable to conventional MOSFETs with a single-walled nanotube replacing the silicon channel. We optimized this geometry (see Fig. 2) with respect to six parameters, which are: 1) the position and length of the gate contact (by varying $L_{\rm dg}, L_{\rm sg}$); 2) the thickness of source and drain contact (T_s, T_d); and 3) the permittivity of the top and bottom dielectric $(\epsilon_{\rm top}, \epsilon_{\rm bot})$.

The simulation framework SIESTA [12] was used for the optimization. It provides various optimizers that can be chosen to fit best for the problems at hand. The optimizer used for this study is a genetic optimizer that relies on the theory of evolutionary computation and genetic algorithms. The population of the n-tuples of free parameters is chosen randomly with respect to a Gaussian normal distribution where a large set of distribution, and generation parameters can be configured and tuned for various kinds of problems. Furthermore, the simulation of the population was distributed on a computer cluster to significantly decrease the optimization time.

At start time, SIESTA provides the initial values of the free geometry parameters ($T_s, T_d, T_{\rm ox}, L_{\rm sg}, L_{\rm dg}, \epsilon_{\rm top}$, and $\epsilon_{\rm bot}$), as shown in Fig. 1. These values are passed to the electrostatic solver, which calculates the potential profile for a device in the on and off states. For the optimization of the $I_{\rm on}/I_{\rm off}$ ratio, $I_{\rm on}/I_{\rm off}$ is defined as the ratio between the current at $V_g = 1.5$ V and $V_g = 0$ V. Afterwards, the potential along the nanotube for the two states is extracted and $I_{\rm on}$ and $I_{\rm off}$ are calculated. The $I_{\rm on}/I_{\rm off}$ ratio is submitted to the optimizer, which generates the next n-tuple of free parameters to improve this value. The subthreshold slope was optimized analogously, submitting the ratio of the current at $V_g = 0.3$ V and $V_g = 0.2$ V to the optimizer. Since the regime where the subthreshold slope can be extracted when plotting $\log_{10} I$ over V_g depends on the geometry of the structure, the slope was re-extracted afterwards from the optimized structures in a region where the slope was linear.

Electrostatic simulations were performed using the Smart Analysis Package [13]. This software contains a finite-element solver to obtain the distributions of the potential and the electric field in the simulation domain. Electrical contacts with given voltages are represented by Dirichlet boundary conditions. For the rest of the border of the simulation domain, a homogeneous Neumann boundary condition is assumed. The nonuniform triangular grid is refined at the metal–nanotube interface, where the Schottky barriers control the current through the tube. The resulting potential profile along the tube is used for the calculation of the transmission coefficient in a postprocessing step.

A. Transport Modeling

Coherent transport in the nanotube is described by the Landauer–Büttiker formula. The drain current through the nanotube is given by an integration in the energy domain [14]

$$I_d = \frac{4q}{h} \int \big[f_s(E) - f_d(E)\big] \mathrm{TC}(E)\, dE \qquad (1)$$

where $f_{s,d}$ are equilibrium Fermi functions at the source and drain contacts, and $\mathrm{TC}(E)$ is the transmission coefficient. Note that, even if $\mathrm{TC}(E) = 1$, the resistance of the tube is given by $h/(4q^2) \approx 6.5$ kΩ, assuming two conduction channels in the tube. This quantum mechanical resistance stems from the difference of possible conduction channels in the tube and the macroscopic metal contact.

Accounting for an idealized CNT band structure [15], which is symmetric around the Fermi level, the first conduction (valence) band is given by

$$E(k) = \pm \frac{\sqrt{3} a \gamma_0}{2} \sqrt{\left(\frac{1}{-3\rho_{\rm cnt}}\right)^2 + k^2} \qquad (2)$$

where a denotes the lattice constant, $\gamma_0 = 2.5$ eV is the transfer integral, $\rho_{\rm cnt}$ is the nanotube radius, and k denotes the wave vector along the CNT radius. The transmission coefficient to states of the first conduction (valence) band is estimated using the Wentzel–Kramers–Brillouin (WKB) approximation [16]

$$\ln \mathrm{TC}(E) = -2 \int \frac{\mathcal{E}_g}{\sqrt{3} a \gamma_0} \sqrt{1 - \left(\frac{E + q\phi(x)}{\mathcal{E}_g/2}\right)^2}\, dx. \qquad (3)$$

Here, $\mathcal{E}_g$ is the CNT bandgap energy and $\phi(x)$ is the electrostatic potential along the CNT. The integration is performed within the classical turning points.

For self-consistent simulations of CNTFETs, we followed the approach of John *et al.* [17], [18] solving a one-dimensional open-boundary Schrödinger equation

$$-\frac{\hbar^2}{2m^*} \frac{\partial^2 \Psi_s}{\partial x^2} + (U - \mathcal{E})\Psi_s = 0 \qquad (4)$$

where Ψ_s is the wave function of a carrier with energy $\mathcal{E}$ and effective mass m^*. The local potential energy U is given by $U_e = -q\phi(x) - \chi_{\rm cnt}$, and $U_h = -U_e + \mathcal{E}_g$ for holes, with $\chi_{\rm cnt}$ denoting the electron affinity. The charge induced on the CNT can be calculated from

$$\begin{aligned} n_{s,d} &= \frac{4}{2\pi} \int f_{s,d} |\Psi_{s,d}|^2\, dk_{s,d} \\ &= \int \frac{\sqrt{2m^*}}{\pi\hbar\sqrt{\mathcal{E}_{s,d}}} f_{s,d} |\Psi_{s,d}|^2\, d\mathcal{E}_{s,d}. \end{aligned} \qquad (5)$$

Here, $n_{s,d}$ denote the concentrations induced from the source and drain side, respectively. The factor 4 in (1) and (5) stems

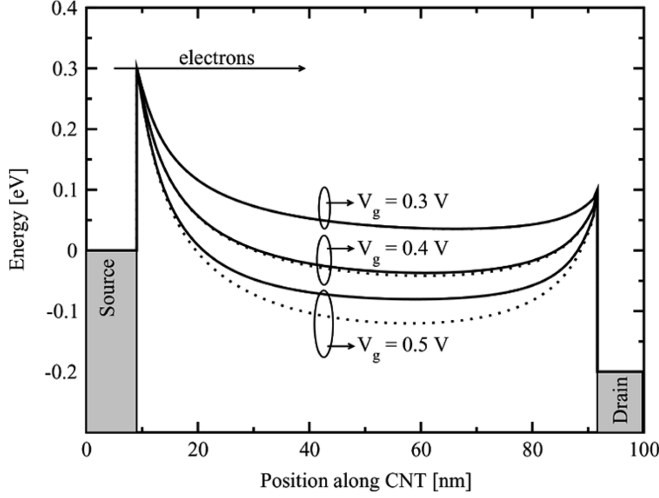

Fig. 3. Conduction band edge for three gate voltages from self-consistent (solid lines) and nonself-consistent calculations at $V_d = 0.2$ V.

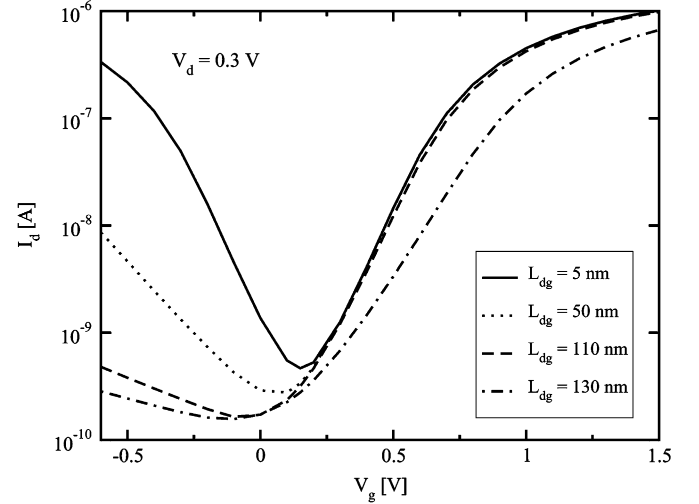

Fig. 4. Subthreshold characteristics for different gate contact geometries. The solid line shows the drain current I_d for a symmetric geometry with $L_{\rm dg} = L_{\rm sg} = 5$ nm, whereas the other lines correspond to geometries with an increased distance between the gate and drain contact.

from the twofold band and twofold spin degeneracy [19]. The total carrier concentrations $n = n_s + n_d$ and $p = p_s + p_d$ enter the Poisson equation

$$\nabla\epsilon\nabla\phi = -\frac{q(p-n)\delta(\rho-\rho_{\rm cnt})}{2\pi\rho} \tag{6}$$

where δ denotes the Dirac delta function describing the CNT charge density. Carriers were considered as charged sheets with the charges being distributed uniformly around the surface of the nanotube. The Poisson equation is solved self-consistently with the Schrödinger equation (4) using the general-purpose device simulator MINIMOS-NT [20]. Band structure modifications due to the potential drop across the nanotube diameter occurring in planar geometries have been neglected since the potential variation across the nanotube diameter is below 0.8 V [21], [22].

B. Simulation Setup

For device optimization a $(16, 0)$ nanotube with a length of 120 nm was assumed to connect the source and drain contact of the CNTFET. The nanotube's bandgap $\mathcal{E}_g$ and radius $\rho_{\rm cnt}$ were set to 0.6 eV and 0.63 nm, respectively. For the effective mass m^*, a value of $0.06m_0$ was chosen, both for electrons and holes [24].

The length of the source and drain contact and the overall thickness of the simulation domain were the only geometry parameters fixed during the optimization process ($L_s = L_d = 10$ nm, $T = 100$ nm). We focus on midgap Schottky barriers where the Fermi level of the metal contacts is located in the middle of the CNT bandgap. Charge on the CNT was neglected during the optimization. Setting n and p to zero in (6), only (1) and (6) have to be solved in a single optimization step. For positive-barrier devices of the type considered here, this leads to only a very slight overestimation of the current (≈10%) with respect to that predicted by a fully self-consistent solution [17], even when the device is in the on regime [7], [11]. In Fig. 3, the band bending along the CNT is plotted for a self-consistent simulation and a simulation where the charge on the CNT has been neglected. It can be seen that the Schottky barriers at the source and drain side are not significantly changed in the energy range of significant tunneling current.

III. SIMULATION RESULTS

In order to get a better understanding of the optimization results, the influence of size and location of the gate contact, size of drain and source contact, and the permittivity of the top and bottom dielectric on the device performance are addressed independently here. Our results for symmetric geometries show good agreement with recent simulations [6]–[8], where these parameters have been investigated separately. The results of the CNTFET geometry optimization for several fixed gate oxide thicknesses are then presented. Finally, we compare important figures-of-merit like the subthreshold slope S and the $I_{\rm on}/I_{\rm off}$ ratio of optimized geometries with values from conventional geometries from both simulation and experiments.

A. Effect of the Gate Geometry

CNTFETs with symmetric gate contacts show ambipolar behavior leading to a symmetric subthreshold characteristics, drawn as a solid line in Fig. 4. When $V_g = V_d/2$, the current through the nanotube reaches its minimum [6]. The amount of electron tunneling from the source side is equal to the hole tunneling from the drain side for this gate bias. Larger gate voltages allow more electron tunneling from the source side, whereas the hole current from the drain is essentially suppressed. When $V_g < V_d/2$, hole tunneling is favored and the electron current is suppressed, whereas for $V_g > V_d/2$, electron current dominates over hole current.

When using asymmetric structures the subthreshold characteristics becomes asymmetric. In Fig. 4, the subthreshold characteristics of geometries with $L_{\rm dg} > 5$ nm are plotted. While $L_{\rm sg} = 5$ nm is kept constant, the length of the gate contact is decreased by increasing $L_{\rm dg}$ and, thus, the control of the gate over the CNT at the drain side is partially lost. This geometry modification directly affects the subthreshold characteristics where

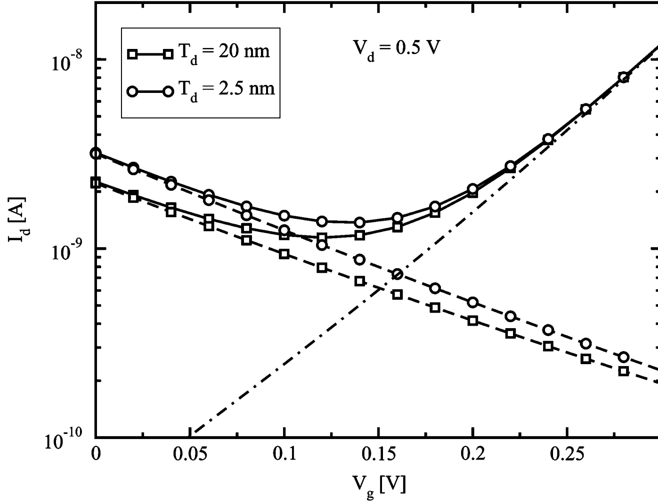

Fig. 5. Drain current as a function of V_g for a drain thickness T_d of 20 (squares) and 2.5 nm (circles). Solid lines are used for the total current and dashed lines for the hole current, which is reduced in the case of large T_d (squares). The electron current (dashed–dotted line) is the same for both cases.

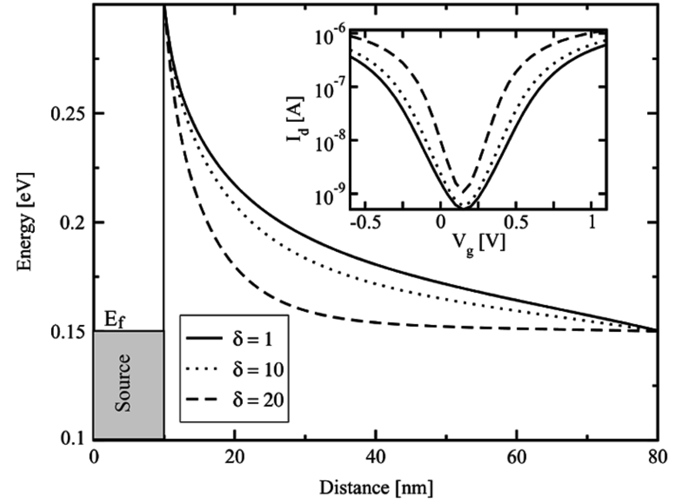

Fig. 6. Conduction band edge near the source contact for a device with $T_{\rm ox} = 10$ nm, plotted for three different ratios $\delta = \epsilon_{\rm top}/\epsilon_{\rm bot}$. For higher δ, the energy barrier is thinned. The inset shows the impact of inhomogenous dielectrics on the subthreshold characteristics at $V_d = 0.3$ V.

a lower hole current can be observed at small or negative gate voltages. At the same time, the electron current, which dominates for $V_g > V_d/2$, is insensitive to the different gate placement. A decrease of electron current takes place only if the overall gate length is below a critical value. This is illustrated in Fig. 4, where the subthreshold characteristics for a geometry with $L_{\rm dg} = 130$ nm; thus having a gate length of only 5 nm is plotted. The decrease of the subthreshold slope is noticeable, but due to fringing fields from the gate contact, the device can still be turned on. From Fig. 4, it can also be seen that the gate voltage leading to a minimum drain current moves toward zero as the gate length decreases. Thus, asymmetric structures have the advantage that the $I_{\rm off}$ current is located around 0 V, which is more practical for real-life applications. Generally, it can be observed that $I_{\rm on}$ and the subthreshold slope are only weakly influenced by the location of the gate as long as $L_{\rm dg}$ stays beyond a critical value, whereas $I_{\rm off}$ can be reduced, which results in a higher $I_{\rm on}/I_{\rm off}$ ratio.

B. Effect of Drain and Source Contact Geometries

To achieve low $I_{\rm off}$, it is necessary to have large tunneling barriers for both electrons and holes at the source and drain contact in the off state. CNTFETs with thin needle-like contacts have thinner tunneling barriers than devices with large contacts for source and drain, which can be understood from simple electrostatic arguments. Hence, large contacts have broader barriers and are able to reduce $I_{\rm off}$. From Fig. 5, it can be seen how the hole current is reduced for a device with $T_d = 20$ nm, as compared to a device with a needle-like drain contact with $T_d = 2.5$ nm. For both geometries, $T_s = 2.5$ nm, and it can be seen that the electron current is not influenced by the increase of T_d. In the same manner as $I_{\rm off}$ can be reduced by increasing the drain contact thickness, the tunneling barrier for electrons at the source side can be reduced using thin source contacts, resulting in an increase of $I_{\rm on}$.

C. Effect of Inhomogenous Dielectrics

It has been reported that using different κ materials above and below the CNT increases the subthreshold slope of CNTFETs [7], where this effect was explained from the refraction law for electric-field lines at interfaces of materials with different permittivities

$$\frac{\tan\alpha_{\rm top}}{\epsilon_{\rm top}} = \frac{\tan\alpha_{\rm bot}}{\epsilon_{\rm bot}}. \tag{7}$$

Here, $\alpha_{\rm top}$ and $\alpha_{\rm bot}$ are the incident field line angles between normal to the interface between a top and bottom dielectric. Equation (7) is valid when the charge on the tube is neglected and results in a lowering of the barrier when using materials with different permittivity above and below the tube. The effect is more pronounced for thick gate oxides and becomes stronger as the ratio $\delta = \epsilon_{\rm top}/\epsilon_{\rm bot}$ is increased (see Fig. 6). The inset of Fig. 6 shows that the reduction of the barrier caused by $\delta > 1$ results in higher drive currents. Furthermore, it can be observed that the overall subthreshold characteristics is shifted upwards and the subthreshold slope increases when increasing δ. On the other hand, side $I_{\rm on}/I_{\rm off}$ is not influenced by this effect.

For CNTFETs with symmetric gate geometries, by increasing δ, the potential barrier for holes tunneling from the drain side is reduced in the same manner as the tunneling barrier for electrons is reduced. This leads to high off currents at large V_d and requires a proper scaling of V_d. To the contrary, the hole tunneling of CNTFETs can be suppressed with an asymmetric contact geometry and inhomogenous dielectrics can improve device characteristics for a large range of drain voltages.

D. Optimized Geometries

Finally, we present results of the device optimization of CNTFETs with different gate–oxide thicknesses. In the optimization setup, we fixed $T_{\rm ox}$ and varied the other geometry parameters in order to find optimized structures for a given $T_{\rm ox}$.

We find that devices with inhomogenous dielectrics, thin source contacts, and thick drain contacts yield the best sub-

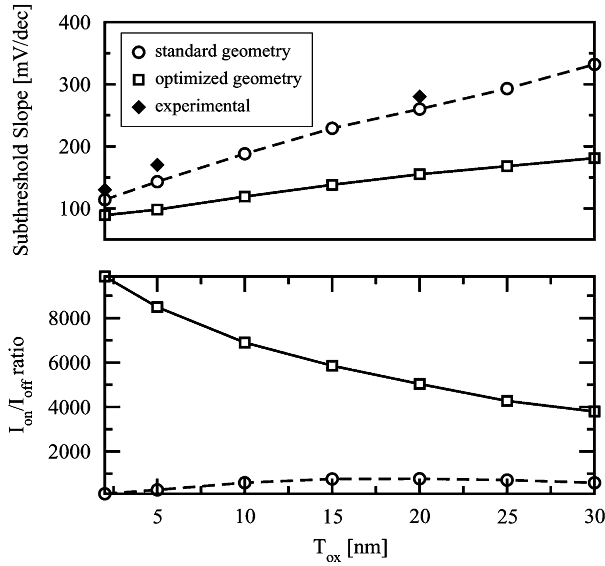

Fig. 7. Comparison of subthreshold slope and $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio for conventional (dashed lines) and optimized (solid lines) geometries. Experimental data for the subthreshold slope from [7] shows a similar scaling behavior.

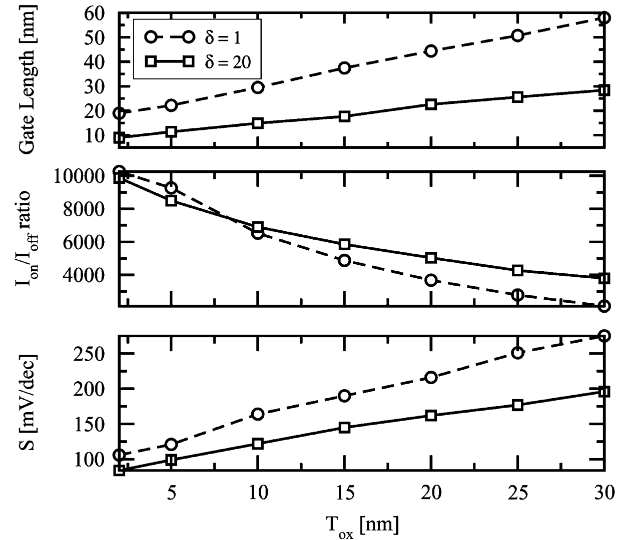

Fig. 8. Optimization results for a homogenous (dashed line with open circles) and a inhomogenous CNTFET (solid line with open squares). The gate length, $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, and subthreshold slope S are plotted.

threshold slope for the whole range of gate–oxide thicknesses (2–30 nm). However, the length of the gate contact, which results in the optimum subthreshold slope, depends on T_{ox}. It was found that the current through the CNT does not depend on L_{sg} as long as $L_{\mathrm{sg}} < 10$ nm, which results in a small overlap of gate and source contact. The gate length L_g for structures optimized with respect to a steep subthreshold slope continuously decreases when decreasing T_{ox}. This stems from the fact that, for geometries with small T_{ox}, the gate contact is more efficient in suppressing the potential barriers at the source (drain) contact. While geometries with a large T_{ox} need a larger gate contact in order to control the current over the potential barrier at the source contact, L_g can be reduced for geometries with small T_{ox}.

From Fig. 7, it can be seen that, for geometries optimized with respect to the subthreshold slope, the subthreshold slope scales approximately as T_{ox}. For comparison, in Fig. 7, the subthreshold slope of a symmetric CNTFET ($L_{\mathrm{dg}} = L_{\mathrm{sg}} = 5$ nm, $T_s = T_d = 10$ nm, $\epsilon_{\mathrm{top}} = \epsilon_{\mathrm{bot}} = 3.9$) is also given. In addition to the improved subthreshold slope for these geometries, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is increased when decreasing the gate–oxide thickness. This behavior is different from that of symmetric CNTFETs. For symmetric geometries, the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio is smaller, and for $T_{\mathrm{ox}} < 15$ nm, a reduction of $I_{\mathrm{on}}/I_{\mathrm{off}}$ takes place. The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of symmetric and optimized CNTFETs are plotted in the lower graph of Fig. 7.

When optimizing geometries with respect to the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, a different behavior occurs. At $T_{\mathrm{ox}} > 10$ nm, structures with inhomogenous dielectrics show a steeper subthreshold slope, as well as a higher $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, while at $T_{\mathrm{ox}} < 10$ nm, geometries with homogenous dielectrics have a larger $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio than geometries with inhomogenous dielectrics. This can be seen from Fig. 8, where the gate length $I_{\mathrm{on}}/I_{\mathrm{off}}$ and the subthreshold slope of optimized geometries with $\delta = 1$ ($\epsilon_{\mathrm{top}} = \epsilon_{\mathrm{bot}} = 3.9$) and $\delta = 20$ ($\epsilon_{\mathrm{top}} = 20, \epsilon_{\mathrm{bot}} = 1.0$) are plotted. Furthermore, it can be observed that the length of the gate contact, leading to the maximum $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, is larger when using homogenous dielectrics. This can be explained by the more efficient reduction of the potential barriers taking place in inhomogenous structures.

IV. Conclusion

The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of single-gate CNTFET structures can be significantly improved by using an asymmetric gate contact located near the source contact and thin source and wide drain contacts. Additionally, the subthreshold slope of such geometries can be improved by inhomogenous dielectrics above and below the tube, whereas the use of inhomogenous dielectrics in symmetric structures merely leads to high I_{off} currents. A subthreshold slope below 100 mV/dec was found for optimized geometries with $T_{\mathrm{ox}} < 5$ nm, which is significantly closer to the thermal limit of approximately 60 mV/dec at room temperature than previously reported values for conventional geometries [6]. Simulation results suggest that the subthreshold slope of single gate CNTFETs scales linearly with the gate–oxide thickness.

In contrast to symmetric devices, structures with asymmetric gate contacts show an increase of $I_{\mathrm{on}}/I_{\mathrm{off}}$ when scaling down the gate–oxide thickness, whereas $I_{\mathrm{on}}/I_{\mathrm{off}}$ decreases with increasing T_{ox} for symmetric devices when $T_{\mathrm{ox}} < 10$ nm.

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