MODELING OF ADVANCED SEMICONDUCTOR DEVICES

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ABSTRACT

Aggressive downscaling of modern semiconductor devices forces development engineers to question the validity of existing modeling approaches. Models for carrier transport have to be considered which are applicable on the transition into the quantum regime. An overview of semiclassical current transport models and their enhancements used for the simulation of nanoelectronic devices is given. Emphasis is put on arising modeling challenges in the existing and future technology nodes. Electron mobility analysis of ultra-scaled, strained field-effect transistors is presented in detail.

INTRODUCTION

The continuous increase in computational power and speed of integrated circuits in the past decades has been enabled by an aggressive size reduction of semiconductor devices. This trend is expected to continue in the coming decade as predicted and institutionalized by the International Technology Roadmap for Semiconductors (1). Today, when the 65 nm technology node with physical transistor gate lengths in the range of 35 nm is in mass production, the technological challenge is to introduce the 45 nm technology node already in a year. A new technology node is introduced every 3 years, with a long-term projection of the 22 nm node to be in mass production by the year 2016. The technological possibility to produce metal-on-insulator field effect transistors (MOSFETs) with gate lengths below 10 nm has already been demonstrated in research labs (2, 3). Also, from a theoretical point of view a device with only a few nm gate length has been predicted to be functional (4, 5).

Nevertheless, emerging severe technological challenges, related to different aspects of MOSFET fabrication and reliability in mass production as well as the rapidly increasing power dissipation, may slow down the so far exponential scaling of complementary MOSFETs (CMOS) technology. With the ongoing search for new technological solutions vital for CMOS downscaling, the development of conceptually new devices and architectures is becoming increasingly important. New nanoelectronic structures, such as carbon nanotubes, nanowires, and molecules, are considered to be the most prominent candidates for the post-CMOS era. Since conventional MOSFETs are already operating in the sub-100 nm range with gate lengths as small as 35 nm, new nanoelectronic devices are expected to complement and substitute some

of the current CMOS functions after being integrated into CMOS technology. While it is not yet clear at which point in time new structures like FinFETs, and processes with high-k dielectrics and metal gates will be competitive, one technology that is indispensable at the 45 nm node is strain engineering. While at the 90 nm node the saturation current I_{DSAT} was improved via process induced strain up to 10 % and 30 % for nMOS and pMOS, respectively, at the 65 nm node strain engineering yields an increase of I_{DSAT} by 53% and 32%, improving the overall chip speed by 40% relative to non-strained devices with the same feature size (6).

Technology computer-aided design (TCAD) tools are used to assist in development and engineering at practically all stages ranging from process simulation to device and circuit optimization. The main purpose of TCAD is the technology development-related cost reduction which currently amounts to 35% and is expected to rise to 40%, according to the ITRS (1). Due to the aggressive downscaling of CMOS device feature sizes and newly emerging nanoelectronic devices, various shortcomings of presently applied TCAD tools become significant. These tools are frequently based on semiclassical macroscopic transport models. From an engineering point of view, classical models such as the drift-diffusion model, have enjoyed an amazing success due to their relative simplicity, numerical robustness, and the ability to perform two- and three-dimensional simulations on large unstructured grids (7). Hot-carrier effects have motivated the development of higher-order transport models such as the hydrodynamic, the energy-transport and the six-moments models (8). However, inaccuracies originate from the quantum mechanical nature of carrier propagation in ultra-scaled devices (9).

An overview of currently developed semiclassical transport models is be presented in the following section. Semiclassical transport models are based on the Boltzmann equation which includes scattering integrals describing realistic microscopic processes. If augmented with quantum corrections, these models are still of great importance due to their relative computational simplicity, numerical stability, and an ability to provide reasonable quantitative results within seconds even for devices with gate length as short as 50 nm. In a separate section, the origin of the electron mobility enhancement originating from uniaxial stress is explained. It is shown that stress introduces anisotropy in the bulk electron mobility and that the mobility enhancement is determined by the stress and channel direction. Finally, the effect of stress on the inversion layer mobility is analyzed. It is shown how the mobility depends on wafer orientation and the thickness of the Si channel in ultra-thin body (UTB) MOSFETs.

SEMICLASSICAL TRANSPORT

After the ground-breaking work of Scharfetter and Gummel (10), who first proposed a robust discretization scheme for the drift-diffusion current relation, computer programs like MINIMOS (11) and PISCES (12) played a pioneering role in numerical simulation of the electrical characteristics of semiconductor devices. Since then, numerous transport models of increasing complexity have been introduced. The semiclassical transport description is based on the Boltzmann equation for the distribution

of carriers $f(\mathbf{r}, \mathbf{k}, t)$ in the phase space. The Boltzmann equation includes carrier scattering by phonons, impurities, interfaces, and other scattering sources through the corresponding collision integrals. Although the solution of the Boltzmann equation can be found numerically by means of Monte Carlo (MC) methods, TCAD models based on moments of the distribution function are highly desirable. Being computationally significantly more efficient than a MC algorithm, these higher-order moments methods provide a reasonable quantitative answer within seconds for devices as short as 50 nm. The fairly new six moments model (8) based on a non-Maxwellian distribution takes naturally into account the hot-carrier effects such as avalanche generation, hot carrier induced gate currents, or hot-carrier diffusion, which plays an important role in Silicon-On-Insulator (SOI) floating body MOSFETs. For the purpose of calibration the full-band MC method is often employed, as it can precisely account for the various scattering processes and band structure effects (13).

Another important development of transport models is related to the MC methods for solving the Boltzmann equation. After the pioneering work of Kurosawa in 1966 (14), who was the first to apply the MC method to simulate carrier transport in semiconductors, the significantly improved MC method was successfully applied to transport description in a variety of semiconductors (15). For electrons in silicon, the most thoroughly investigated case, it is believed that a satisfactory understanding of the band structure and of the basic scattering mechanisms has been achieved giving rise to a "standard model" (16). Nowadays, an accurate MC evaluation of carrier transport properties in inversion layers is of primary importance for predicting performance of modern CMOS bulk devices. Due to the strong confinement of carriers in the inversion layer of bulk MOSFETs or due to the geometric confinement in multigate FETs the carrier motion is quantized in one or two confinement directions giving rise to the formation of subbands. One possibility to address the effect of quantum confinement on the electron concentration is to use an effective potential. This can be achieved by a convolution of the electrostatic potential with a Gaussian function, which leads to a smoothing of the original potential (17), (18), (19).

Another method is based on the calculation of a quantum corrected potential by solving self-consistently the Schrödinger-Poisson equation system (20), (21). The quantum corrected potential suppresses the carrier concentration close to the interface, mimicking the real quantum-mechanical behavior. These approaches combine advantages of full-band description and flexibility of scattering processes of three-dimensional classical MC simulations with the generality of material composition and transport peculiarities due to quantum confinement and can also address the effects of strain.

The MC approach may incorporate the quantized carrier motion in the direction orthogonal to the current. The quantum-mechanical motion of carriers in the confined direction is addressed by the self-consistent solution of the corresponding Schrödinger and Poisson equation, leading to the formation of subbands. The carrier motion within each subband may still be considered semiclassical and therefore can be well described by the corresponding Boltzmann equation written for the subband distribution function $f_n(\mathbf{r}, \mathbf{k}, t)$. Because of possible carrier transitions between different subbands due to scattering, the collision integrals on the right-hand-side of

the Boltzmann equation have to include the terms responsible for the intersubband scattering processes. The transport in the inversion layer of a MOSFET is finally described by a set of Boltzmann equations for every subband, coupled by the intersubband scattering integrals. The set of the subband Boltzmann equations for $f_n(\mathbf{r}, \mathbf{k}, t)$ is conveniently solved by a MC method. This approach therefore combines the advantages of a quantum description in confinement direction with a semiclassical description in transport direction and represents a transition between semiclassical and quantum-mechanical pictures. Various simulations of the low-field surface mobility in inversion layers of Si will be given in the following, when the effect of uniaxial stress on the inversion layer mobility is investigated. In order to reproduce the experimental "universal mobility" curve in Fig. 3, depending on the stress level, doping, and the inversion layer concentration, up to 100 subbands forming at a (100) silicon interface were taken into account, with realistic electron-phonon and surface roughness scattering included (22).

STRESS/STRAIN EFFECTS ON ELECTRON MOBILITY

Uniaxially stressed Si is used in leading edge logic technologies, because it can increase mobility and current drive of both n-channel and p-channel MOSFETs. While mobility in biaxially strained inversion layers has often been subject to theoretical investigations, the technologically more relevant application, with process-induced uniaxial stress along the channel direction, has surprisingly been neglected until recently (23).

Phenomenologically the effect of strain on the mobility can be modeled using the bulk linear piezo coefficients to quantify strained Si mobility enhancement (24). The piezo coefficients can certainly be used as a guide how strain maximizes the mobility enhancement, however, they are valid only for small levels of strain and have to be adapted to predict the mobility enhancement in inversion layers.

We have followed a more rigorous physics-based model, based on solving the Boltzmann equation by means of the Monte Carlo method to analyze strain effects. First, the effect of strain on the bulk electron band structure and the bulk mobility is discussed. We continue our analysis by addressing the combined effect of quantum confinement and stress on the electron inversion layer mobility. Finally, simulation results for electron mobility in silicon-on-insulator (SOI) transistors with ultra-thin-Si body (UTB) are presented.

Effect of Strain on Bulk Electron Mobility

Strain alters the energy band structure of Si, and consequently, the electrical properties become anisotropic. According to deformation potential theory (25) strain lifts the degeneracy of the Δ_6 conduction bands. The strain induced valley shifts affect the mobility in two respects: (i) Mobility is enhanced, because scattering between the X-valleys of the conduction band is reduced, and (ii), the X-valleys are no longer

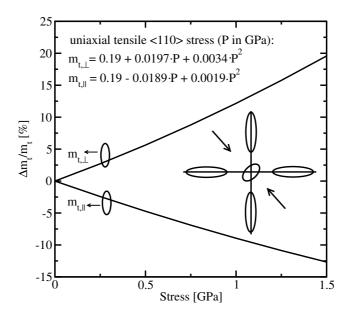


Fig. 1: Effective mass change for electrons in Δ_2 valley parallel and perpendicular to stress direction as a function of tensile uniaxial stress along [110].

equally populated, giving rise to an anisotropic mobility, either increasing or reducing the enhancement from (i).

Our Monte Carlo simulator (26) allows the simulation of arbitrarily strained Si and SiGe. It was demonstrated that the mobility enhancement occurring in strained $Si_{1-x}Ge_x$ layers on $Si_{1-y}Ge_y$ substrates for arbitrary substrate orientations can be accurately reproduced (27). Recent extensions consider strain effects arising from uniaxial stress. Experiments (28, 29) have shown that the mobility enhancement $\Delta \mu_n$ cannot solely be attributed to the strain-induced valley splitting, and a recent study has shown that a stress along the $\langle 110 \rangle$ direction leads to a significant change of the electron effective masses Δm^* (23). This result is surprising, because within the framework of deformation potential theory the strain induced electron mass change Δm^* is usually neglected. Thus, in modeling applications it was widely accepted so far that stress/strain merely lifts the degeneracy of the Δ_6 conduction bands, but has no significant impact on the electron effective masses.

We performed calculations of the band structure of Si for general strain conditions by means of the nonlocal empirical pseudopotential method including spin-orbit coupling. This method was developed by Chelinkowsky and Cohen (30) for unstrained Si and is frequently used to calculate the full band structure of semiconductors since it is efficient, and requires only a limited set of fitting parameters (31–33). Our calculations confirm the experimental findings that in the particular case of uniaxially [110] stressed Si the effective mass change cannot be neglected for transport modeling (see Fig. 1).

Fig. 2 shows the effect of in-plane stress on a standard (001) wafer on the in-plane electron mobility. Uniaxial stress is applied along [110] and [100]. Both conditions split the Δ_6 conduction bands in a two-fold set Δ_2 and a four-fold set Δ_4 . If stress

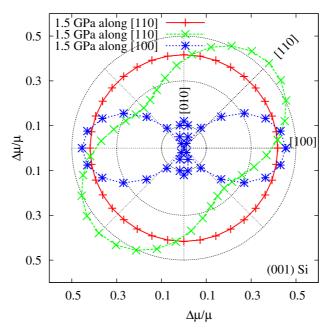


Fig. 2: Mobility enhancement for uniaxial [110] tensile stress with (\times) and without (+) effective mass correction. Symbols (*) show the anisotropic mobility enhancement for the same amount of stress along [100].

is applied along [110] the valley orientated along [001] moves down in energy, having m_t in the plane of transport. Thus, in-plane mobility is isotropically enhanced. If stress is applied along [100] the valleys orientated along [001] and [010] move down in energy. These valleys have the transport mass m_t in the stress direction, but in the in-plane direction perpendicular to the stress [010], the [010] valley has a mass of m_l , thus the mobility is lowered in this direction. Fig. 2 demonstrates that only by the inclusion of the effective mass change induced by [110] stress the experimentally observed anisotropic mobility enhancement is reproduced by simulation.

Effect of Strain and Substrate Orientation on Electron Inversion Layer Mobility

We will continue our analysis by investigating the origin of the electron inversion layer mobility enhancement with uniaxial stress. To demonstrate the influence on the substrate orientation, simulations are performed for (001) and (110) oriented wafers. It is shown that uniaxial stress leads to a pronounced anisotropy of the inplane mobility for both substrate orientations. While on (110) substrates this effect stems from the ellipsoidal shape of the lowest subband ladder, an effective mass change induced by [110] stress has to be taken into account to explain the anisotropic mobility of [110] uniaxially stressed (001) wafers.

While the bulk mobility enhancement for general stress conditions can be determined from the piezo coefficients for small stress levels and from MC simulations for larger stress levels, in inversion layers the effective mobility is mainly determined by quantum confinement, thus one cannot use the bulk piezo coefficients or bulk MC simulations to determine the stress induced effective mobility enhancement $\Delta \mu_{\text{eff}}$.

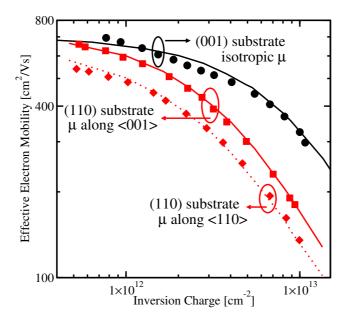


Fig. 3: Simulated effective electron mobility (lines) for substrate orientation (001) and (110) compared to measurements (34, 35) (symbols). The anisotropic mobility on (110) is given along [001] and [110].

Depending on the substrate orientation the six-fold degenerate X-valley splits into up to three different subband ladders. While on (001) substrates the subbands of the lowest subband ladder (unprimed ladder) are spherical and the ladder is two-fold degenerate, on (110) substrates the subbands are elliptical and the unprimed ladder is four-fold degenerate. The higher density of states and larger transport masses on (110) substrates thus yield a lower inversion layer mobility as compared to (001). This can be seen in Fig. 3, where we compare experimental data (34,35) to our simulation results. The inversion layer mobility was calculated by means of a subband Monte Carlo method (22) taking into account phonon scattering, surface roughness scattering according to Ando's model, and screening effects.

It is well known that the hole inversion layer mobility is higher on (110) oriented wafers than on standard wafers with (001) orientation, whereas the electron mobility is smaller for this surface orientation (see Fig. 3). To enhance the electron mobility on (110) substrates a uniaxial tensile stress along [001] can be applied, as this stress condition increases the splitting between the primed and unprimed ladder. From EPM simulations for this stress condition we observe only a negligible change of the effective masses which determine the transport in the subband layers, so this effect can be neglected. In Fig. 4 we see that stress increases $\mu_{\rm eff}$ parallel to the stress, whereas the mobility perpendicular to the stress is smaller as compared to the unstressed case. Since no effective mass change occurs, the mobility change is expected to saturate at larger stress (~ 1 GPa), as soon as the primed ladder becomes depopulated. The resulting mobility can be understood from a stress induced repopulation between unprimed and primed subband ladders which are both elliptic. This result is in good agreement with experimental data (28).

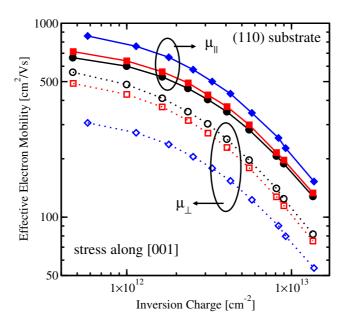


Fig. 4: Simulated effective electron mobility parallel (solid lines/closed symbols) and perpendicular (dotted lines/open symbols) to stress direction [001] without stress (circles), 0.1 GPa (squares), and 1.0 GPa stress (diamonds).

Electron Inversion Layer Mobility in Stressed UTB SOI MOSFETs

Finally, the effect of stress on the effective electron mobility enhancement in UTB MOSFETs is analyzed. On (001) substrates it was shown before that, if stress is applied in the channel direction [110], one can benefit from two effects: stress induced valley splitting and the effective mass change. For $T_{\rm SOI}$ =20 nm, $\Delta\mu_{\rm eff}$ can be understood from a combination of the two effects yielding an anisotropic $\Delta\mu_{\rm eff}$ as compared to the unstressed system (see Fig. 5). At $T_{\rm SOI}$ =2.4 nm the strong quantum confinement induces an intrinsic valley splitting, thus the stress induced valley shifts have no further effect on the mobility. The larger $\mu_{\rm eff||}$ and smaller $\mu_{\rm eff||}$ parallel/perpendicular to the stress direction (compare Fig. 5) is a result from the effective mass change only and found in good agreement with experimental data (23). In contrast to (100) substrates, when reducing $T_{\rm SOI}$ on (110) substrates, the stress induced $\Delta\mu_{\rm eff}$ decreases, because no effective mass change occurs.

SUMMARY AND CONCLUSIONS

As downscaling continues, quantum effects steadily become more prominent in advanced semiconductor devices. Simultaneously, well established TCAD tools based on semiclassical models lose their ability to accurately predict the main characteristics. To demonstrate the need for model refinements a state-of-the-art simulation example was presented, showing how Monte Carlo simulations, if augmented by the relevant quantum corrections, can successfully predict mobilities in ultra-scaled stress

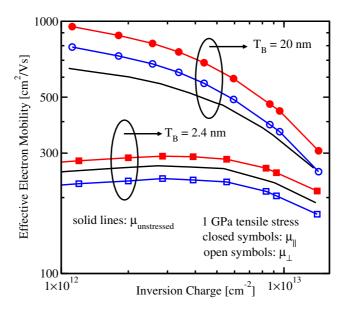


Fig. 5: Simulated μ_{eff} for substrate orientation (001) for two body thicknesses. Stress and channel along [110].

field-effect transistors. However, it should be kept in mind, that often from a point of view of a device engineer, timely results are more valuable than accurate analyses (36). Thus, the mobilities extracted from Monte Carlo simulations may be cast in TCAD models based on moments of the distribution function, providing reasonable qualitative answers for devices within seconds.

REFERENCES

- 1. International Technology Roadmap for Semiconductors 2005 Edition, http://www.itrs.net/Common/2005ITRS/Home2005.htm (2005).
- 2. B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Documaci, Z. Ren, F.-F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P. Wong, W. Haensch, *IEDM Techn. Dig.*, 267 (2002).
- 3. H. Iwai, Solid-State Electron., 48 (4), 497 (2004).
- 4. V. A. Sverdlov, T. J. Walls, K. K. Likharev, *IEEE Trans. Electron Devices*, **50** (9), 1926 (2003).
- 5. L. Risch, Proc. European Solid-State Device Research Conf., 63 (2005).
- 6. M. Horstmann, A. Wei, T. Kammler, IEDM Techn. Dig., 61 (2005).
- 7. S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer, (1984).
- 8. T. Grasser, T.-W. Tang, H. Kosina, S. Selberherr, *Proc. IEEE*, **91** (2), 251 (2003).
- 9. F. O. Heinz, F. M. Bufler, A. Schenk, W. Fichtner, Symposium on Nano Device Technology, Hsinchu, Taiwan, 2 (2004).
- 10. D. L. Scharfetter, H. K. Gummel, *IEEE Trans. Electron Devices*, **16** (1), 64 (1969).

- 11. S. Selberherr, W. Fichtner, H. Pötzl, in *Numerical Analysis of Semiconductor Devices and Integrated Circuits, Vol. I*, Boole Press, Dublin, 275 (1979).
- 12. M. R. Pinto, PISCES IIB, Stanford University, (1985).
- 13. M. V. Fischetti, S. E. Laux, *Physical Review B*, **38** (14), 9721 (1988).
- 14. T. Kurosawa, in *Proc. Intl. Conf. on Physics of Semiconductors*, 424 (1966).
- 15. C. Jacoboni, L. Reggiani, Reviews of Modern Physics, 55 (3), 645 (1983).
- 16. M. Fischetti, A. Laux, in 26th European Solid State Device Research Conference, 813 (1996).
- 17. Y. Li, T.-W. Tang, X. Wang, *IEEE Trans. Nanotechnology*, 1 (4), 238 (2002).
- 18. K. Z. Ahmed, P. A. Kraus, C. Olsen, F. Nouri, *IEEE Trans. Electron Devices*, **50** (12), 2564 (2003).
- 19. D. E. P. Palestri, S. Eminente, C. Fiegna, E. Sangiorgi, L. Selmi, *Solid-State Electron.*, 49, 727 (2005).
- 20. G. A. Kathawala, B. Winstead, U. Ravaioli, *IEEE Trans. Electron Devices*, **50** (12) 2467 (2003).
- 21. X.-F. Fan, X. Wang, B. Winstead, L. F. Register, U. Ravaioli, S. K. Banerjee, *IEEE Trans. Electron Devices*, **51** (6), 962 (2004).
- 22. E. Ungersboeck, H. Kosina, in *Proc. Intl. Conf. on Simulation of Semiconductor Processes and Devices*, Tokyo, 311 (2005).
- 23. K. Uchida, T. Krishnamohan, K.C. Saraswat, Y. Nishis, *IEDM Techn. Dig.*, 135 (2005).
- 24. S.-E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, *IEEE Electron Dev. Lett.*, **51** (11), 1790 (2004).
- 25. C. Herring, E. Vogt, *Physical Review*, **101** (3), 944 (1956).
- 26. I μ E, VMC 2.0 User's Guide, Institute for Microelectronics, Technische Universität Wien, Austria, (2006).
- 27. S. Smirnov, H. Kosina, *Solid-State Electron.*, **48**, 1325 (2004).
- 28. H. Irie, K. Kita, K. Kyuno, A. Toriumi, *IEDM Techn. Dig.*, 225 (2004).
- 29. K. Uchida, R. Zednik, C.-H. Lu, H. Jagannathan, J. McVittie, P.C. McIntyre, Y. Nishi, *IEDM Techn. Dig.*, 229 (2004).
- 30. J.R. Chelikowsky, D.J. Chadi, M.L. Cohen, *Physical Review B*, 8, 2786 (1973).
- 31. M. Rieger, P. Vogl, *Physical Review B*, **48**, 14276 (1993).
- 32. M. Fischetti, S.E. Laux, J. Appl. Phys., 80 (4), 2234 (1996).
- 33. C. Jungemann, B. Meinerzhagen, *Hierarchical Device Simulation. The Monte Carlo Perspective*, Springer, (2003).
- 34. K. Uchida, J. Koga, S. Takagi, *IEDM Techn. Dig.*, 805 (2003).
- 35. G. Tsutsui, M. Saitoh, T. Saraya, T. Nagumo, T. Hiramoto, *IEDM Techn. Dig.*, 747 (2005).
- 36. M. Duane, *IEICE Trans. Electron.*, **E82**-C (6), 976 (1999).