Planarization of Passivation Layers during Manufacturing Processes of Image Sensors

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Abstract— **Image sensor processes are sensitive to passivation planarization which prevents clear layer coating issues and shortens the optical path between color filter and active surface. We present analysis of the deposition of passivation layers into trenches of image sensors. The simulation results are obtained by using the topography simulator ELSA (Enhanced Level Set Applications). We predict a range of trench width, stack height, and the thickness of the deposited layers leading to a sufficient planarization margin.**

I. Introduction

An image sensor device is constructed as follows [1]; after the formation of a photodiode on silicon substrate via implantation, ILD (Inter-Layer Dielectrics) layers such as PMD (Pre-Metal Dielectrics), IMD (Inter-Metal Dielectrics), and passivation layers, CFA (Color Filter Array), and OCM (Over Coating Material) are deposited subsequently followed by the formation of a microlens at the end. Among these processes the passivation or better to say a planarized passivation plays an important role.

Passivation planarization improves our image sensor products by reduction of the thickness of clear polymer planarization used prior to the color filter module that results in optical response benefits from stack height reduction. Furthermore, it enhances our image sensor products by reducing within-chip color variation caused when clear resist is coated over large step heights, resulting in streaking.

A typical passivation stack in IC chips is a layer of SiO_2 from PECVD (Plasma Enhanced Chemical Vapor Deposition) TEOS (Tetraethoxysilane) covered by a layer of PECVD Si_3N_4. Our objective is to achieve planarized passivation in the presence of deep trenches that serve as moisture barrier or topmost metal topography. Planarization of a moisture seal Si_3N_4 layer can be achieved by optimizing the trench width and taking advantage of the PECVD breadloafing characteristic. Planarization of a TEOS process on top metal topography can be achieved by depositing a thick layer of silicon dioxide from TEOS, which then is planarized by CMP (Chemical Mechanical Planarization) down to an optimized thickness. Such an optimization requires a topography simulator for predicting profiles of these deposition processes.

The topography simulator ELSA [2] is based on a level set method [3] for tracking moving boundaries in two and three dimensions. ELSA has been proven for different semiconductor manufacturing processes, e.g., the deposition of silicon dioxide into trenches for power MOSFET applications [4], the calculation of the capacitances contributing into RC timing delays in interconnect lines [2], and finally, the prediction of three-dimensional void characteristics as a function of geometrical layout to avoid cracking effects [5].

II. The Goals of Investigations

The goals of the simulations are: First, optimizing the trench width such that after Si_3N_4 deposition and breadloafing, the trench top closes completely, while sufficient bottom and sidewall coverage is obtained. Second, assuming $1\mu\text{m}$ silicon dioxide is deposited from TEOS and polished down to $0.3\mu\text{m}$, optimizing the trench width and height such that a sufficient planarization margin larger than the CMP process variation is obtained. As shown in Fig. 1 the planarization margin is defined as the distance between the top of the void or the bottom of the oxide dimple (when no void forms) to $0.3\mu\text{m}$ above the metal.

The geometrical parameters considered for investigations are divided into two different sets. The first set consists of 45 cases for the deposition of silicon nitride with the following geometrical parameters D, H, and T (cf. Fig. 2) that stand for trench width, trench height, and the thickness of the deposited layer, respectively:

- D = 0.5, 1.0, 2.0, 3.0, and $4.0\mu\text{m}$
- H = 2.0, 3.0, and $4.0\mu\text{m}$
- T = 0.3, 0.6, and $0.9\mu\text{m}$

The second set consists of 63 cases for the deposition of silicon dioxide from TEOS with the following parameters:

- D = 0.3, 0.5, 0.8, 1.0, 1.4, 2.0, and $3.0\mu\text{m}$
- H = 0.3, 0.5, and $0.9\mu\text{m}$
- T = 0.3, 0.7, and $1\mu\text{m}$

A. Results of Silicon Nitride Deposition

Table I represents a part of the simulation results, namely, those of the deposition of silicon nitride into the trenches with $D = 0.5\mu\text{m}$ and $D = 1\mu\text{m}$. The results of $D = 1\mu\text{m}$ are graphically shown in Fig. 3. The results given in Table I can be summarized as follows:

- A planar passivation with complete nitride sealed die edge is possible, which requires a $1\mu\text{m}$ or lower trench width.

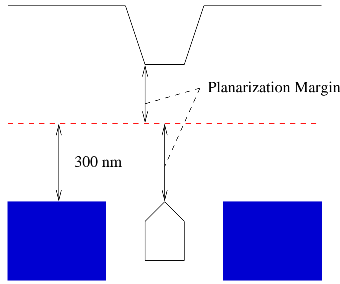

Fig. 1. An illustrative description of planarization margin.

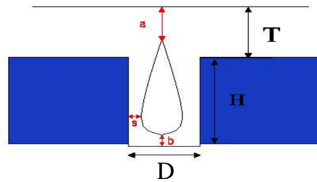

Fig. 2. A schematic of a trench and its geometrical parameters. D, H, and T stand for trench width, metal thickness, and the thickness of the deposited layer. The parameters a, b, and s are used for the difference between the top of the void and the thickness of the deposited layer, bottom coverage, and sidewall coverage, respectively.

TABLE I

TABULATED RESULTS FOR $0.5\mu m$ AND $1\mu m$ WIDE TRENCHES.

T(μm)	H(μm)	D(μm)	a(μm)	s(μm)	b(μm)
0.9	4	1	0.43	0.29	0.17
0.6	4	1	NA	0.29	0.17
0.3	4	1	NA	0.14	0.09
0.9	3	1	0.49	0.31	0.17
0.6	3	1	NA	0.31	0.17
0.3	3	1	NA	0.14	0.09
0.9	2	1	0.4	0.34	0.26
0.6	2	1	NA	0.34	0.26
0.3	2	1	NA	0.14	0.09
0.9	4	0.5	0.9	0.1665	0.06
0.6	4	0.5	0.57	0.1665	0.06
0.3	4	0.5	0.17	0.1665	0.06
0.9	3	0.5	0.9	0.1665	0.06
0.6	3	0.5	0.57	0.1665	0.06
0.3	3	0.5	NA	0.1665	0.06
0.9	2	0.5	0.9	0.18	0.11
0.6	2	0.5	0.57	0.18	0.11
0.3	2	0.5	NA	0.18	0.11

- When the trench width is reduced to $0.5\mu m$, the topside nitride thickness can be reduced to $0.6\mu m$. However, this could raise reliability issues.

B. Results of Silicon Dioxide Deposition

Based on our results for the cases listed in Section II, the planarization margins for different trench widths and heights have been calculated as shown in Fig. 4. The results can be summarized as follows:

- By polishing down from $1\mu m$ to $0.3\mu m$ TEOS:
  - $0.3\mu m$ trench height provides sufficient planarization margin regardless of trench width (cf. Fig. 4).
  - $0.5\mu m$ and $0.9\mu m$ trench heights lead to a non-planar surface either by opening up voids or by incomplete removal of the dimple at spaces $> 1\mu m$ (cf. Fig. 4).

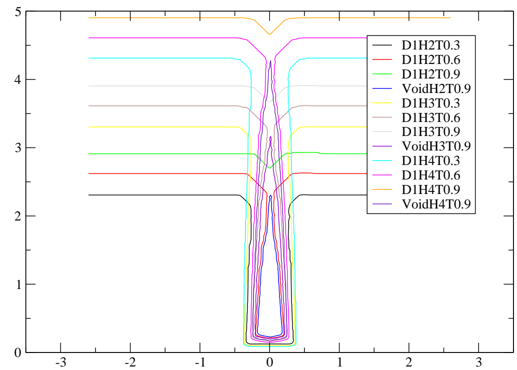

Fig. 3. The deposition of silicon nitride into trenches of D = $1\mu m$.

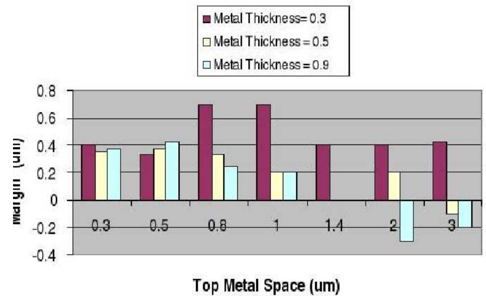

Fig. 4. Planarization margin calculated for different widths and thicknesses.

III. CONCLUSION

Based on the results obtained by using a state of the art topography simulator, the features causing non-planar passivation were optimized. The optimization leads to optical response benefits due to stack height reduction. Furthermore, within-chip color variation is reduced.

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