Numerical Analysis of Gate Stacks

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Numerous technological innovations, including material and process changes such as high–k gate dielectrics and metal gate electrodes, are investigated to meet the upcoming scaling requirements while keeping the gate leakage current within tolerable limits [1]. To overcome the technological problems, further theoretical and experimental research is needed which requires an extensive use of computer simulation. We present a software tool, the Vienna Schrödinger Poisson solver (VSP), for numerical analysis of novel gate stacks with emphasis on reliability.

For investigations of the electrostatics of MOS inversion layers, our closed boundary Schrödinger Poisson solver VSP [2] includes models for interface traps and bulk traps in arbitrarily stacked gate dielectrics. The band structure for electrons and holes is specified by an arbitrary number of valley sorts, defined by an anisotropic effective mass and a band edge energy. The effects of substrate orientation and strain on the band structure are taken into account too.

The leakage current calculations are performed in a post processing step, since they have a negligible influence on the electrostatic potential. The direct tunneling current components from both continuum J_{3D} and quasi bound states (QBS) J_{2D} are taken into account according to [3]. Trap assisted tunneling (TAT), which is a major issue regarding reliability in novel gate stacks [4], is considered in terms of an inelastic single step tunneling process [5]. The current density is the sum $J_{\mathrm{tat}} = \mathrm{q}\sum_i R_i \Delta x_i$ where R_i denotes the capture and emission rates of each trap and Δx_i is the trap cross section. The model has been calibrated to measurements.

The software is written in C++ using state-of-the-art software design techniques. VSP offers a graphical user interface written in Java, as well as a XML based interface. Furthermore, VSP has an open software application interface (API) for the use in third party simulation environments. These features are mandatory for tasks like parameter identification and model calibration, for example for CV-curves and gate stack optimizations. Binaries are available for Linux, Windows, IBM AIX, and MacOs on request. Some typical applications are described in the captions of Fig. 1, Fig. 2, and Fig. 3 respectively.

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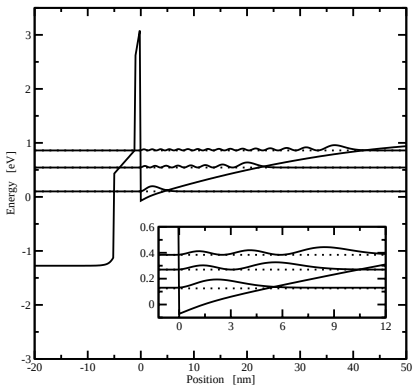

Figure 1: The wavefunctions and the energy levels of some QBS in the inversion layer of an nMOS device with a stacked gate dielectric.

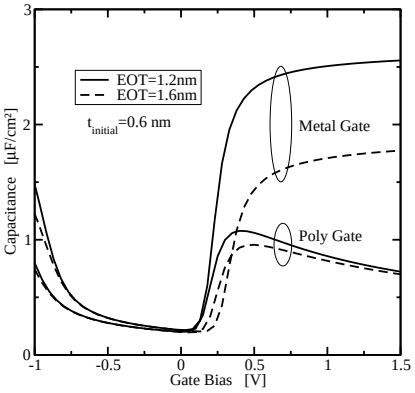

Figure 2: The CV-characteristic of SiO_2-HfO_2 stacked gate dielectric for different EOTs. Metal gates are suitable for scaling the EOT down to the sub 1.0 nm range.

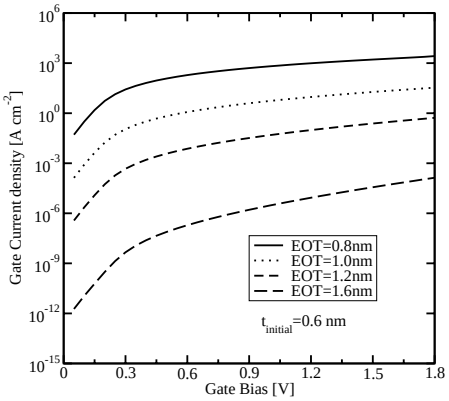

Figure 3: The leakage current density of a SiO_2 HfO_2 stacked gate dielectric.

[1] International Technology Roadmap for Semiconductors - 2005 Edition, 2005, http://public.itrs.net.

[2] M. Karner *et al.*, in *International Workshop on Computational Electronics* (Vienna, 2006).

[3] A. Gehring and S. Selberherr, in *Proc. Intl. Conf. on Simulation of Semiconductor Processes and Devices* (München, 2004), pp. 25–28.

[4] M. Houssa *et al.*, J.Appl.Phys. **87**, 8615 (2000).

[5] F. Jiménez-Molinos *et al.*, J.Appl.Phys. **90**, 3396 (2001).