Optimal Design for Carbon Nanotube Transistors

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***Abstract*— A numerical study of carbon nanotube field effect transistors is presented. To investigate transport phenomena in such devices the non-equilibrium Green's function formalism was employed. Phenomena like tunneling and electron-phonon interactions are rigorously taken into account. The effect of geometrical parameters on the device performance was studied. Our results clearly show that device characteristics can be optimized by appropriately selecting geometrical parameters.**

I. Introduction

A carbon nanotube (CNT) can be viewed as a rolled-up sheet of graphite with a diameter of a few nano-meters. Depending on the chiral angle the CNT can be either metallic or semiconducting. Semiconducting CNTs can be used as channels for field-effect transistors (FETs). CNTFETs have been studied in recent years as potential alternatives to CMOS devices because of their capability of ballistic transport.

Depending on the work function difference between the metal contact and the CNT, carriers at the metal-CNT interface encounter different barrier heights. Devices with positive [1] and zero [2] barrier heights were fabricated. The barrier height is defined as the potential barrier which is seen by carriers at the Fermi level in the metal. Therefore, in a device with zero barrier height, carriers with energies above the Fermi level of the metal reach the channel by thermionic emission and carriers with energies below the Fermi level have to tunnel to reach the channel. Devices with positive barrier heights have lower on-current and also suffer from ambipolar behavior [3, 4], while devices with zero barrier height theoretically [5] and experimentally [6] show better performance. In this work we focus on devices with zero barrier height for electrons. The barrier height for holes is given by the band gap of the CNT. Since the dispersion relations for electrons and holes are the same, our discussions are valid for holes as well.

Using the non-equilibrium Green's function (NEGF) formalism quantum phenomena like tunneling, and scattering processes can be rigorously modeled. Here we extended our previous work [7] by including the effect of electron-phonon interaction in the calculations, considering large signal dynamic response, and investigating the influence of geometrical parameters. In the next section our methodology is described. Then the effect of different geometrical parameters on the device characteristics is analyzed, and methods for performance optimization are suggested.

II. Approach

In this section the models used to study the static and dynamic response of CNTFETs are explained.

A. Static Response

Based on the NEGF formalism we investigated the effect of device geometry on the performance of carbon nanotube field-effect transistors. We have solved the coupled system of transport and Poisson equations numerically. Due to quantum confinement along the tube circumference, carrier have bound wave functions around the CNT and can propagate along the tube axis. Under the assumption that the potential profile does not vary around the circumference of the CNT, sub-bands will be decoupled. In this work we assume bias conditions for which the first sub-band contributes mostly to the total current. In the mode-space approach [8] the transport equation for each sub-band can be written as:

$$G^{\mathrm{R,A}}_{\mathbf{r},\mathbf{r}'}(E) = [EI - H_{\mathbf{r},\mathbf{r}'}(E) - \Sigma^{\mathrm{R,A}}_{\mathbf{r},\mathbf{r}'}(E)]^{-1} \tag{1}$$

$$G^{<,>}_{\mathbf{r},\mathbf{r}'}(E) = G^{\mathrm{R}}_{\mathbf{r},\mathbf{r}'}(E)\Sigma^{<,>}_{\mathbf{r},\mathbf{r}'}(E)G^{\mathrm{A}}_{\mathbf{r},\mathbf{r}'}(E) \tag{2}$$

In (1) an effective mass Hamiltonian was assumed. All our calculations assume a CNT with a band gap of $\mathrm{E_g} = 0.6$ eV corresponding to a CNT with a diameter of $\mathrm{d_{CNT}} = 1.6$ nm, and $m^* = 0.05m_0$ for both electrons and holes. A recursive Green's function method is used for solving (1) and (2) [9]. The total self-energy in (1) consists of the self-energies due to the source contact, drain contact, and electron-phonon interaction, $\Sigma^R = \Sigma^R_{\mathrm{S}} + \Sigma^R_{\mathrm{D}} + \Sigma^R_{\mathrm{el-ph}}$. The self-energy due to electron-phonon interaction consists of the contribution of elastic and inelastic scattering mechanisms, $\Sigma^{<,>}_{\mathrm{e-ph}} = \Sigma^{<,>}_{\mathrm{el}} + \Sigma^{<,>}_{\mathrm{inel}}$. Assuming a single sub-band the electron-phonon self-energies are simplified to (3)-(6).

$$\Sigma^{<,>}_{\mathrm{el},(\mathbf{r},\mathbf{r})}(E) = D_{\mathrm{el}} G^{<,>}_{\mathbf{r},\mathbf{r}}(E) \tag{3}$$

$$\begin{aligned}\Sigma^{<}_{\mathrm{inel},(\mathbf{r},\mathbf{r})}(E) = &\sum_{\nu} D^{\nu}_{\mathrm{inel}} \\ &[(n_B(\hbar\omega_\nu)+1)G^{<}_{\mathbf{r},\mathbf{r}}(E+\hbar\omega_\nu) \\ &+ n_B(\hbar\omega_\nu)G^{<}_{\mathbf{r},\mathbf{r}}(E-\hbar\omega_\nu)]\end{aligned} \tag{4}$$

$$\begin{aligned}\Sigma^{>}_{\mathrm{inel},(\mathbf{r},\mathbf{r})}(E) = &\sum_{\nu} D^{\nu}_{\mathrm{inel}} \\ &[(n_B(\hbar\omega_\nu)+1)G^{>}_{\mathbf{r},\mathbf{r}}(E-\hbar\omega_\nu) \\ &+ n_B(\hbar\omega_\nu)G^{>}_{\mathbf{r},\mathbf{r}}(E+\hbar\omega_\nu)]\end{aligned} \tag{5}$$

$$\Im m[\Sigma^{\mathrm{R}}(E)] = \frac{1}{2i}[\Sigma^{>} - \Sigma^{<}] \tag{6}$$

where n_B is given by the Bose-Einstein distribution function. In general electron-phonon interaction parameters ($D_{\mathrm{el,inel}}$) depends on the diameter and the chirality of the CNT. The

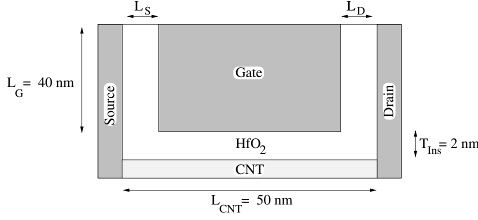

Fig. 1. The device structure. The device is 250 nm extended into the third dimension. $\epsilon_r = 15$.

calculation of these parameters is presented in [10]. The imaginary and real parts of the self-energy broadens and shifts the density of states, respectively. We neglected the real part of the self-energy.

The transport equations (1) to (6) are iterated to achieve convergence of the electron-phonon self-energies, resulting in a self-consistent Born approximation. Then the coupled system of transport and Poisson equation is solved iteratively. The carrier concentration and the current density at some point $\mathbf{r}$ of the device can be calculated as (7) and (8).

$$n_{\mathbf{r}} = -4i \int G^{<}_{\mathbf{r},\mathbf{r}}(E) \frac{dE}{2\pi} \tag{7}$$

$$j_{\mathbf{r}} = \frac{4q}{\hbar} \int \mathrm{Tr}[\Sigma^{<}_{\mathbf{r},\mathbf{r}} G^{>}_{\mathbf{r},\mathbf{r}}(E) - \Sigma^{>}_{\mathbf{r},\mathbf{r}} G^{<}_{\mathbf{r},\mathbf{r}}(E)] \frac{dE}{2\pi} \tag{8}$$

In CNTs elastic scattering is caused by acoustic phonons and inelastic scattering occurs due to zone boundary (ZB), optical (OP), and radial breathing (RBM) phonon modes. In CNTs with diameters in the range $d_{\mathrm{CNT}} = 1-2$ nm, the energies of the these phonon modes are $\hbar\omega_{\mathrm{ZB}} \approx 160$ and 180 meV, $\hbar\omega_{\mathrm{OP}} \approx 200$ meV, and $\hbar\omega_{\mathrm{RBM}} \approx 30$ meV respectively [11, 12]. Due to small occupation number of high energy phonons, such as OP and ZB phonon modes, they do not degrade the performance considerably, whereas the RBM phonon mode can have a detrimental effect. However, due to weak electron-phonon coupling the RBM mode has a negligible effect at room temperature. The electron-phonon coupling is also weak for acoustic phonon

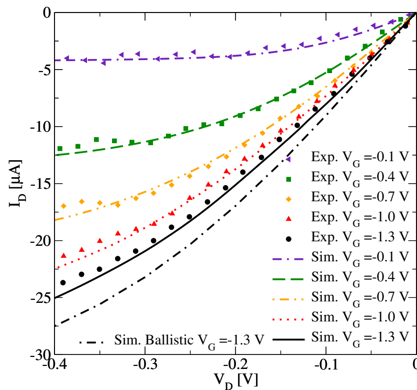

Fig. 2. Comparison of the simulation results and experimental data [6] for the output characteristics. The results for the bias point $V_G = -1.3$ V are compared with the ballistic limit.

(AP) modes. Therefore, short CNTFETs can operate close to the ballistic limit. Fig. 2 shows excellent agreement between simulation results and experimental data [6]. The result for the bias point $V_{\mathrm{G}} = -1.3$ V is compared with the ballistic limit, which confirms the validity of nearly ballistic transport in short CNTFETs.

B. Dynamic Response

To investigate the dynamic response of the device we consider the device delay time defined as:

$$\tau = \frac{C_{\mathrm{G}} V_{\mathrm{DD}}}{I_{\mathrm{on}}} \tag{9}$$

Here, $C_{\mathrm{G}} = C_{\mathrm{GS}} + C_{\mathrm{GD}} + C_{\mathrm{GG}}$ with ${C_{\mathrm{GG}}}^{-1} = {C_{\mathrm{Ins}}}^{-1} + {C_{\mathrm{Q}}}^{-1}$. The quantum capacitance is given by $C_{\mathrm{Q}} = 8\mathrm{q}^2/\mathrm{h}\nu_{\mathrm{F}} \approx 400\mathrm{aF}/\mu\mathrm{m}$, including the twofold band and spin degeneracy [13, 14]. The insulator capacitance, occurring between the tube and a plane, is given by [15]:

$$C_{\mathrm{Ins}} = \frac{2\pi\kappa\epsilon_0}{\cosh^{-1}(T_{\mathrm{Ins}}/R_{\mathrm{CNT}}+1)} \tag{10}$$

For the geometry parameters given in Fig. 1 $C_{\mathrm{Ins}} \approx 400\mathrm{aF}/\mu\mathrm{m}$. For a device with 50 nm channel length $C_{\mathrm{GG}} \approx 10\mathrm{aF}$. To calculate the gate-source and gate-drain parasitic capacitances we assumed the capacitance of two parallel plates, $C_{\mathrm{GS,GD}} = \kappa\epsilon_0 A/L_{\mathrm{S,D}}$, (see Fig. 1). Even with a small total area of $A = 250\ \mathrm{nm} \times 40\ \mathrm{nm}$ and a large spacer width of $L_{\mathrm{GS,GD}} = 10$ nm the parasitic capacitances $C_{\mathrm{GS}} + C_{\mathrm{GD}} \approx 260$ aF are much bigger than C_{GG}. As a result, $C_{\mathrm{G}} \approx C_{\mathrm{GS}} + C_{\mathrm{GD}} = \kappa\epsilon_0 A(1/L_{\mathrm{S}} + 1/L_{\mathrm{D}})$.

III. Simulation Results

In this section the effects of the gate-source spacer, gate-drain spacer, insulator thickness, and the insulator dielectric constant on the device characteristics are studied.

Due to ambipolar behavior, in the off-regime the drain current of CNTFETs starts to increase [3, 6, 16]. To reduce this effect we have proposed to increase the gate-drain spacer [7]. When increasing $\mathrm{L_D}$, the off-current decreases, while the on-current remains nearly unchanged, such that the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio increases. By increasing L_{D} the gate-drain parasitic capacitance decreases, which results in reducing the device delay time. Fig. 3 shows the effect of L_{D} on the device delay time versus $I_{\mathrm{on}}/I_{\mathrm{off}}$. As shown, a significant performance improvement is achieved. The disadvantage of this method is that at low drain biases electrons have to tunnel through a thicker barrier to reach the drain contact, resulting in a smaller drain current (Fig. 4).

When increasing L_{S}, the gate-source parasitic capacitance is reduced, and so is the on-current. The band edge profile near the source contact plays an important role in controlling the total current. Increasing L_{S} reduces the gate control of the band-edge profile near the source contact. Both the tunneling current and thermionic emission current contribute to the total current. Electrons with energies lower than the barrier height have to tunnel through the source-sided metal-CNT interface barrier to reach the channel while electrons

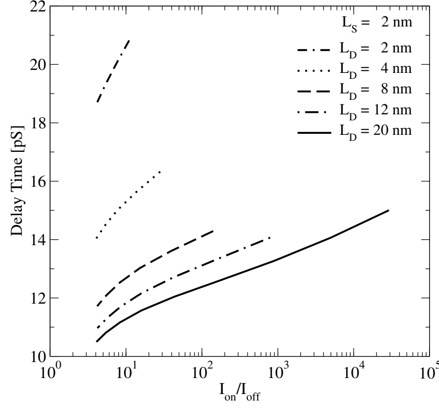

Fig. 3. The effect of $L_{\rm D}$ on the device delay time versus $\rm I_{on}/I_{off}$ ratio. $L_{\rm S} = 2$ nm and $V_{\rm DD} = 0.8$ V.

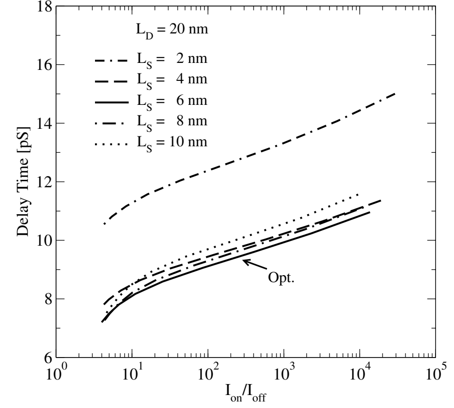

Fig. 5. The effect of $L_{\rm S}$ on the device delay time versus $\rm I_{on}/I_{off}$ ratio. $V_{\rm DD} = 0.8$ V. The optimal $L_{\rm S}$ for both device types are shown.

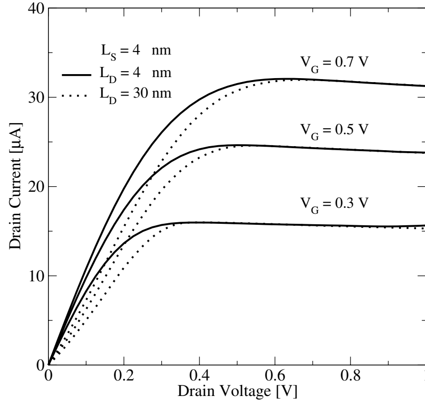

Fig. 4. Output characteristics at different gate biases for devices with $L_{\rm D} =$ 4 nm and $L_{\rm D} = 20$ nm. $L_{\rm S} = 4$ nm.

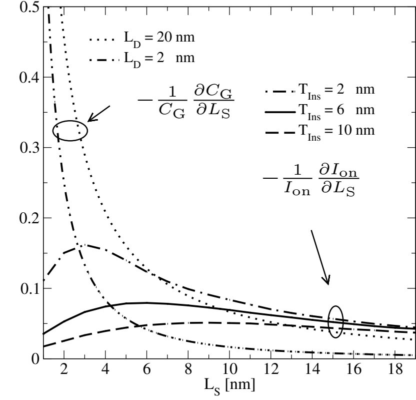

Fig. 6. The sensitivity of the parasitic capacitance and the on-current to $L_{\rm S}$ for different insulator thicknesses. The intersection of the curves gives the optimal $L_{\rm S}$, which minimizes τ.

with energies higher than the barrier height are injected by thermionic emission. Since the tunneling probability decreases exponentially with the barrier width, the tunneling current decreases with increasing $L_{\rm S}$. However, the thermionic emission current is independent of the barrier width. The contribution of the tunneling current decreases with decreasing barrier height, while that of thermionic emission increases. Since τ is proportional to the parasitic capacitance and inversely proportional to the on-current (9), there is an optimal value for $L_{\rm S}$, which minimizes τ. As shown in Fig. 5 the optimal value of $L_{\rm S}$ for the given material and geometrical parameters results in optimized device characteristics. It can be easily shown that the optimal value $\rm L_{S0}$, where $\frac{\partial \tau}{\partial L_{\rm S}}|_{\rm L_{S0}} = 0$, is achieved when $\frac{1}{C_{\rm G}}\frac{\partial C_{\rm G}}{\partial L_{\rm S}}|_{\rm L_{S0}} = \frac{1}{I_{\rm on}}\frac{\partial I_{\rm on}}{\partial L_{\rm S}}|_{\rm L_{S0}}$. Considering the expression derived for $C_{\rm G}$ in Section II.B, we have $\frac{1}{C_{\rm G}}\frac{\partial C_{\rm G}}{\partial L_{\rm S}} = [L_{\rm S}(1 + L_{\rm S}/L_{\rm D})]^{-1}$. Fig. 6 shows the sensitivity of the on-current to $L_{\rm S}$. However, the mentioned sensitivity is not zero due to the contribution of the tunneling current from states below the Fermi level. Since at positive gate biases the conduction band-edge is pushed below the source Fermi level, even in devices with zero barrier height the tunneling current can contribute to the total current. For thinner insulators the width of the source-sided barrier decreases, resulting in a higher tunneling current contribution to the total current and a higher sensitivity of the on-current to $L_{\rm S}$. The optimal spacer width is $L_{\rm S} \approx 6$ nm at $T_{\rm Ins} = 2$ nm and $L_{\rm D} = 20$ nm. Note that the optimal value for $L_{\rm S}$ depends on $L_{\rm D}$. For small values of $L_{\rm D}$ the gate-drain parasitic capacitance dominates the gate-source parasitic capacitance, therefore any further decrease of $L_{\rm S}$ does not improve the delay time.

Electron-phonon interaction reduces the on-current, both, directly and indirectly [17, 18]. The direct effect is due to backscattering of carriers, but scattering also redistributes the carrier concentration profile along the device. This redistribution affects the band-edge profile so that it reduces the total current. To reduce the indirect effect one should increase the gate-CNT coupling. If thin and High-κ insulators are used then $C_{\rm Ins} \gg C_{\rm Q}$ and $C_{\rm GG} \approx C_Q$, implying that the potential on the tube becomes the same as the gate (perfect coupling). This regime is called quantum capacitance limit in which the device is potential-controlled rather than charge-controlled [19]. Fig. 7 compares the ratio of the current in the presence of scattering to the ballistic limit for different insulators. For the given material and geometrical parameters a $\kappa > 20$ maximizes the performance of the device. But, with using high-κ materials not only the on-current but also

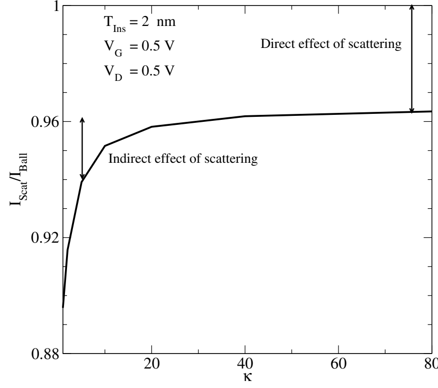

Fig. 7. The ratio of the drain current in the presence of scattering to the ballistic limit for different κ. The proportions due to direct and indirect effect of scattering on the on-current are shown. For high-κ the indirect part reduces.

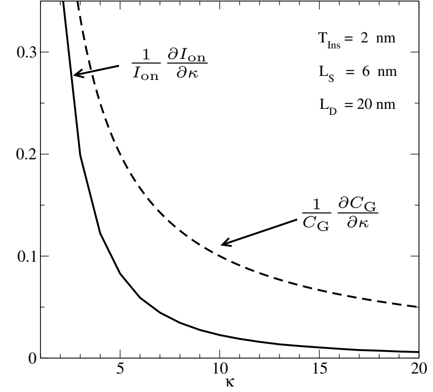

Fig. 8. The sensitivity of the parasitic capacitance and the on-current to κ. Since the curves do not intersect at high values of κ lower values of κ minimizes τ.

the parasitic capacitances increase. Therefore, there is a κ which optimizes the delay time. It can be shown that the optimized value is achieved when $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial \kappa}|_{\kappa 0} = \frac{1}{I_{\mathrm{on}}}\frac{\partial I_{\mathrm{on}}}{\partial \kappa}|_{\kappa 0}$. Considering the expression derived for C_{G} in Section II.B, we have $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial \kappa} = \frac{1}{\kappa}$. Fig. 8 shows the sensitivity of the on-current and parasitic capacitances to κ. Since the curves do not intersect at high values of κ, lower values minimizes τ. Therefore, there is a trade-off between device delay time and the on-current. For a specific application this parameter can be optimized.

IV. Conclusion

We showed that the device characteristics can be optimized by appropriately selecting the geometrical parameters. With increasing the gate-drain spacer, the off-current and the gate-drain parasitic capacitance reduce at the cost of a drain current reduction at low bias voltages. With increasing the gate-source spacer, the drain current and gate-source parasitic capacitance decrease. Since the device delay time is proportional to the parasitic capacitances and inversely proportional to the on-current, there is a value for the gate-source spacer which minimizes the device delay time. The optimal point is where the sensitivity of these quantities are equal. By using high-κ insulators the gate-CNT coupling increases which results in higher on-current, but the parasitic capacitances increase and as a result the device delay time increases.

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