Optimizing the Performance of Carbon Nanotube Transistors

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***Abstract*— A numerical study of carbon nanotube field effect transistors is presented. The non-equilibrium Green's function formalism was employed to investigate the static response. Based on the quasi-static approximation, the dynamic response has been determined. The effect of the gate-source and gate-drain spacers on the static and dynamic response of the device was studied. Simulation results suggest that both the dynamic and static characteristics of the device can be improved by appropriately designing the gate-source and gate-drain spacers.**

I. Introduction

Exceptional electronic and mechanical properties together with nanoscale diameter make carbon nanotubes (CNTs) promising candidates for nanoscale field effect transistors (FETs). In short devices (less than 100 nm) carrier transport through the device is nearly ballistic [1,2]. We employed the Non-Equilibrium Green's Function (NEGF) formalism to study the static response of CNTFETs. The Quasi Static Approximation (QSA) was used to investigate the dynamic response of these devices.

Depending on the work function difference between the metal contact and the CNT, carriers at the metal-CNT interface encounter different barrier heights. Fabrication of devices with positive (Schottky type) [3] and zero (ohmic) [1] barrier heights for holes have been reported. Devices with positive barrier height have lower on-current and exhibit severe ambipolar behavior [4], while devices with zero barrier height show better performance both theoretically [5] and experimentally [2]. We consider in this work devices with zero ($\Delta E_{Be} = 0$ eV) barrier heights for electrons. The barrier height for holes is given by $\Delta E_{Bh} = E_g - \Delta E_{Be}$. Since the dispersion relations for electrons and holes are the same, our discussions are valid for holes as well. In devices with positive barrier heights most carriers should tunnel through the source-sided barrier at the metal-CNT interface to reach the channel, while in devices with zero barrier height carrier are injected by thermionic emission. The gate voltage controls the current by modulating the transmission coefficient of carriers through the device [1]. However, unwanted ambipolar behavior can occur, which limits the static characteristics of the device by reducing the I_{on}/I_{off} ratio. We show that not only the ambipolar behavior and static characteristics, but also the dynamic characteristics of the device are improved by appropriately designing the gate-source and gate-drain spacers.

II. Approach

In this section the models used to study the static and dynamic response of CNTFETs are explained.

A. Static Response

Based on the NEGF formalism we studied the effect of device geometry on the performance of carbon nanotube field-effect transistors. We have solved the coupled system of transport and Poisson equations numerically. Due to quantum confinement along the tube circumference, carrier have bound wave functions around the CNT and can propagate along the tube axis. Under the assumption that the potential profile does not vary around the circumference of the CNT, sub-bands will be decoupled [6]. In this work we assume bias conditions for which the first sub-band contributes mostly to the total current. In the mode-space approach [6] the transport equation for each sub-band can be written as:

$$G^R = [EI - H - \Sigma^R]^{-1} \quad (1)$$

In (1) an effective mass Hamiltonian was assumed. All our calculations assume a CNT with band gap of $E_g = 0.6$ eV corresponding to a CNT with a radius of $R_{CNT} = 0.8$ nm, and $m^* = 0.05 m_0$ for both electrons and holes. The total self-energy in (1) consists of the self-energies due to the source contact, drain contact, and electron-phonon interaction, $\Sigma^R = \Sigma^R_S + \Sigma^R_D + \Sigma^R_{el-ph}$ [7]. In this work we assumed ballistic transport through the device, and the self energy due to electron-phonon interaction is neglected. Considering the contribution of the source and drain contacts, the total carrier concentration is calculated as:

$$n = \int G^R \Gamma_S G^A f(E - E_{FS}) dE + \int G^R \Gamma_D G^A f(E - E_{FD}) dE \quad (2)$$

where, $G^A = [G^R]^\dagger$ and $\Gamma_{S,D} = i(\Sigma_{S,D} - \Sigma^\dagger_{S,D})$. The carrier charge was taken into account as sheet charge distributed uniformly over the surface of the CNT [8].

The Landauer-Büttiker formula is used to calculate the current through the device:

$$I = \frac{4q}{h} \int [f(E - E_{FS}) - f(E - E_{FD})] TC(E) dE \quad (3)$$

where $TC(E) = \mathrm{tr}\{\Gamma_S G^R \Gamma_D G^A\}$ is the transmission coefficients of carriers.

The coupled system of transport and Poisson equation is solved iteratively. Details are presented in [7].

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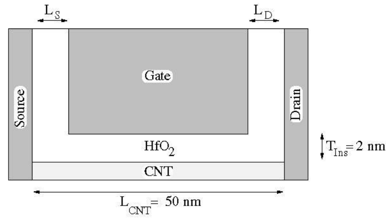

Fig. 1. Sketch of the device. $T_{\text{Ins}} = 2$ nm, $L_{\text{CNT}} = 50$ nm and $\epsilon_{\text{r}} = 15$.

B. Dynamic Response

To investigate the dynamic response of the device we consider the device delay time defined as:

$$\tau = \frac{C_{\text{G}} V_{\text{DD}}}{I_{\text{on}}} \tag{4}$$

Here, $C_{\text{G}} = C_{\text{GS}} + C_{\text{GD}} + C_{\text{GG}}$ with ${C_{\text{GG}}}^{-1} = {C_{\text{Ins}}}^{-1} + {C_{\text{Q}}}^{-1}$. The quantum capacitance is given by $C_{\text{Q}} = 8\text{q}^2/\text{h}\nu_{\text{F}} \approx 400\text{aF}/\mu\text{m}$, including the twofold band and spin degeneracy [9]. The insulator capacitance, occurring between the tube and a plane, is given by[10]:

$$C_{\text{Ins}} = \frac{2\pi\epsilon}{\cosh^{-1}(T_{\text{Ins}}/R_{\text{CNT}} + 1)} \tag{5}$$

For the geometry parameters given in Fig. 1 $C_{\text{Ins}} \approx 400\text{aF}/\mu\text{m}$. For a device with 50 nm channel length $C_{\text{GG}} \approx 10\text{aF}$. To calculate the gate-source and gate-drain parasitic capacitances we assumed the capacitance of two parallel plates, $C_{\text{GS,GD}} = \epsilon A/L_{\text{S,D}}$, (see Fig. 1). Even with a small total area of $A = 200$ nm × 25 nm and a large spacer width of $L_{\text{GS,GD}} = 10$ nm the parasitic capacitances $C_{\text{GS}} + C_{\text{GD}} \approx 130$ aF are much bigger than C_{GG}. As a result, $C_{\text{G}} \approx C_{\text{GS}} + C_{\text{GD}} = \epsilon A\{1/L_{\text{S}} + 1/L_{\text{D}}\}$. To normalize τ we assumed $A = 1\ \text{nm}^2$.

III. The Effect of Geometry on the Device Characteristics

In this section the effect of the spacer widths L_{S} and L_{D} on the static and dynamic response of CNTFETs is studied. For the static response the output and transfer characteristics are compared, and for the dynamic response the device delay

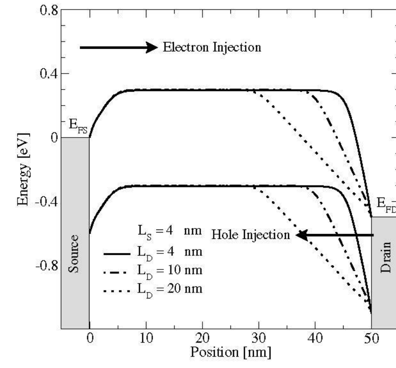

Fig. 3. The effect of L_{D} on the band-edge profiles of the device with $\Delta\text{E}_{\text{Be}} = 0.0$ eV. $\text{V}_{\text{G}} = -0.5$ V and $\text{V}_{\text{D}} = 0.5$ V.

time versus the $I_{\text{on}}/I_{\text{off}}$ ratio. The latter figure of merit can be used to compare devices with different geometries and material properties [11].

A. The Effect of L_{D} on the Device Characteristics

The transfer characteristics at different drain biases are shown in Fig. 2. In the off-regime (negative gate bias) the drain current of CNTFETs starts to increase, and by increasing the drain bias this phenomenon becomes more apparent [2, 12]. This effect is due to the ambipolar behavior of these devices, which can be well understood by considering the band edge profiles. As shown in Fig. 3, if the drain voltage becomes higher than the gate voltage, the barrier thickness for holes at the drain contact is reduced and the tunneling current of holes increases. At the minimum current points in Fig. 2, electrons and holes have the same contribution to the total current, whereas in other regions either the electron or hole contribution will dominate. By increasing L_{D} the band edge profile near the drain contact is less affected by the gate voltage (Fig. 3). Therefore, when the voltage between the gate and drain contacts increases the barrier thickness for holes near the drain contact is less reduced, and as a result the tunneling current of holes is suppressed. Fig. 4 compares the transfer characteristics of devices with different L_{D}. When increasing L_{D}, the ambipolar behavior is suppressed and the off-current decreases, while the on-current remains nearly unchanged,

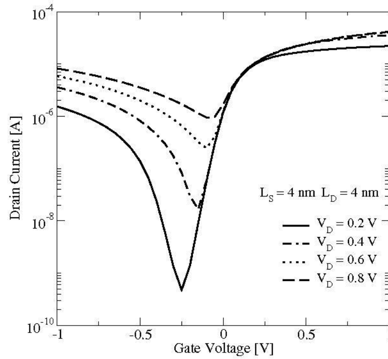

Fig. 2. Transfer characteristics at different drain biases.

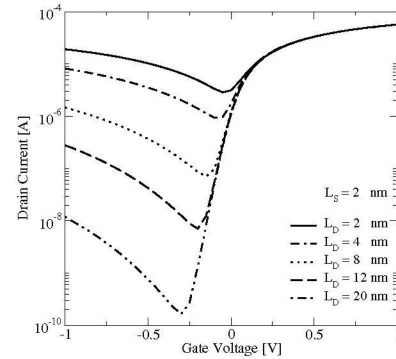

Fig. 4. The effect of L_{D} on the transfer characteristics.

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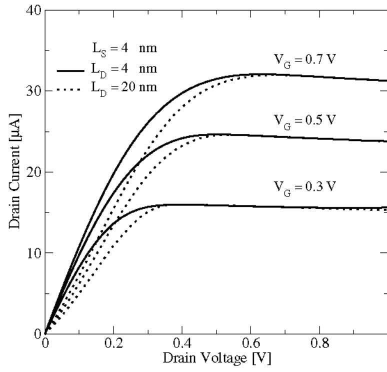

Fig. 5. Output characteristics at different gate biases for devices with $L_{\mathrm{D}} = 4$ nm and $L_{\mathrm{D}} = 20$ nm. $L_{\mathrm{S}} = 4$ nm.

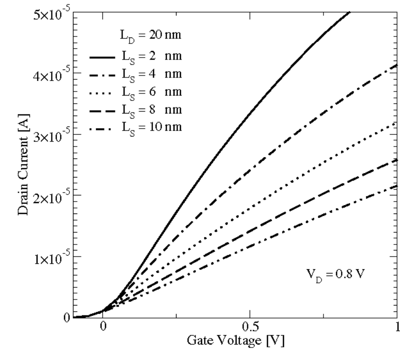

Fig. 7. The effect of L_{S} on the transfer characteristics. $L_{\mathrm{D}} = 20$ nm and $V_{\mathrm{D}} = 0.8$ V

such that the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio increases. The disadvantage of increasing L_{D} is that at low drain biases electrons have to tunnel through a thicker barrier near the drain contact, resulting in a smaller drain current at low drain voltages (Fig. 5). This phenomenon is more apparent in devices with positive barrier heights for electrons at the drain-CNT interface [4, 8].

In devices with positive barrier heights the ambipolar behavior is more apparent due to lower barrier height for holes. To avoid this problem, we have shown that a double gate structure can be used to strongly suppress the ambipolar behavior of such devices [4] without reducing the drain current at low drain biases. In a double gate device the carrier injection at the source and drain contacts is controlled separately. However, addition of a gate increases the parasitic capacitance.

Increasing L_{D} increases the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, while the gate-drain parasitic capacitance decreases. As show in Fig. 6, increasing L_{D} improves the device delay time versus $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio by several orders of magnitude.

B. The Effect of L_{S} on the Device Characteristics

The band edge profile near the source contact plays an important role in controlling the total current. Increasing L_{S} reduces the gate control of the band-edge profile near the source contact. Both the tunneling current and thermionic emission current contribute to the total current. Electrons with energies lower than the barrier height have to tunnel through the source-sided metal-CNT interface barrier to reach the channel while electrons with energies higher than the barrier height are injected by thermionic emission. Since the tunneling probability decreases exponentially with the barrier width the tunneling current decreases with increasing L_{S}. But, the thermionic emission current is independent of the barrier width. Contribution of tunneling current decreases with decreasing barrier height, while that of the thermionic emission increases. However, even for devices with zero barrier height the mentioned sensitivity is not negligible due to the contribution of the tunneling current from states below the Fermi level. Since at positive gate biases the conduction band-edge is pushed below the source Fermi level, even in devices with zero barrier height the tunneling current can contribute to the total current. For thiner insulators the width of the source-sided barrier decreases, resulting in a higher tunneling current contribution to the total current and a higher sensitivity of the on-current to L_{S} Fig. 8.

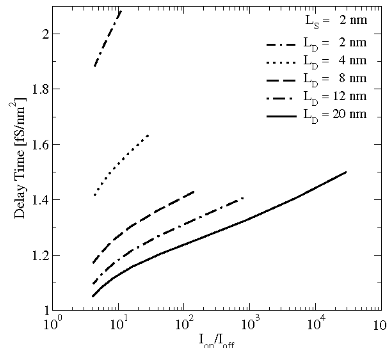

Fig. 6. The effect of L_{D} on the device delay time versus $\mathrm{I_{on}/I_{off}}$ ratios.

When increasing L_{S}, the gate-source parasitic capacitance is reduced, and so is the on-current. Since τ is proportional to the parasitic capacitance and inversely proportional to the on-current (4), there is an optimal value for L_{S}, which minimizes τ. It can be easily shown that the optimal value $\mathrm{L_{S0}}$, where $\frac{\partial \tau}{\partial L_{\mathrm{S}}}|_{\mathrm{L_{S0}}} = 0$, is achieved when $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial L_{\mathrm{S}}}|_{\mathrm{L_{S0}}} = \frac{1}{I_{\mathrm{on}}}\frac{\partial I_{\mathrm{on}}}{\partial L_{\mathrm{S}}}|_{\mathrm{L_{S0}}}$. Considering the expression derived for C_{G} in Section II.B, we have $\frac{1}{C_{\mathrm{G}}}\frac{\partial C_{\mathrm{G}}}{\partial L_{\mathrm{S}}} = \frac{1}{L_{\mathrm{S}}(1+L_{\mathrm{S}}/L_{\mathrm{D}})}$. Fig. 8 compares the optimal L_{S} for devices with different barrier height, T_{Ins} and L_{D}. In devices with zero barrier height the on-current is less sensitive to L_{S}, resulting in a large, optimal spacer width ($L_{\mathrm{S}} \approx 6$ nm at $T_{\mathrm{Ins}} = 2$ nm and $L_{\mathrm{D}} = 20$ nm). With the increase of the barrier height the sensitivity of the on-current to L_{S} increases and optimal spacer widths become smaller ($L_{\mathrm{S}} \approx 3-4$ nm at $T_{\mathrm{Ins}} = 2$ nm and $L_{\mathrm{D}} = 20$ nm). As shown in Fig. 9 the optimal value of L_{S} for the given material and geometrical parameters results in optimized device characteristics. Note that the optimal value for L_{S} depends on L_{D}. For small values of L_{D} the gate-drain parasitic capacitance dominate the gate-source parasitic capacitance, therefore further decrease of L_{S} does not improve the delay time.

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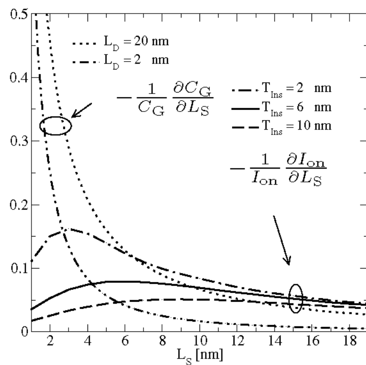

Fig. 8. The sensitivity of the parasitic capacitance and the on-current to L_S for different insulator thicknesses. The intersection of the curves gives the optimal L_S, which minimizes τ.

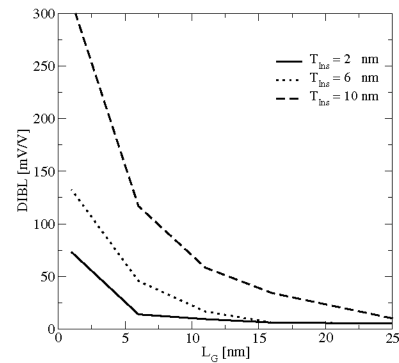

Fig. 10. The effect of L_G on the DIBL effect.

IV. Discussions

We showed that an appropriate selection of L_S and L_D improves both the static and dynamic response of the device. The results are based on two assumptions, namely that a) parasitic capacitances dominate quantum and insulator capacitances and b) transport is ballistic. As discussed in Section II.B, for most parameter values parasitic capacitances dominate quantum and insulator capacitances. However, if this condition is not satisfied the total capacitance would not be decreased by a further increase of the spacer width. The assumption of ballistic transport is theoretically justified for the short devices considered in this work [13, 14]. Experimental results indicate that short channel CNTFETs, with channel lengths less than several hundred nanometer, can operate close to the ballistic limit [2].

To avoid drain induced barrier lowering (DIBL), the length of the gate contact L_G should not be too short. Fig. 10 shows that for $L_G > 20$ nm the DIBL effect is not important. In devices with thin insulators the insulator capacitance can be larger than the quantum capacitance, such that $C_G \approx C_Q$. Under this condition the gate has good control over the channel. Therefore, with decreasing insulator thickness, the DIBL effect reduces. For very small gate-lengths (≈ 2 nm) observation of Coulomb blockade effects has been reported [15]. However, in this work we assumed gate lengths in the range $20 - 40$nm, so that Coulomb blockade is not important.

As discussed in [16], the QSA is valid for frequencies below 4 THz. Therefore, as long as the calculated delay time is above the pS range for the given geometry the QSA approximation remains valid.

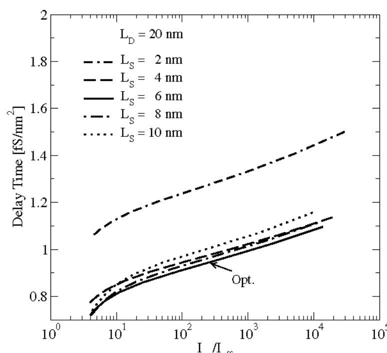

Fig. 9. The effect of L_S on the device delay time versus I_{on}/I_{off} ratios. $L_D = 20$ nm and $V_{DD} = 0.8$ V. The optimal L_S is shown.

V. Conclusion

We showed that both the static and dynamic responses of CNTFETs can be improved by appropriately designing the gate-source and gate-drain spacers. We showed that increasing the gate-drain spacer suppresses the ambipolar behavior and reduces the gate-drain parasitic capacitance. When increasing the gate-source spacer, both the on-current and the gate-source parasitic capacitance are decreased, which implies that the device delay time can be optimized for given geometrical and material parameters. Our discussions are based on the assumption that carrier transport in the device is ballistic and that parasitic capacitances dominate the quantum and insulator capacitances.

Acknowledgment

This work was partly supported by the European Commission, contract No. 506844 (NoE SINANO), and the National Program for Tera-level Nano-devices of the Korea Ministry of Science and Technology as one of the 21st Century Frontier Programs.

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