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Numerical Analysis of Gate Stacks

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An efficient software tool for investigations on novel stacked gate dielectrics with emphasis on reliability has been developed. The accumulation, depletion, and inversion of carriers in MOS capacitors is properly considered for n- and p-substrates. The effect of carrier quantization on the electrostatics and the leakage current is included by treating carriers in quasi-bound states (QBS) and continuum states. The effect of interface traps and bulk traps in arbitrarily stacked gate dielectrics is taken into account. Trap assisted tunneling (TAT) is incorporated assuming an inelastic single step tunneling process. A brief overview of implemented models is given. The capabilities of our tool are demonstrated by several examples.

Introduction

In order to enable further device down-scaling to the decananometer channel length regime numerous technological innovations including material and process changes such as high-κ gate dielectrics and metal gate electrodes, are currently investigated (1). For future CMOS devices the use of high-κ gate dielectrics provides an option to keep the gate leakage current within tolerable limits while retaining a good control over the inversion charge (2). Gate stacks consisting of layers of high-κ dielectrics such as Si_3N_4, Al_2O_3, Ta_2O_5, HfO_2, or ZrO_2 have been suggested. The relevant parameter values for these materials reported in (3)-(9) are summarized in Tab. I. The different conduction band offsets of a SiO_2/HfO_2 gate stack can be seen in Fig. 1. To overcome the technological problems, further theoretical and experimental research including the use of computer simulation is needed. We present a software tool, the Vienna Schrödinger Poisson solver (VSP), for the numerical analysis of novel gate stacks (10).

The software is written in C++ using state-of-the-art software design techniques. VSP offers a graphical user interface, as well as an XML based interface. Furthermore, VSP has an open software application interface (API) for integration into third party simulation environments. These features are mandatory for tasks such as parameter

Table I: Permittivity, band gap, and conduction band offset of gate stack materials.

	Permittivity κ/κ_0 [1]	Band gap $\mathcal{E}_g$ [eV]	Band offset $\Delta\mathcal{E}_C$ [eV]
SiO_2	3.9	8.9 – 9.0	3.0 – 3.5
Si_3N_4	7.0 – 7.9	5.0 – 5.3	2.0 – 2.4
Al_2O_3	7.9 – 12.0	5.6 – 9.0	2.78 – 3.5
ZrO_2	12.0 – 25.0	5.0 – 7.8	1.4 – 2.5
HfO_2	16.0 – 40.0	4.5 – 6.0	1.5
Ta_2O_5	23.0 – 26.0	4.4 – 4.5	0.3 – 1.5
TiO_2	39.0 – 170.0	3.0 – 3.5	0.0 – 1.2

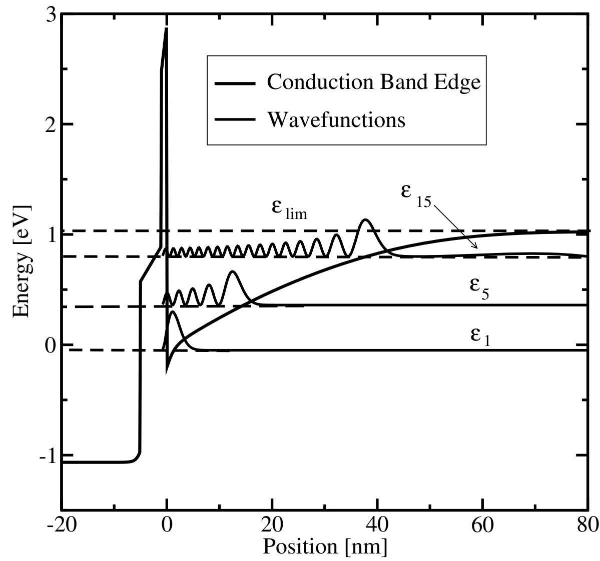

Fig. 1: The conduction band edge of an NMOS inversion layer with a stacked gate dielectric. A potential potential well with a finite height $\mathcal{E}_{lim}$ forms. The wavefunctions and the energy levels of three quasi-bound states are shown.

identification and model calibration, for example, for CV-characteristics and gate stack optimizations. Binaries are available for Linux, Windows, IBM AIX, and MacOs on request.

The Models

This section briefly describes the models implemented in the Schrödinger Poisson (S/P) solver. The chosen software architecture allows new models to be added easily. VSP is a quantum mechanical solver for closed as well as open boundary problems. The thereby calculated carrier concentration is used in the Poisson equation in a self consistent manner. Quantization effects can be treated in both, in the Si substrate and in the poly-Si gate.

The Poisson Model

The Poisson equation describes the relation between the electrostatic potential φ and the space charge ρ.

$$\nabla \cdot (\varepsilon \nabla\varphi) + \rho(\varphi) = 0 \qquad [1]$$

Hence, for S/P calculations a system of coupled partial differential equations (PDE) has to be solved self-consistently. We use an iterative predictor corrector scheme (11) in order to achieve a fast and stable convergence behavior. For each iteration step i, a linearized Poisson equation has to be solved:

$$\nabla \cdot (\varepsilon\nabla\varphi^i) + \varphi^i \frac{\partial\rho}{\partial\varphi}\Big|_{\varphi^{i-1}} = -\rho(\varphi^{i-1})\,. \qquad [2]$$

Effective Mass Approach

The band structure for electrons and holes is given by an arbitrary number of valley sorts, defined by an anisotropic effective mass and a band edge energy (12) (see Fig. 2). In this way a wide range of materials can be treated. Also, the effects of substrate orientation and strain on the band structure can be taken into account.

Closed System Carrier Density

The energy levels $\mathcal{E}_n$ and the wave functions Ψ_n of bound states within a quantum well follow from the effective mass Schrödinger equation:

$$\left(-\frac{\hbar^2}{2}\frac{\partial}{\partial x}\frac{1}{m(x)}\frac{\partial}{\partial x} + V(x)\right)\Psi(x) = \mathcal{E}\,\Psi(x)\,. \qquad [3]$$

For a well with a finite barrier height $\mathcal{E}_{\mathrm{lim}}$ (e.g. for a MOS inversion layer shown in Fig. 1), the occupation of the subband states is considered up to this energy. The

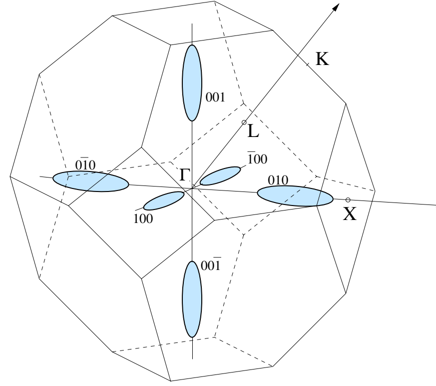

Fig. 2: Equi-energy surfaces of the first conduction band of unstrained Silicon. VSP treats the conduction band as three valleys having the same minimum energy but different orientations of the effective mass tensor.

electron density is given by the effective DOS of a two-dimensional electron gas $N_{\mathrm{C,2D}}$ and the incomplete Fermi function $\mathcal{F}_0(x,b)$ as follows.

$$n_{\mathrm{C,2D}}(x) = N_{\mathrm{C,2D}} \sum_n |\Psi_n(x)|^2 \times \left(\mathcal{F}_0\left(\frac{\mathcal{E}_\mathrm{F}-\mathcal{E}_n}{\mathrm{k_B}T}, 0\right) - \mathcal{F}_0\left(\frac{\mathcal{E}_\mathrm{c}-\mathcal{E}_\mathrm{F}}{\mathrm{k_B}T}, \frac{\mathcal{E}_\mathrm{c}-\mathcal{E}_\mathrm{lim}}{\mathrm{k_B}T}\right)\right) \quad [4]$$

Starting at $\mathcal{E}_\mathrm{lim}$, a continuum of states is assumed, carrying the electron density

$$n_{\mathrm{C,3D}}(x) = N_{\mathrm{C,3D}}\ \mathcal{F}_{1/2}\left(-\frac{\mathcal{E}_\mathrm{c}-\mathcal{E}_\mathrm{F}}{\mathrm{k_B}T}, -\frac{\mathcal{E}_\mathrm{lim}-\mathcal{E}_\mathrm{c}}{\mathrm{k_B}T}\right) . \quad [5]$$

The total electron density is the sum of the two contributions: $n_\mathrm{C} = n_{\mathrm{C,2D}} + n_{\mathrm{C,3D}}$. Similar expressions apply for holes. The treatment of carriers in the non-quantized energy regime is mandatory to handle carrier accumulation properly.

Bulk and Interface Trap Charges

VSP includes models for interface traps and bulk traps in arbitrarily stacked gate dielectrics. The occupation of the bulk traps can be defined by the user. The occupation of the two-dimensional interface states g_int is calculated using Fermi statistics (13). The surface charge is given by

$$\rho_\mathrm{int} = \mathrm{q} \int_{\mathcal{E}_\mathrm{min}}^{\mathcal{E}_\mathrm{max}} g_\mathrm{int}(\mathcal{E}_x)\, f(\mathcal{E}_x)\, \mathrm{d}\mathcal{E}_x \, . \quad [6]$$

The hereby calculated bulk and surface charges enter the Poisson equation, and hence have to be evaluated at each iteration step.

Direct Tunneling Current

The leakage current is calculated in a post processing step, since it has a negligible influence on the electrostatic potential. The direct tunneling current components from both continuum J_{3D} and quasi-bound states (QBS) J_{2D} are taken into account according to (14). Following (15), these direct tunneling current components can be estimated by

$$J_{\mathrm{d,2D}} = \mathrm{q}\sum_i \frac{n_i}{\tau_i}\,, \qquad [7]$$

$$J_{\mathrm{d,3D}} = \mathrm{q}\int_{\mathcal{E}_{\mathrm{lim}}}^{\mathcal{E}_{\mathrm{max}}} TC(\mathcal{E}_x, m_{\mathrm{diel}}) N(\mathcal{E}_x, m_{\mathrm{D}})\,\mathrm{d}\mathcal{E}_x\,. \qquad [8]$$

The lifetime τ_i of the ith QBS is evaluated based on a semiclassical approximation (14) or a more rigorous formulation using the complex energy eigenvalues of the Schrödinger equation with open boundary conditions (16).

Trap Assisted Tunneling Current

Trap assisted tunneling (TAT), which is a major reliability issue in novel gate stacks (17), is modeled by an inelastic single step tunneling process (18) as depicted in Fig. 3. The current density reads:

$$J_{\mathrm{tat}} = \mathrm{q}\int_0^{t_{\mathrm{ox}}} \frac{N_{\mathrm{t}}(x)}{\tau_{\mathrm{c}}(x)+\tau_{\mathrm{e}}(x)}\,\mathrm{d}x\,. \qquad [9]$$

Here τ_{c} and τ_{e} denotes the capture and emission times of the traps, respectively, and $N_{\mathrm{t}}(x)$ gives the spatial distribution of the trap density. The model has been calibrated to measurements.

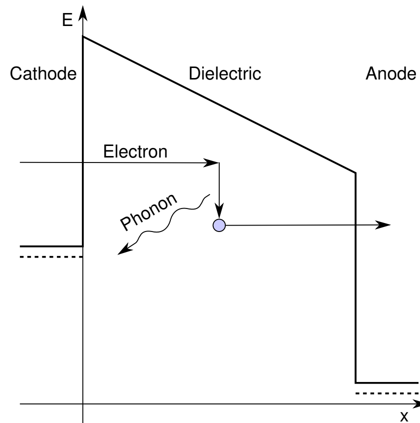

Fig. 3: The trap assisted tunneling process, where the excess energy of the tunneling electrons is released by means of phonon emission.

Application and Results

Conventional bulk MOS, partially depleted SOI, and novel device designs like DG-MOS structures can be investigated. With the described software package, NMOS structures with various gate dielectrics and gate materials have been simulated. For instance, the band edge energy of a MOS structure with a stacked gate dielectric under inversion conditions has been evaluated. The conduction band edge and some of the QBS are depicted in Fig. 1. A doping concentration of $N_{\mathrm{A}}=5 \times 10^{17}\mathrm{cm}^{-3}$ in the bulk and $N_{\mathrm{D}}=1 \times 10^{19}\mathrm{cm}^{-3}$ in the poly-silicon gate was assumed.

The capacitance voltage characteristics (CV) of MOS structures with different effective oxide thicknesses (EOT) including a Si_3N_4 layer are plotted in Fig. 4. The corresponding leakage currents are shown in Fig. 5. A nearly exponential increase of the leakage current by decreasing the oxide thickness can be clearly seen. Furthermore, structures including a layer of HfO_2 have been analyzed. The CV characteristics using a metal gate and a poly silicon gate are shown in Fig. 6. The effect of poly depletion can be clearly seen. The properties are considerably improved due the metal gate. Hence, the use of a metal gate is reasonable for further down scaling the EOT.

VSP has the capability to evaluate the static and the high-frequency CV characteristics of MOS structures. This feature is demonstrated in Fig. 7 showing the high-frequency CV curves which can be easier obtained by measurement than the static one. The influence of states at the semiconductor insulator interface for various density interface states (DIT) profiles (see Fig. 8) has been investigated. The corresponding CV characteristics are shown in Fig. 9.

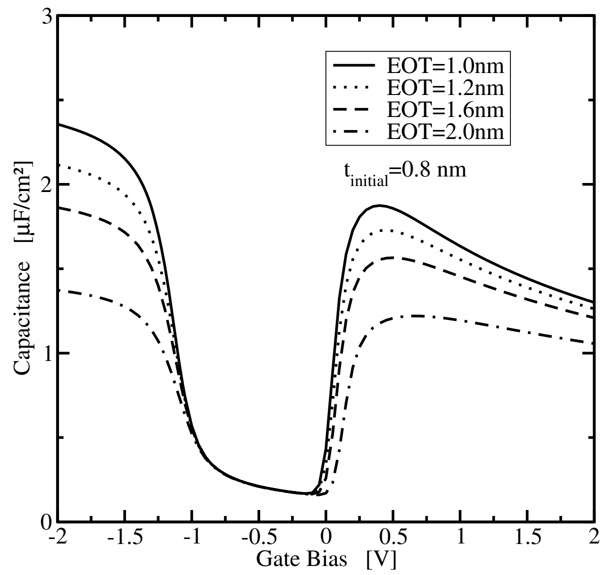

Fig. 4: The CV characteristics of SiO_2/Si_3N_4 stacked gate dielectrics for different EOTs. An initial SiO_2 layer of 0.8 nm has been assumed.

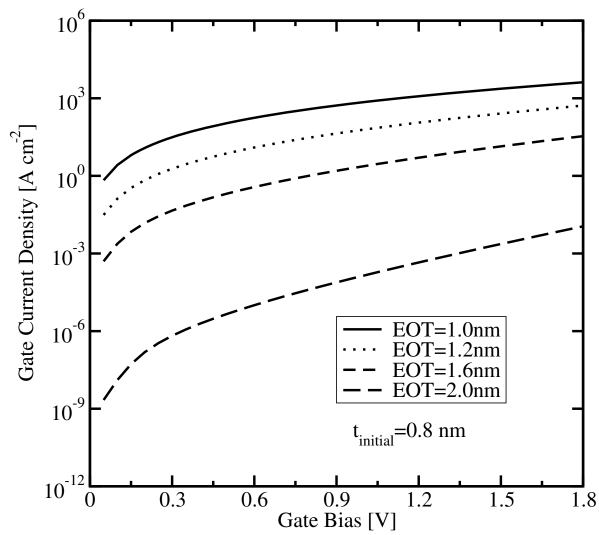

Fig. 5: The gate current density of SiO_2/Si_3N_4 stacked gate dielectrics at several EOTs.

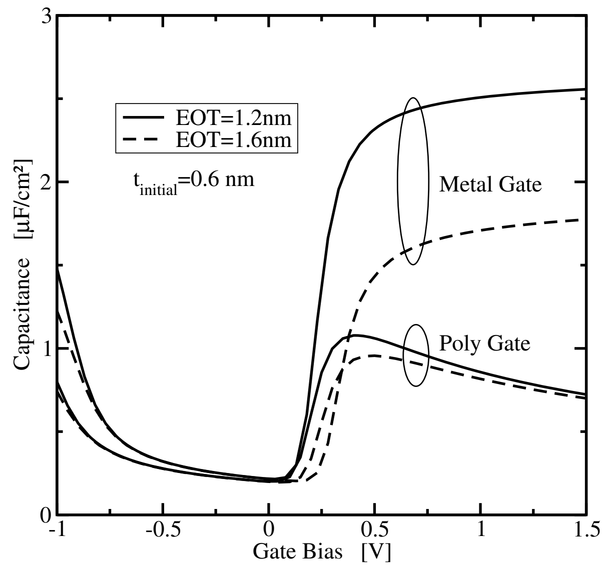

Fig. 6: The CV characteristic of SiO_2/HfO_2 stacked gate dielectrics for different EOTs. Metal gates are suitable for scaling the EOT down.

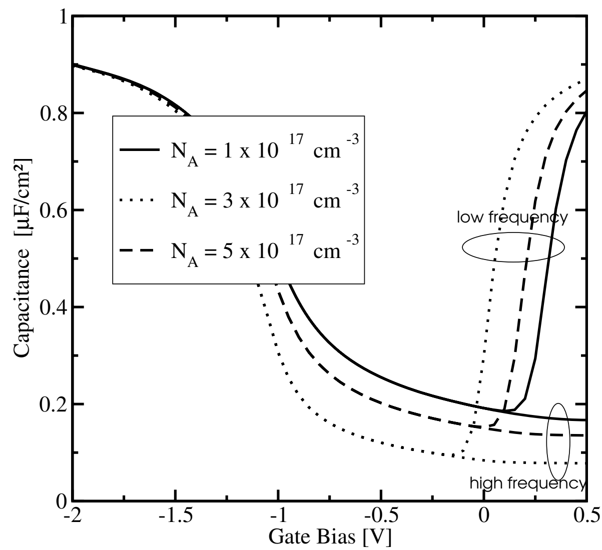

Fig. 7: The static and the high frequency CV characteristics of an NMOS structure with different substrate doping concentrations.

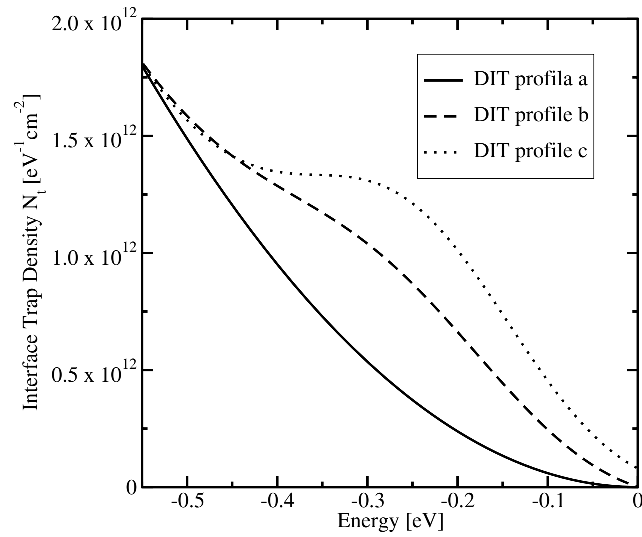

Fig. 8: The distribution of interface trap density versus energy. The value zero corresponds to the middle of the bandgap in the bulk Si.

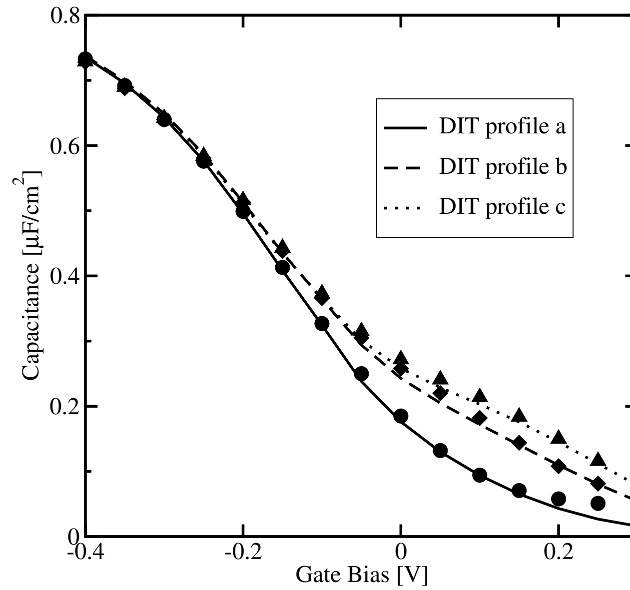

Fig. 9: The circles, the diamonds, and the triangles show CV measurements of an example gate stack at 1 kHz, 10 kHz, and 1MHz, respectively. The simulated CV characteristics assuming the DIT profiles as shown in Fig. 8 can reproduce the measurement data.

Summary

We developed the Vienna Schrödinger Poisson solver (VSP), a multi-purpose quantum mechanical solver, with the aim to aid theoretical as well as experimental research on novel gate dielectrics. A brief overview of models implemented in VSP including direct- and trap assisted tunneling has been given. Furthermore, some relevant features have been demonstrated by several examples.

Acknowledgments

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