Enhancement Mode HEMTs: Evaluation of Two Approaches by Numerical Simulation

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Abstract — *Normally-off operation of high electron mobility transistors is desired for many reasons, however proved to be difficult to achieve, despite the rapid development of the depletion mode devices. Amongst the few approaches proposed so far, we focus on two, which promise high performance. The first device features an InGaN cap layer, while the later relies on gate recess technology. We perform DC and AC analyses, using our device simulator calibrated against experimental data, and compare the performance of the devices based on simulation results.*

I. Introduction

The transport and material properties of GaN and AlN and their heterostructures have encouraged the research of AlGaN/GaN based transistors for various applications in the last decade. Consequently, outstanding results have been reported for the depletion mode (D-mode) high electron mobility transistors (HEMTs). However, for several applications enhancement mode (E-mode) devices are essential. In analog electronics they supersede the negative voltage supply and also assure a safe state in case of power loss. In digital electronics, they allow complementary logic.

Despite the interest in E-mode operation, the excellent results as in D-mode devices remain to be seen. The first E-mode transistor was reported back in 1996 by Khan *et al.* [1], and several other refinements followed. In this paper we focus on two recently proposed approaches. The first relies on gate recess combined with fluorine based surface treatment, while the second incorporates a thin InGaN layer, which raises the conduction band. For the study of the devices we use our two-dimensional device simulator MINIMOS-NT.

II. Device Structure with InGaN-Cap

The InGaN/AlGaN/GaN device structure was proposed by Mizutani *et al.* [2]. A 3 μm thick GaN layer is grown on sapphire substrate. A 20 nm thick $Al_{0.25}Ga_{0.75}N$ supply layer follows (5 nm undoped, 10 nm highly-doped, and 5 nm undoped). A 5 nm non-intentionally doped $In_{0.2}Ga_{0.8}N$ layer is deposited next. The gate length l_g=1.9 μm, source-gate distance is 1.5 μm, and gate-drain distance is 2.4 μm.

III. Device Structure with Recessed Gate

The gate recess structure and its fabrication is reported by Palacios *et al.* [3]. The 11 nm thick GaN channel is grown on-top of a 1 nm thick $In_{0.1}Ga_{0.9}N$ back-barrier. A 1 nm thick AlN layer between the channel and the 25 nm $Al_{0.33}Ga_{0.67}N$ is grown in order to improve the electron mobility. After the AlGaN surface treatment a 12 nm gate recess is performed, resulting in a gate-to-channel distance of 13 nm. The gate length l_g is 160 nm, source-gate distance is 0.6 μm, and gate-drain distance is 0.9 μm.

IV. Simulation Setup

The device simulator MINIMOS-NT has proven to be a suitable tool for the analysis of heterostructure devices [4]. Recently, it has been used for the study of a whole generation of AlGaN/GaN HEMTs [5]. Since the longitudinal electric field in the channel reaches peak values of above 500 kV/cm, the hydrodynamic transport model is used to properly model electron transport and energy relaxation. Self-heating effects are accounted for by using a global self-heating model, which calculates a spatially constant lattice temperature. The value of the sheet charge at the AlGaN/GaN interface induced by the polarization effects is derived from the DC characteristics. Additional charges at the InGaN and AlGaN interfaces are accounted for [6].

V. Simulation Results

Figure 1 shows the results for the transfer characteristics of both devices. After a calibration of the sheet charges a good agreement is achieved. The InGaN/GaN device exhibits lower current, however a higher threshold voltage is achievable, without recessing the InGaN cap layer [2]. The threshold voltage of the recess device can be increased too (Figure 2) by increasing the recess depth.

Figure 3 compares the DC transconductance g_m for both devices. The decrease in the measured g_m of the InGaN/AlGaN/GaN transistor at higher gate bias, might be due to non-idealities in the source and drain ohmic contacts, which are not considered in the simulation.

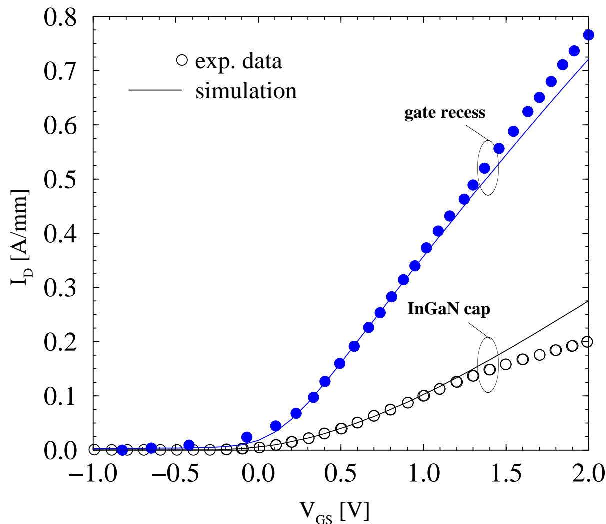

Figure 1: Comparison of the measured (symbols) and simulated (lines) transfer characteristics at V_{ds}=5 V.

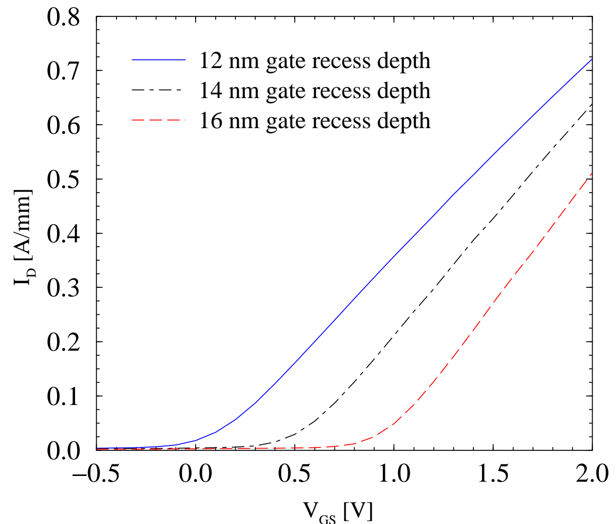

Figure 2: Simulated transfer characteristics at V_{ds}=5 V for HEMTs with different gate recess depths.

As expected, the recessed gate device exhibits a higher g_m due to the much shorter gate length l_g and the reduced gate-to-channel separation.

We also perform an AC analysis of the transistors. The recessed gate structure (l_g=0.16 μm) exhibits transit cut-off frequency f_T=85 GHz, while our simulation gives f_T=10 GHz for the InGaN/AlGaN/GaN device (l_g=1.9 μm). Note, that the product $f_T \times l_g$=19 GHz·μm is higher than 14.4 GHz·μm of the recessed-gate device. Our simulation of an InGaN cap structure with l_g=0.8 μm shows that f_T=30 GHz can be achieved.

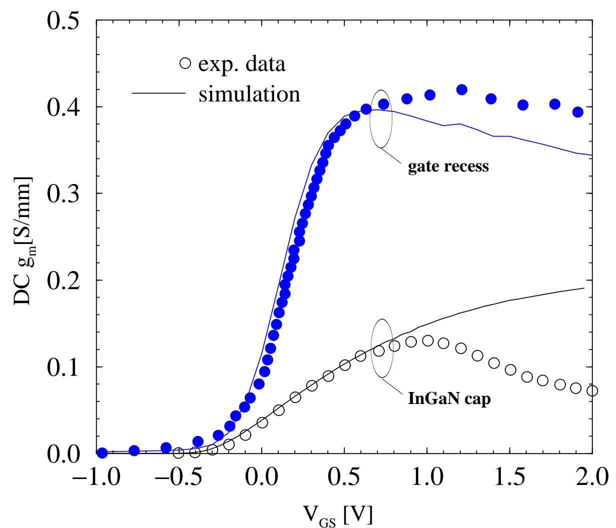

Figure 3: Comparison of the measured (symbols) and simulated (lines) DC transconductance g_m at V_{ds}=5 V.

VI. Conclusion

After a calibration against experimental data our device simulator provides reliable results for the DC and AC performance of the investigated novel HEMTs. This allows us to perform further device optimization, e.g. for higher current capability, higher threshold voltage, and better AC performance.

Acknowledgments

The authors acknowledge support from the Austrian Science Fund (FWF), Project START Y247-N13.

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