Modeling Thermal Effects in Nanodevices

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***Abstract*—In order to investigate the role of self-heating effects on the electrical characteristics of nanoscale devices, we implemented a 2-D Monte Carlo device simulator that includes the self-consistent solution of the energy balance equations for both acoustic and optical phonons. The acoustic and optical phonon temperatures are fed back into the electron transport solver through temperature-dependent scattering tables. The electrothermal device simulator was used in the study of different generations of nanoscale fully depleted silicon-on-insulator devices that are either already in production or will be fabricated in the next five to ten years. We find less degradation due to self-heating in very short channel device structures due to the increasing role of nonstationary velocity-overshoot effects which are less sensitive to the local temperature.**

***Index Terms*—Acoustic and optical phonons, Boltzmann transport equation (BTE), nanodevices, particle-based device simulations, scaling, thermal effects.**

I. Introduction

IT IS WELL known [1] that heat generation and the associated thermal management in very large scale integrated circuits (or nanoscale devices) are some of the major barriers to further increase clock speeds and decrease feature size. The modern semiconductor industry benefits greatly from device scaling for the purpose of improving the device performance and reducing the manufacturing cost [1]. It is predicted that, when the device dimension scales down for a factor of F, the power-consumption density usually increases by a factor of F^2 or F^3 for the case of constant voltage scaling. In addition, for conventional CMOS devices, by scaling them down to nanometer dimensions, it was predicted that the characteristic phonon hot-spot region [2] near the drain would not scale proportionally. The size of the phonon hot spot is on the order of the magnitude of the high electric field region near the drain in a 180-nm device. What happens in nanoscale devices is very difficult to predict. As it will be seen from the present simulation results discussed in Section III, in nanoscale transistors, self-heating has a less detrimental effect when compared with larger structures due to the fact that velocity overshoot dominates carrier transport, and there is less exchange of energy between the electron system and the phonon bath [3], [4]. While this result does not mean that one does not have to be concerned with heating in nanoscale devices, it only means that we mainly have to focus on efficient ways of removing the heat from the device active region with, for example, state-of-the-art Peltier coolers. Note that the predictions regarding heating in devices become more complicated with the fact that for channel lengths below 35 nm [5], various nonclassical transistor structures will likely take over due to their delivery of higher performance with lower leakage current than traditional scaled CMOS approaches. New transistors, particularly ultrathin body (UTB) and double-gate MOSFETs, offer paths to further scaling, perhaps to the end of the 2006 International Technology Roadmap for Semiconductors. In UTB silicon-on-insulator (SOI), power consumption is drastically reduced along with leakage current, and the devices show promise for high-performance CMOS, microprocessors, and system-on-a-chip designs. In UTB-SOI structures [6], control of short-channel effects and threshold-voltage (V_t) adjustment can be realized with little or no channel doping. However, an issue that has shown to be important for the SOI devices is lattice heating. Heating effects arise in SOI devices because the device is thermally isolated from the substrate by the buried oxide layer. No simulator can properly predict the electrical characteristics of nanoscale devices if it does not treat electron transport correctly, particularly nonstationary velocity-overshoot effect. In particular, simulators that rely on energy balance models for the electronic transport typically overestimate or underestimate the velocity overshoot due to the improper choice of the energy relaxation times taken from bulk calculations.

In this paper, we solve the Boltzmann transport equation (BTE) for electrons using the ensemble Monte Carlo (EMC) method coupled with moment expansion equations for the phonons, both acoustic and optical. The coupling of electrons and nonequilibrium phonons has been studied for many years and was included, e.g., in EMC simulations to study photoexcited carrier relaxation in quantum wells [7], [8] and more recently by Alam and Lundstrom [9] to simulate laser diodes. However, these models are essentially momentum space models and do not address spatially varying systems such as short-channel transistors. Recently, there have been studies on describing thermal effects in devices that couple the Monte Carlo/Poisson approach to electrothermal modeling [10], [11] in SOI and nitride devices. In that work, a somewhat simplistic model for nonequilibrium phonons is taken, which does not distinguish the acoustic and the optical phonons as separate subsystems.

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In this paper, we solve simultaneously the acoustic and optical phonon energy balance equations and also take into account the coupling of the two subsystems. In addition, we focus here on ultrashort gate-length devices, where nonstationary transport dominates.

II. Problem Specification

It is now generally acknowledged that modeling and simulation are preferred alternatives to trial and error approaches to semiconductor fabrication in the present environment where the cost of process runs and associated mask sets is increasing exponentially with scale [12]. Hence, accurate physical device simulation tools are essential to accurately predict device and circuit performance, and optimize design. At the nanometer scale, there are several effects that have to be accurately captured in the state-of-the-art device simulation tools, including quantum–mechanical effects [13], [14], the effects of random impurities due to unintentional doping [15], and self-consistent modeling of thermal power dissipation and the resulting self-heating and degradation of device performance. The development of simulation tools that incorporate lattice heating self-consistently in the loop is of immediate need for the industry since SOI devices are already in production (thus, one can help in a better and faster design of such structures), and active cooling using Peltier coolers based on heterojunction diodes is receiving increased attention within the scientific and industrial communities. The novelty of the approach that we have undertaken to resolve some of these issues is the fact that we use an EMC device simulator (i.e., the EMC method coupled self-consistently with a 2-D Poisson solver) that is solved self-consistently to the energy transport equations for phonons, treating both the acoustic and optical phonon systems separately, as discussed next in more detail.

To properly treat heating without any approximations made in the problem at hand, one, in principle, has to solve the coupled BTEs for the electron and phonon systems together. More precisely, one has to solve the coupled electron–optical phonons–acoustic phonons–heat bath problem, where each subprocess involves different timescales and has to be addressed in a somewhat individual manner and included in the global picture via a self-consistent loop. We consider the coupled system of semiclassical BTEs for the distribution functions of electrons $f(\mathbf{k},\mathbf{r},t)$ and phonons $g(\mathbf{k},\mathbf{r},t)$

$$\left(\frac{\partial}{\partial t}+\nu_e(k)\cdot\nabla_r+\frac{e}{\hbar}E(r)\cdot\nabla_k\right)f = \sum_q\left\{W_{e,q}^{k+q\to k}+W_{a,-q}^{k+q\to k}-W_{e,-q}^{k\to k+q}-W_{a,q}^{k\to k+q}\right\} \tag{1}$$

$$\left(\frac{\partial}{\partial t}+\nu_p(q)\cdot\nabla_r\right)g = \sum_k\left\{W_{e,q}^{k+q\to k}-W_{a,q}^{k\to k+q}\right\}+\left(\frac{\partial g}{\partial t}\right)_{p-p}. \tag{2}$$

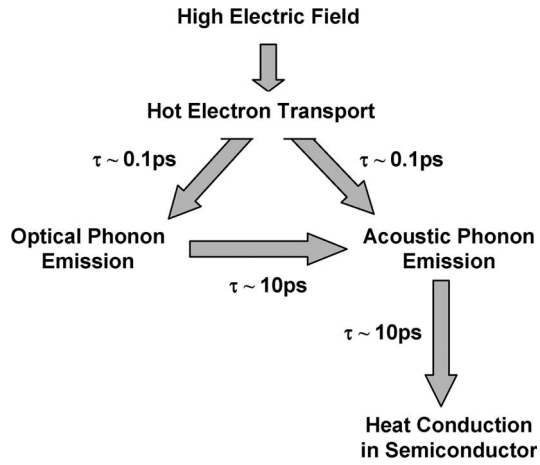

Fig. 1. Most likely path between energy-carrying particles in a semiconductor device is shown together with the corresponding scattering time constants.

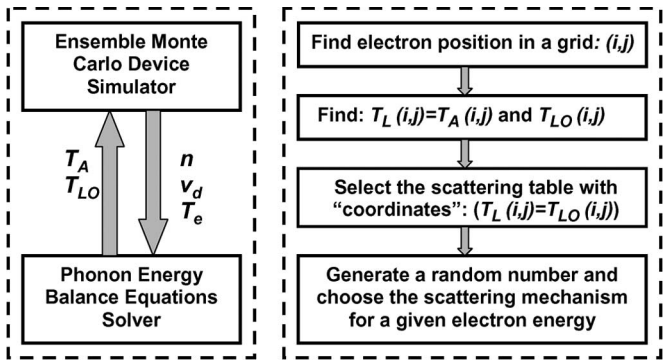

Fig. 2. Left panel: Exchange of variables between the two kernels. Right panel: Choice of the proper scattering table.

Here, $W_{e,q}^{k+q\to k}$ is the probability for electron transition from $k+q$ to k due to the emission of phonon q. Similarly $W_{a,q}^{k+q\to k}$ refers to the processes of absorption. The system is nonlinear, as the probabilities W depend on the product $f\cdot g$ of the electron and phonon distribution functions. The last term on the right-hand side (RHS) of (2) accounts for the phonon–phonon interaction. During the evolution of the system, the electrons gain energy from the electrical field E in the device. The transfer of energy between electrons and phonons is due to the terms W, with a timescale on the order of 0.1 ps (see Fig. 1 above for more details). These terms are common for (1) and (2). Nevertheless, even without the phonon–phonon interaction in (2), the equation set poses a multiscale problem since the left-hand sides involve different timescales; the velocity ν_p of the phonons is two orders of magnitude lower than the velocity ν_e of the electrons. Accordingly, the heat transfer by the lattice is a much slower process than the charge transfer.

Narumanchi *et al.* [16] have reported the full solution of the phonon BTE represented by (2) within the relaxation time approximation, including multiple phonon branches, which are both longitudinal and transverse, for the optical and acoustic modes, and various scattering processes, which are both elastic and inelastic for the phonons. However, to date, such a direct solution to the phonon BTE has not been self-consistently coupled within a spatially varying system to an appropriate

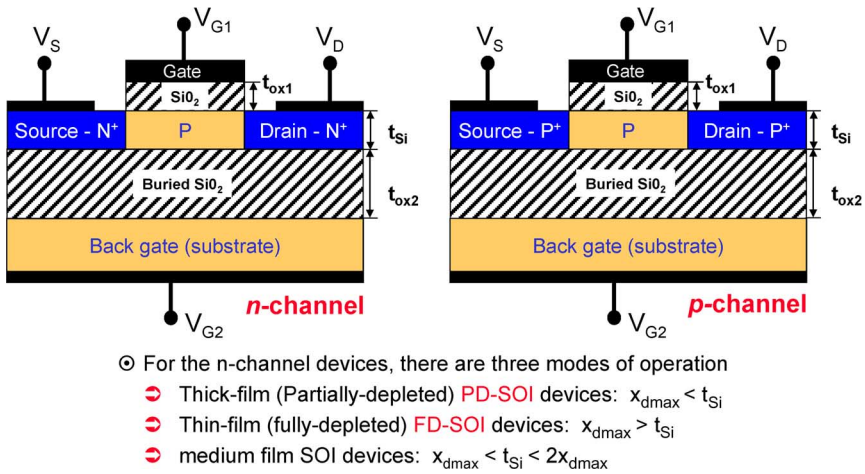

Fig. 3. Basic configuration of n-channel and accumulation mode p-channel SOI devices. x_{dmax} is the maximum depletion layer thickness.

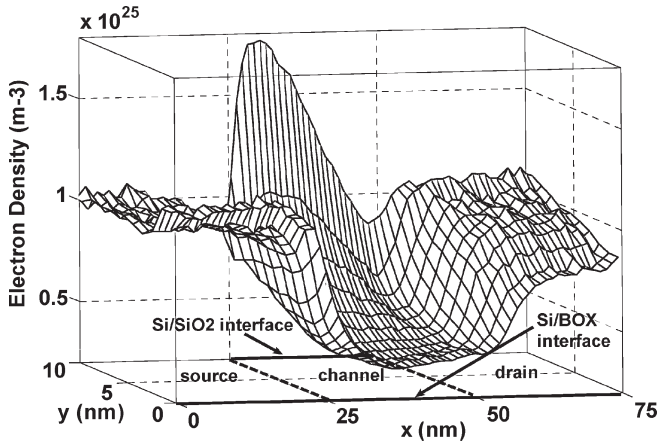

Fig. 4. Sample electron density.

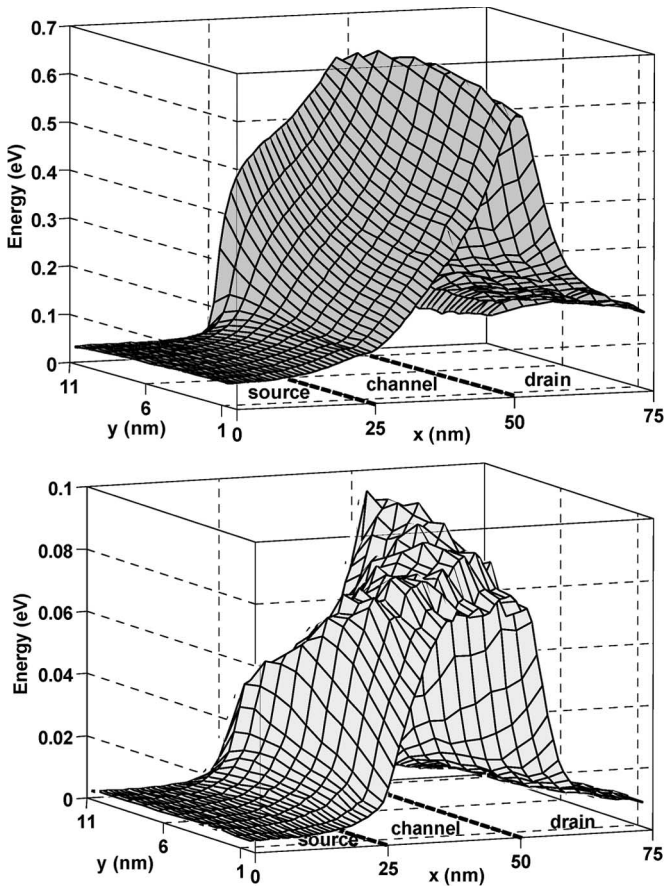

Fig. 5. Top panel: Electron thermal energy. Bottom panel: Electron drift energy.

electron transport model for coupled electrothermal simulation. Therefore, to simplify the calculations to a tractable form, in this paper, we have used a Chapman–Enskog-type expansion [17] to replace the microscopic phonon transport equation by a diffusion problem for the local density and energy of the phonons, where the diffusion coefficients are dependent on the state of the electrons. This method involves computation of the phonon-energy-dependent scattering tables in the EMC code for the electron transport, which already represents a big improvement over the current state of the art, where, as already discussed, the coupling of thermal and charge effects is strictly one way. This approach also takes care of the multiscale nature of the problem, assuming a quasi-steady state; the phonons are in steady state, albeit with a spatially dependent temperature distribution. In this paper, we neglect the effect of the optical phonon dispersion on the tabulated scattering rates. However, Sinha *et al.* [18] have argued that the phonon dispersion for optical phonons should actually be an important effect on the scattering rates within this framework. We have performed simulations of similar device structures as those reported here, including the full optical phonon dispersion, and have found little effect on the simulated current work which will be reported elsewhere [19].

Note that, when considering the electron lattice coupling, the energy transfer from electrons to the high-energy optical phonons is very efficient. However, the optical phonons possess negligible group velocity and, thus, do not participate significantly in the heat diffusion. They instead must transfer their energy to the acoustic phonons, which diffuse heat. The energy transfer between phonons is relatively slow compared with the electron–optical phonon transport, and thus, thermal nonequilibrium may also exist between optical and acoustic

TABLE I
CONTRIBUTION OF DIFFERENT SCATTERING MECHANISMS

Intervalley Scattering:	*Number of events (isothermal)*	*Percent (%) (isothermal)*	*Number of events (thermal)*	Percent (%) (thermal)
acoustic phonon (absorption)	4234	9.38	17425	10.5
acoustic phonon (emission)	7863	17.42	27864	16.8
optical phonon (absorption)	4017	8.9	22202	13.8
optical phonon (emission)	29020	64.3	98408	59.32

phonons. Fig. 1 shows the primary path of thermal energy transport and the associated time constants.

Based on Fig. 1, the primary path of energy transport is represented first by scattering between electrons and optical phonons $(T_{\rm LO})$ and then optical phonons to the lattice (T_A) [20]. The BTE for the two kinds of phonons is then used to provide the energy balance of the process. This means that we have coupled the electron BTE with the equations for the optical and the acoustic energy transfer (that are derived from the phonon BTE) of the form [21]

$$C_{\rm LO}\frac{\partial T_{\rm LO}}{\partial t} = \frac{3nk_B}{2}\left(\frac{T_e - T_{\rm LO}}{\tau_{e-{\rm LO}}}\right) + \frac{nm^*\nu_d^2}{2\tau_{e-{\rm LO}}} - C_{\rm LO}\left(\frac{T_{\rm LO} - T_A}{\tau_{{\rm LO}-A}}\right) \tag{3a}$$

$$C_A\frac{\partial T_A}{\partial t} = \nabla\cdot(k_A\nabla T_A) + C_{\rm LO}\left(\frac{T_{\rm LO} - T_A}{\tau_{{\rm LO}-A}}\right) + \frac{3nk_B}{2}\left(\frac{T_e - T_L}{\tau_{e-L}}\right). \tag{3b}$$

The first two terms in the RHS of (3a) represent the energy gain from the electrons, where n is the electron density, and ν_d is the drift velocity, whereas the last term is the energy loss to the acoustic phonons. The latter appears as a gain term on the RHS of (3b). The first term on the RHS of (3b) accounts for the heat diffusion, and the last term must be excluded if the electron–acoustic phonon interaction is treated as elastic. In this term, the lattice temperature T_L is estimated as equivalent to T_A. Note that proper boundary conditions accounting for the heat sink apply for (3b). $C_{\rm LO}$ and C_A represent the heat capacity of optical and acoustic phonons, respectively, and k_A is the thermal conductivity. In our simulator, the electron temperature T_e is obtained from the EMC time averages. Note that the existing state of the art in this area is a nonself-consistent solver that has been recently developed by Raman *et al.* [22]. This group first solves the hydrodynamic transport model for the electrons to get the electron data, and then, as a postprocessing scheme, the group solves (3) to get the proper lattice temperature distribution.

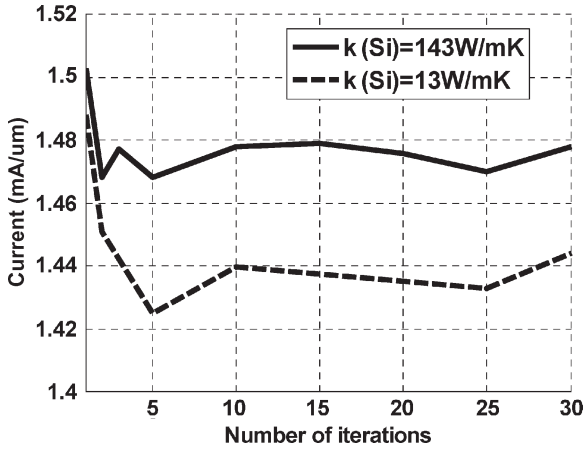

Fig. 6. Current convergence.

In our research effort, the EMC code for the carrier BTE solution [23], [24] has been modified as well. As we have a variable lattice temperature in the hot-spot regions, we have introduced the concept of temperature-dependent scattering tables. For each combination of acoustic and optical phonon temperatures, one energy-dependent scattering table is created. These scattering tables involve additional steps in the MC phase (Fig. 2—right panel) because to randomly choose a scattering mechanism for a given electron energy, it is necessary to find the corresponding scattering table. To do that, first, the electron position on the grid needs to be found in order to know the acoustic and optical phonon temperatures in that grid point, and then, the scattering table with "coordinates" $(T_L, T_{\rm LO})$ is selected. By using current state-of-the-art computers, the precalculation of these scattering tables does not require much CPU time or memory resources and is done once in the initialization stages of the simulation for a range of temperatures. An interpolation scheme is then adopted afterward for temperatures for which we do not have the appropriate scattering table.

To properly connect the particle-based picture of electron transport with continuous "fluidlike" phonon energy balance equations, a space-time averaging and smoothing of electron density, drift velocity, and electron energy are included. At the end of each MC time step, the electrons are assigned to the nearest grid point. Then, the drift velocities and thermal energies are averaged with the number of electrons at the corresponding grid points. After the MC phase, a time averaging of electron density, drift velocity, and thermal energy is done, and the

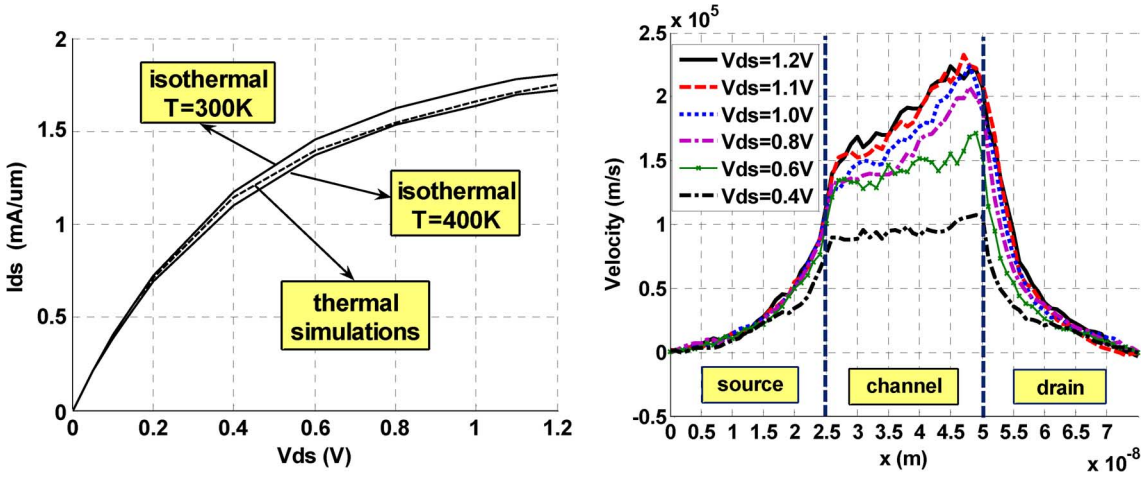

Fig. 7. Left panel: Output characteristics for $V_{\rm gs} = 1.2$ V. Top/middle curve corresponds to the case of excluded/included lattice heating model. Bottom curve is an isothermal simulation but for lattice temperature $T = 400$ K throughout the whole simulation domain. Right panel: Velocity along the channel for $V_{\rm gs} = 1.2$ V and different values of $V_{\rm ds}$. Note that for $V_{\rm ds} > 0.4$ V, electrons are in the velocity-overshoot regime which suggests that lattice heating does not significantly degrade the device characteristics.

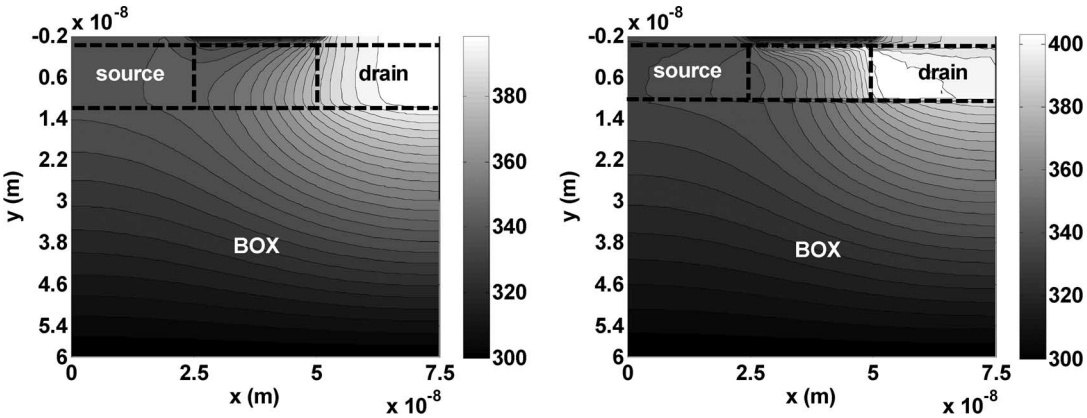

Fig. 8. Left panel: Acoustic phonon temperature for $V_{\rm gs} = 1.2$ and $V_{\rm ds} = 1$ V. Notice the significant heating of the lattice that is equal to the acoustic phonon temperature in our model. Right panel: Optical phonon temperature for $V_{\rm gs} = 1.2$ V and $V_{\rm ds} = 1$ V. Notice the region near the drain with higher optical phonon temperature with respect to the acoustic phonon temperature.

electron temperature distribution is calculated. It is assumed that the drift energy is much smaller than the thermal energy. The smoothing of these variables is necessary because most of the grid points, particularly at the interfaces, are rarely populated with electrons. This leads to very low lattice temperatures in those points. The exchange of variables between electron and phonon solvers is shown on the left panel of Fig. 2.

Because the SOI devices consist of two distinct regions, namely, the silicon device layer and the buried oxide layer (in which the phonons have significantly smaller mean-free paths), the phonon BTE is solved in the silicon layer to accurately model heat transport, but the simpler heat diffusion equation is used in the amorphous BOX because the characteristic length scale of conduction is much smaller than the film thickness. The two distinct computational regions are coupled through interface conditions that account for differences in material properties. For the coupling of the silicon and oxide solution domains, it is necessary to calculate the flux of energy through the interface between the two materials at each point along the interface for every time step.

The boundary conditions used have been chosen based on those typically used in commercial simulators. The Silvaco ATLAS simulation package [25] (THERMAL3D module) states that the only thermal contact should be the substrate. We have performed simulations on our structure to verify this assertion with and without the presence of silicon substrate, and we have concluded that due to the large thermal conductivity of bulk Si, a 300-K boundary condition on the bottom contact maps well into a 300-K boundary condition on the bottom of the BOX. In other words, the presence of the bottom silicon substrate does not affect either the electrical or the thermal characteristics of the structure being considered. In addition, according to the prescriptions given in the Silvaco ATLAS package, the source and drain should be left floating, and the only electrode where one should specify the isothermal boundary conditions is the gate. In fact, in the paper itself, we change the thickness of the gate metal, and the boundary condition at the end of the gate has not much influence on the current degradation. In these simulations, except at the boundary, we treat the metal gate as a material characterized with its own thermal conductivity. Since current nanoscale devices use

metal gates to avoid polysilicon depletion, such an isothermal assumption is also seemingly justified. However, to study the efficacy of the gate as a heat sink, we simulate the effect on the current of several different temperatures for the gate.

III. Heating Effects in FD SOI Devices—Simulation Results

A. Simulator and Role of Velocity Overshoot

The thermal simulator described in Section II has been used in the investigation of the role of heating effects on the electrical characteristics (ON-state current) in different generations of nanoscale fully depleted (FD) SOI devices that are either already in production or will be fabricated in the next five to ten years. Note that this is the first study that is concerned with the electrical aspect of the problem in nanoscale devices. All previous studies have exclusively dealt with the phonon aspect of the problem or have considered larger structures. We consider both standard SiO_2 gate oxide and gate stack $(HfO_2 + SiO_2)$ in the smallest structures being investigated, where high-k dielectrics are going to be used to prevent high OFF-state leakage currents. In our detailed study of the influence of lattice heating on the device thermal characteristics, contrary to common expectations, we find that the degradation of the current decreases with decreasing device gate length due to the more pronounced velocity-overshoot effect in the device characteristics, which results in smaller transit time of the carriers through the active region which, in turn, reduces the probability for interaction with the phonons. This observation is clearly seen from the results presented next. The dimensions of the n-channel FD SOI MOSFET being investigated at present are the following: The channel length is 25 nm; the silicon film width, which is equal to the source/drain junction depth, is 10 nm; the gate-oxide width is 2 nm; the BOX width is 50 nm; the source/drain doping is 1×10^{19} cm^{-3}; and the channel doping is 1×10^{18} cm^{-3}. A generic picture of partially depleted and FD SOI devices is shown in Fig. 3.

To simulate the steady-state state behavior of a device, the system is started in some initial condition, with the desired potential applied to the contacts, and then, the simulation proceeds in a time-stepping manner until steady-state is reached. A common starting point for the initial guess is to start out with charge neutrality, i.e., to assign particles randomly according to the doping profile in the device, so that, initially, the system is charge neutral on the average. After assigning the charges randomly in the device structure, the charge is then assigned to each mesh point using an adequate particle-mesh coupling method, and Poisson's equation is solved. The forces are then interpolated on the grid, and particles are accelerated over the next time step. When the system is driven into a steady-state regime and the MC simulation time has elapsed, we calculate the steady-state current through a specified terminal.

To continue with the thermal part of the simulation, the average electron density, drift velocity, and electron temperature must be calculated on a grid. For the given bias conditions, the average electron density in the channel (Fig. 4) is very high at the Si/SiO_2 interface near the source injection barrier, whereas pinchoff region exists near the drain.

TABLE II
Current Variation With Gate Temperature for 25-nm FD SOI Device Structure With SiO_2 as Gate Oxide

Type of simulation	*Gate Temperature*	Current Decrease
thermal	300K	5.1%
thermal	400K	9.18%
thermal	600K	17.12%

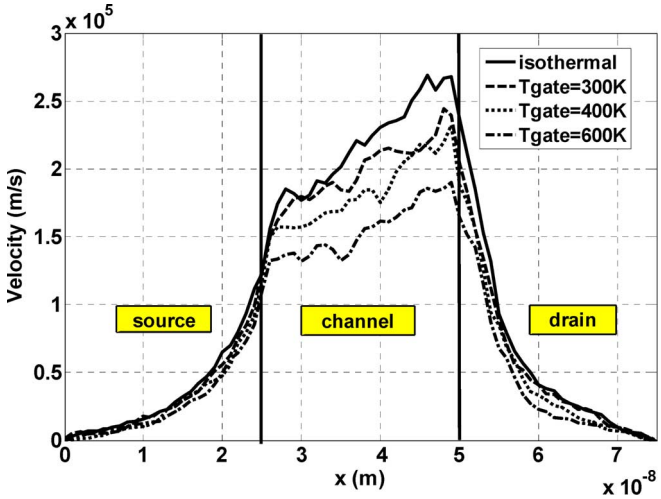

Fig. 9. Velocity along the channel for $V_{gs} = 1.1$ V and $V_{ds} = 1.1$ V for different gate temperatures. Note that the electrons are in the velocity-overshoot regime.

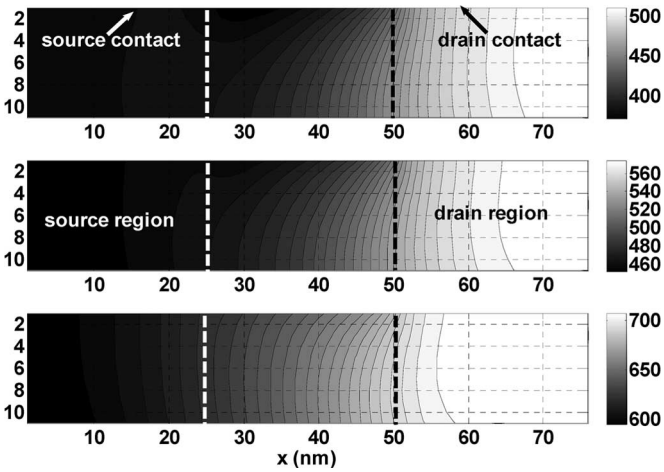

Fig. 10. Lattice temperature profiles in the silicon layer in a 25-nm gate-length FD SOI MOSFET for $V_{gs} = 1.1$ V and $V_{ds} = 1.1$ V and different gate-electrode temperatures (300 K, 400 K, and 600 K from up to down). SiO_2 is used as a gate oxide.

The two components of the electron kinetic energy are shown in Fig. 5. They show that the thermal part of electron kinetic energy is much larger than the drift part; thus, electron temperature can be calculated from the thermal energy.

Finally, the acoustic and optical phonon temperatures are calculated with the phonon energy balance equation solver. During the simulation, the gate contact and the bottom of the BOX are set to 300 K, whereas Neumann boundary conditions for the heat transfer are used in all other outer surfaces. In addition, the tolerance used in the "thermal" successive over

TABLE III
CURRENT DECREASE WITH GATE TEMPERATURE FOR 25-nm FD SOI DEVICES STRUCTURE WITH HfO_2 GATE STACK

Gate temperature	*Zero Metal Gate Electrode Thickness*	Gate Electrode Thickness (The boundary condition for the temperature is at the end of the metal gate, which means that the thermal simulator also solves the metal region)			
		3 nm	5 nm	7 nm	40 nm
300K	10.5%	10.54%	11.22%	11.16%	10.62%
400K	13.81%	13.86%	13.98%	13.72%	13.34%
500K	17.13%	16.92%	17.33%	17.23%	17.27%

relaxation algorithm is equal to 0.001, which leads to a very fast convergence.

When the simulation starts, all variables obtained from the first iteration of the EMC solver are calculated by using a uniform distribution for the acoustic and optical phonon temperatures. This means that only one scattering table is used for all electrons no matter where they are located in the device. When the phonon temperatures are computed from the phonon energy balance equations, they are "returned" at the beginning of the MC free-flight–scattering phase. Now, for each mesh point, we have a scattering table that corresponds to the acoustic and optical phonon temperatures at that point. In this case, the electron position defines which scattering table is "valid," and then, by generating a random number, the scattering mechanism is chosen for the given electron energy. The impact of the phonon-temperature-dependent scattering tables can be demonstrated by counting the number of energy-exchange electron–phonon scattering events. From Table I, it could be concluded that the inclusion of the phonon-temperature-dependent scattering table increases the number of electron–phonon interactions.

The outer Gummel loop between the MC solver and the phonon energy balance solver ends when the steady-state conditions for the phonon temperatures and the device current are reached. To test the overall convergence of the coupled thermal and EMC codes, we registered the variations of the drain current with the number of thermal iterations for the given bias conditions. The results of these simulations (see Fig. 6) show that only three to five thermal iterations are necessary to obtain the steady-state solution of the current. In addition, we find that, when thermal simulations are self-consistently coupled with EMC code, a smaller number of time steps are needed to obtain a steady-state condition in the EMC phase. For example, to get equal slopes from the cumulative source and drain charge time characteristics, the simulation time for isothermal EMC code should be at least 8 ps, whereas 2.5-ps simulation time for Monte Carlo poisson solver (MCPS) phase is enough to reach steady state when thermal simulations are included.

The left panel of Fig. 7 shows the effect of lattice heating on the I–V characteristics of a 25-nm gate-length FD SOI structure. The velocity overshoot is clearly seen on the right panel of Fig. 7. For this particular device structure, the corresponding degradation of device characteristics due to thermal effects is relatively small, i.e., less than 10%. As shown from the temperature maps of acoustic and optical phonons in Fig. 8, the maximum rise in the lattice temperature is on the order of 100 °C on the drain side of the gate as expected. For comparison, we also compare in Fig. 7 the effect of an elevated lattice temperature of 400 K assuming an isothermal model compared with the nonuniform model, which shows that most of the effect observed in the I–V is due to lattice heating.

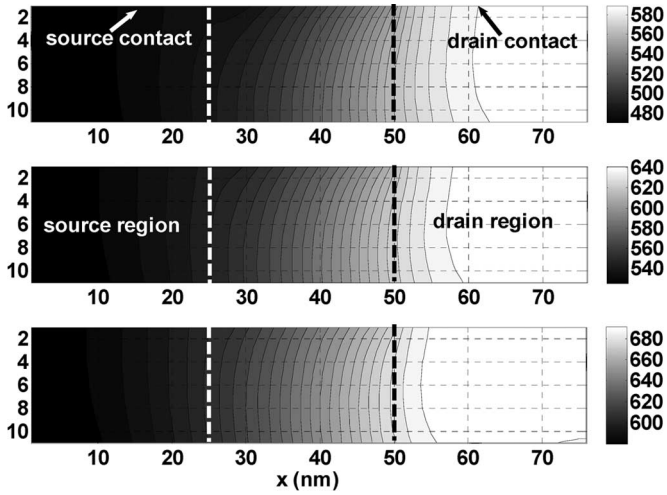

Fig. 11. Lattice temperature profiles in the silicon layer in a 25-nm gate-length FD SOI MOSFET for $V_{gs} = 1.1$ V and $V_{ds} = 1.1$ V and different gate temperatures (300 K, 400 K, and 500 K from up to down). Gate stack (SiO_2 and HfO_2) is used.

B. Influence of the Boundary Condition on the Gate Electrode on the On-Current

To properly solve the phonon balance equations, the device should be attached to a heat sink somewhere along the boundary, or a finite heat conduction through the surface should be allowed. In our code, a heat sink is modeled by a simple Dirichlet boundary condition (i.e., constant temperature). We use the gate-electrode contact and the bottom of the BOX as heat sinks. Table II gives the percentage of the current decrease due to the heating effects with the variation of gate-electrode temperature. The calculated results show that the current degradation is more prominent for higher gate temperatures. When the temperature of the bottom of the BOX was set to the same values as given in Table II, the current degradation was around 1%; thus, in all other simulations, the temperature of the bottom of the BOX was set to 300 K.

Fig. 9 shows the velocity profile along the channel for the same bias conditions ($V_{gs} = V_{ds} = 1.1$ V) and different gate temperatures, where, as can be seen, the velocity in the channel decreases with the increase of the gate temperature, but the carriers in the channel are still in the velocity-overshoot regime. As shown from the temperature maps of acoustic phonons in

TABLE IV
GEOMETRICAL DIMENSIONS OF THE SIMULATED FD SOI MOSFETS

Gate Length L_{gate} *(nm)*	*Oxide Thickness* t_{OX} *(nm)*	*Source/Drain Length* $L_{S/D}=L_{gate}$ *(nm)*	*Silicon Layer Thickness* $t_{si}=0.4L_{gate}$ *(nm)*	*BOX Thickness* t_{BOX} *(nm)*	*Source/Drain Doping Concentration* N_D (m^{-3})	Channel Doping Concentration N_A (m^{-3})
25	2	25	10	50	1×10^{25}	1×10^{24}
45	2	45	18	60	1×10^{25}	1×10^{24}
60	2	60	24	80	1×10^{25}	1×10^{24}
80	2	80	32	100	1×10^{25}	1×10^{23}
90	2	90	36	120	1×10^{25}	1×10^{23}
100	2	100	40	140	1×10^{25}	1×10^{23}
120	3	120	48	160	1×10^{25}	1×10^{23}
140	3	140	56	180	1×10^{25}	1×10^{23}
180	3	180	72	200	1×10^{25}	1×10^{23}

TABLE V
CURRENT DECREASE WITH GATE TEMPERATURE FOR DIFFERENT FD SOI TECHNOLOGIES

Type of simulation	*Gate Electrode Temperature (K)*	*25 nm FD SOI nMOSFET Vgs=Vds=1.2V*		*45 nm FD SOI nMOSFET Vgs=Vds=1.2V*		*60 nm FD SOI nMOSFET Vgs=Vds=1.2V*	
		Current (mA/um)	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**
isothermal	**300**	**1.929**	\	**1.5645**	\	**1.2457**	\
thermal	**300**	**1.8176**	**5.78**	**1.4717**	**5.93**	**1.1885**	**4.73**
thermal	**400**	**1.7467**	**9.45**	**1.3957**	**10.79**	**1.1124**	**10.83**
thermal	**600**	**1.5997**	**17.1**	**1.2612**	**19.39**	**0.9882**	**20.79**

Type of simulation	*Gate Electrode Temperature (K)*	*80 nm FD SOI nMOSFET Vgs=Vds=1.5V*		*90 nm FD SOI nMOSFET Vgs=Vds=1.5V*		*100 nm FD SOI nMOSFET Vgs=Vds=1.5V*	
		Current (mA/um)	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**
isothermal	**300**	**1.7810**	\	**1.6671**	\	**1.5743**	\
thermal	**300**	**1.5850**	**11**	**1.4805**	**11.19**	**1.4004**	**11.05**
thermal	**400**	**1.4612**	**17.96**	**1.3678**	**17.95**	**1.2833**	**18.48**
thermal	**600**	**1.2571**	**29.42**	**1.1784**	**29.31**	**1.1158**	**29.12**

Type of simulation	*Gate Electrode Temperature (K)*	*120 nm FD SOI nMOSFET Vgs=Vds=1.8V*		*140 nm FD SOI nMOSFET Vgs=Vds=1.8V*		*180 nm FD SOI nMOSFET Vgs=Vds=1.8V*	
		Current (mA/um)	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**	**Current (mA/um)**	**Current Decrease (%)**
isothermal	**300**	**1.3657**	\	**1.2341**	\	**1.0321**	\
thermal	**300**	**1.1439**	**16.34**	**1.0416**	**15.6**	**0.8570**	**15.22**
thermal	**400**	**1.0630**	**22.16**	**0.9654**	**21.85**	**0.8100**	**21.52**
thermal	**600**	**0.9256**	**32.22**	**0.8311**	**32.27**	**0.6940**	**32.76**

Fig. 10, the lattice temperature in the source, the channel, and the drain region is increasing with the increase of the gate-electrode temperature, which means that the increased lattice temperature has a larger impact on the decrease of the carrier velocity in the channel.

C. Thermal Degradation in High-k Devices

To further investigate the influence of the gate temperature on the current decrease due to the self-heating, instead of SiO_2 as gate oxide, we used a gate stack (SiO_2 and HfO_2) and a copper metal gate with a finite thickness for the same 25-nm FD SOI structure. In order to compare the results of these two device structures, the gate stack thickness was calculated in such a manner that the surface potential for $V_{\rm gs} = 1.1$ V and $V_{\rm ds} = 0$ is the same for both. The results of the thermal simulations for the FD SOI structure with gate stack are tabulated in Table III. When the gate electrode is modeled with zero thickness, the current decrease due to the thermal effects is 5% more when we use a gate stack instead of a SiO_2 gate oxide. From Table III, one can also note that the details of gate-electrode thickness modeling have little effect on the simulated current degradation. The lattice temperature profile in the silicon layer for different gate temperatures, with 40-nm gate-electrode thickness, is shown in Fig. 11. As can be seen from the results shown in this figure, the lattice temperature is increased due to the gate stack

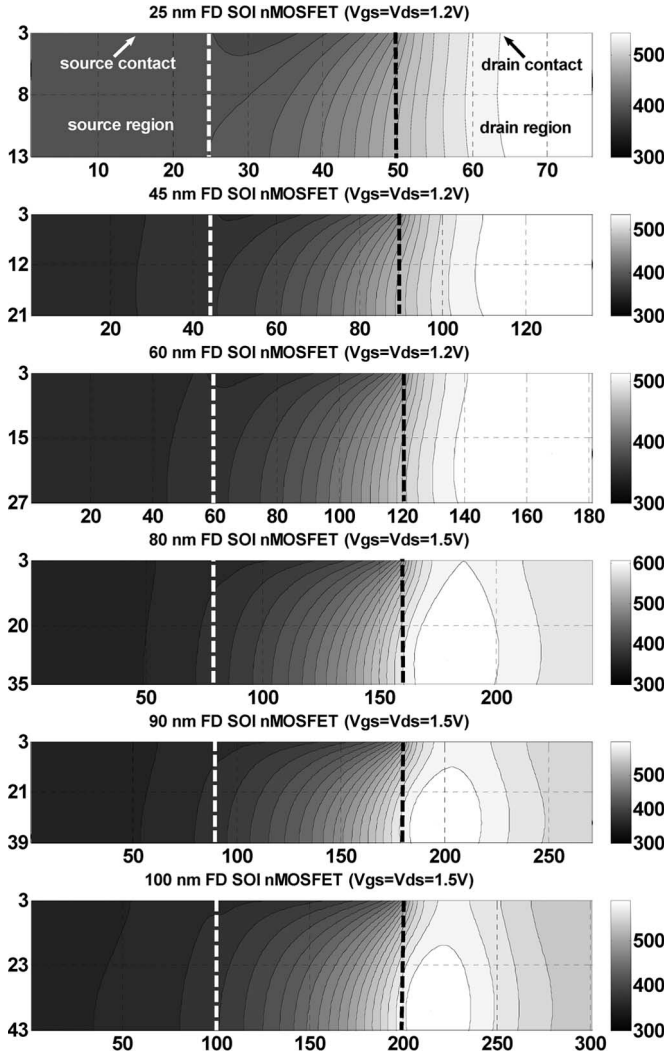

Fig. 12. Lattice temperature profiles in the silicon layer for FD SOI MOSFETs from Table IV with a gate temperature set to 300 K (top: 25 nm; bottom: 100 nm).

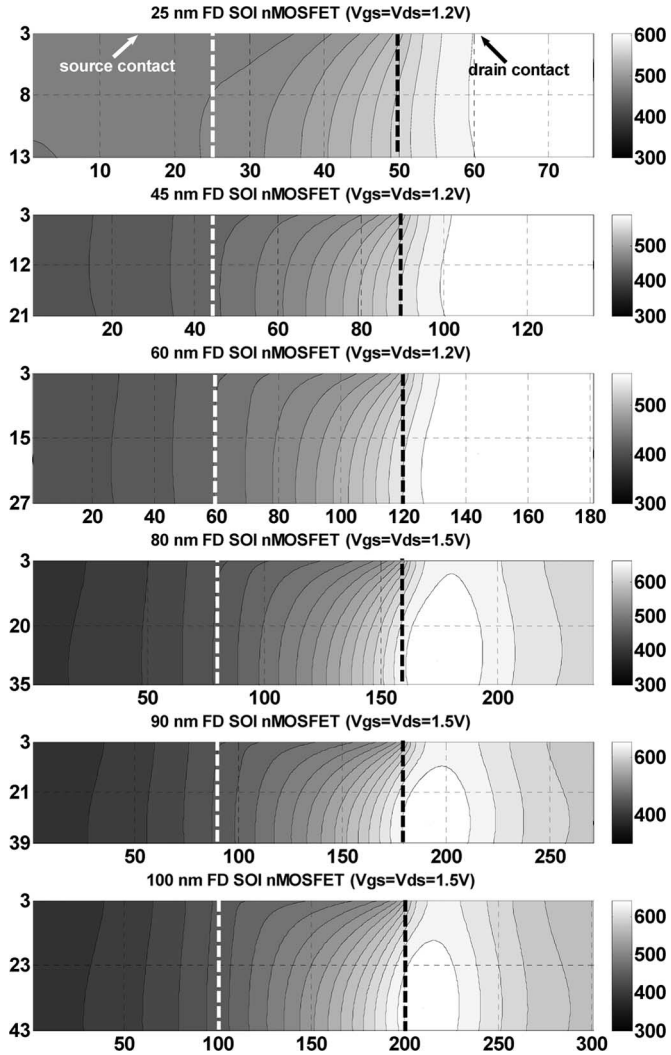

Fig. 13. Lattice temperature profile in a silicon layer for different device geometries of FD SOI MOSFET when the gate temperature is set to 400 K.

compared with the corresponding lattice temperature profile in Fig. 10.

D. Thermal Degradation With Scaling of Device Geometry

In addition to the previously noted observation regarding the influence of the velocity overshoot, we modeled larger FD SOI device structures, and we also investigated the influence of the temperature boundary condition on the gate electrode on the current degradation due to heating effects. The geometrical dimensions of the simulated FD SOI MOSFETs are given in Table IV, whereas Table V gives the percentage of the current decrease due to the heating effects with the variation of the gate-electrode temperature for the device structures being considered. The calculated results show that the current degradation is more prominent for larger devices and for higher gate temperatures. For 80-nm and larger devices, simulated carriers are not in the velocity-overshoot regime in the larger portion of the channel (particularly near the source end of the channel). Snapshots of the lattice temperature profiles in the silicon layer for these devices when the gate temperature is set to 300 K are shown in Fig. 12. From these snapshots, one can observe the following: 1) The temperature in the channel is increasing with the increase of the channel length, and 2) the maximum lattice temperature region (hot spot) is in the drain, and it shifts toward the channel for larger devices. This behavior is more drastic for higher gate temperatures (see Fig. 13).

Fig. 14 shows the ensemble averaged lattice and optical phonon temperatures along the channel in the silicon layer only for three technologies of devices being considered (25, 80, and 180 nm). Note that there is a bottleneck between the lattice and the optical phonon temperature in the channel which is more pronounced for shorter devices, which is due to the fact that the energy transfer between the optical and acoustic phonons is relatively slow compared with the electron–optical phonon processes and the fact that the electrons are in the velocity overshoot (and since the channel is very short, they spent little time in the channel). To better understand the phonon temperature bottleneck, different cross sections (at Si/SiO_2 interface, at half Si-layer width, and at Si/BOX interface) of the lattice and the optical phonon temperature profiles in the channel direction were investigated as well. We find that the

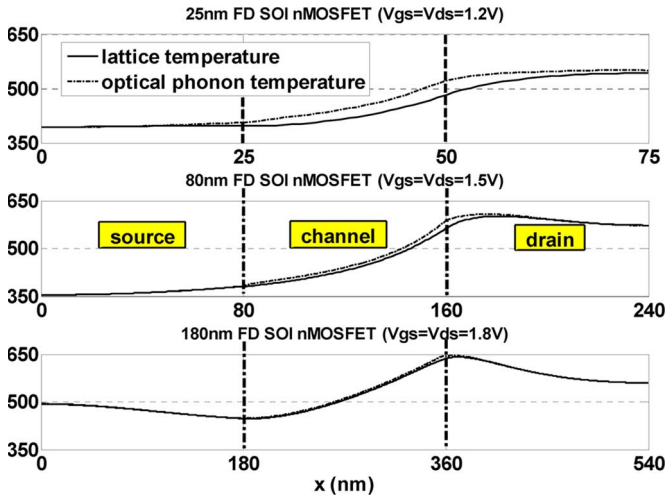

Fig. 14. (Full) Averaged lattice and (dashed) optical phonon temperature profiles in the channel direction in the silicon layer for (top) 25-nm, (middle) 80-nm, and (bottom) 180-nm FD SOI n-channel MOSFETs with a gate temperature set to 300 K.

bottleneck is decreasing from the Si/SiO_2 interface to the Si/BOX interface. For shorter devices, it exists in the whole channel region, which is not the case for longer devices (thicker Si layer and longer channel length). From the results we have presented here, one can conclude that the higher the temperature in the channel and/or the longer the electrons in the channel, the larger the degradation of the device electrical characteristics is due to the heating effects.

IV. Conclusion

A self-consistently coupled thermal/EMC device simulator has been developed and applied to the study of FD SOI devices. We show that the pronounced velocity overshoot present in the nanometer-scale device structure considered in this paper minimizes the degradation of the device characteristics due to lattice heating. This observation was also justified with SILVACO Atlas simulations which demonstrated that for larger energy relaxation times, which correspond to the case of more pronounced velocity overshoot, current degradation in the ON-state due to thermal effects is on the order of 10%, not to 30%, as found in larger device structures in which the velocity overshoot does not play a significant role.

We also investigate the influence of the gate temperature on the amount of current degradation due to the heating effects. Namely, we used the gate contact as a heat sink to properly solve the phonon balance equations. As can be seen from the temperature maps of acoustic phonons presented in this paper, the lattice temperature in the source, channel, and drain region is increasing with the increase of the gate temperature, which means that the increased lattice temperature has a larger impact on the decrease of the carrier velocity in the channel. To further investigate the influence of the gate temperature on the current decrease due to the heating effects, instead of the gate oxide, we used a gate stack (SiO_2 and HfO_2) and a copper metal gate with finite thickness for the same 25-nm FD SOI structure. When the gate is not modeled, the current decrease due to the thermal effects is 5% more when a gate stack and then a gate oxide are used. In addition, the lattice temperature is increased due to the gate stack compared with the corresponding lattice temperature profile when using silicon dioxide. When examining heating in different device technologies, we observed a bottleneck between the lattice and the optical phonon temperature in the channel which is more pronounced for shorter devices, which is due to the fact that the energy transfer between optical and acoustic phonons is relatively slow compared with the electron–optical phonon processes and the fact that the electrons are in the velocity overshoot (and since the channel is very short, they spent little time in the channel). To better understand the phonon temperature bottleneck, different cross sections of the lattice and the optical phonon temperature profiles in the channel direction were investigated. Briefly, we find that the bottleneck is decreasing from the Si/SiO_2 interface to the Si/BOX interface. For shorter devices, it exists in the whole channel region, which is not the case for longer devices (thicker Si layer and longer channel length). From the results we have presented here and those we have published earlier, one can conclude that the higher the temperature in the channel and/or the longer the electrons in the channel, the larger the degradation of the device electrical characteristics is due to the heating effects.

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