A Rigorous Model for Trapping and Detrapping in Thin Gate Dielectrics

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Abstract- **We rigorously model charge trapping and detrapping in ultrathin dielectrics. In addition to charge exchange with the substrate, the poly-gate interface is taken into account which gives rise to decreased charge trapping compared to conventional models designed for thicker gate dielectrics. Finally, an extension of this model also accounting for the shift of trap levels may possibly explain the large time scales experimentally observed during the recovery after application of an on-state voltage.**

I. INTRODUCTION

The success of semiconductor industry relies on continuously shrinking device dimensions which is accompanied by the emergence of quantum mechanical effects such as tunneling and trapping. Meanwhile research in this field encounters a point where these effects become increasingly important as it is the case for Hot Carrier Injection (HCI) and Stress-Induced Leakage Current (SILC) among others.

Even though considerable progress in oxide reliability has been made, the presence of traps in dielectric such as silicon oxynitrides and hafnium dioxide is experimentally confirmed by a series of measurement techniques. In particular Electron-Paramagnetic-Resonance (EPR) allows the identification of a large number of defects. Several variants of the E'_γ center have been detected in silicon dioxide [1], while especially K centers in silicon oxynitrides have been discovered [2]. Some of these traps are suspected to be charge traps, however, their nature is not fully understood and no comprehensive model for charge trapping exists to date. It is well established that the trap behavior strongly depends on the spatial and energetical distribution of traps within the dielectric. Various sorts of traps have been proposed in literature, however, detailed knowledge is still vague. Zhang [3], for instance, proposed two types of traps: Cycling Positive Charges (CPC) which show an oscillating behavior for switching bias - in contrast to the so-called Anti-Neutralization Positive Charges (ANPC) which form a constant background charge. Annealing studies undertaken on irradiated samples reveal accelerated annealing behavior of traps at elevated temperatures [4]. Furthermore, traps featuring more than only two charge states, the so-called amphoteric traps, have been proposed in [5]. In short, several distinct properties for different sorts of traps may have to be taken into account when dealing with trapping in dielectrics.

An issue which has attracted some recent attention is the idea that charge trapping is suggested to be involved in Negative Bias Temperature Instability (NBTI). In literature, two kinds of explanations for NBTI are persued: First, the NBTI phenomenon is traced back to the creation and passivation of dangling bonds correlated to diffusion of hydrogen to and from the interface. Second, trapping and detrapping of charge carriers into the gate dielectric is regarded as the origin of NBTI or supposed to constitute an appreciable contribution to NBTI [6,7]. Tewksbury's trapping model [8] which addresses this issue in considerable detail has been used in this context [7]. However, our simulations extended by the impact of the gate contact indicate short storage times for trapped charges in thin dielectrics. This is in stark contrast to observations in experiments. As one possible explanation for these long storage times the impact of energy level shifts are investigated. They occur, when traps capture charge carriers followed by reformation of the trap and a shift of the corresponding trap level. Such shifts have been suggested in a speculative manner [3] and as a result of first principles calculations [9]. In this work, the focus is put on investigating the impact of level shifts in addition to charge trapping from the poly-gate interface. A rigorous model is suggested which incorporates the poly-gate interface as well as such level shifts.

II. THEORETICAL BACKGROUND

In the following, a brief overview of the models employed in this study is given. The present description of trapping and detrapping extends the approach followed by Tewksbury [8] - termed the fixed level model throughout this study - by allowing for charge injection from the poly-gate interface and incorporating trap level shifts. The rate equation (1) forms the basis of the fixed level model:

$$\begin{aligned}\partial_t f_t(E_t,x) = \;& n(E_t) r_{in}(E_t,x)(1-f_t(E_t,x)) \\ & - p(E_t) r_{in}(E_t,x) f_t(E_t,x)\end{aligned} \tag{1}$$

where $n(E_t)$ or $p(E_t)$ denote the number of occupied or empty states in the substrate and f_t stands for the occupancy of the traps located within the dielectric at a distance x from the substrate interface. Note that all quantities are evaluated at the same trap energy E_t. A derivation of the rates r_{in} and r_{out} based on Fermi's golden rule yields a WKB coefficient multiplied with a prefactor ν_0:

$$\begin{aligned} r_{in/out} &= \nu_0 \exp(-2\int_{x_{if}}^{x_t} k \cdot x dx) \\ k^2 &= \tfrac{2m}{\hbar^2}(E_{c/v} - E), \end{aligned} \tag{2}$$

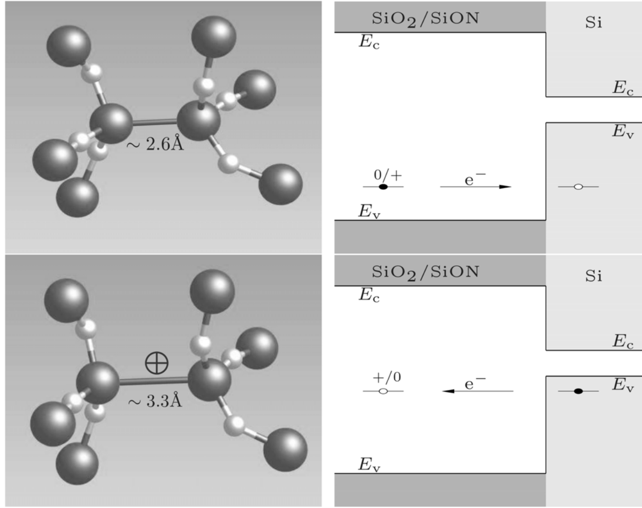

Fig. 1. Representation of a E'$_\delta$ [10] defect and its defect levels within the silicon dioxide bandgap. When a positive charge is introduced into this defect, the bond length increases, giving rise to a shift of the trap level upwards in the energy scale.

where x_t is the position of the trap, x_{if} the position of the interface. $E_{c/v}$ stands for the conduction or the valence band edge, respectively. Interface states may also be included in $n(E_t)$ and $p(E_t)$ but have to be specified by different prefactors due to their distinct nature compared to band states. The fixed level model, which was designed for thick gate dielectrics, neglects charge injection from the poly-gate interface - a shortcoming which has to be overcome for modeling modern semiconductor devices. This can be remedied by introducing additional rates on the right hand side of equation (3).

$$\begin{aligned} \partial_t f_t(E_t,x) = \quad & n_s(E_t) r_{in}(E_t,x)(1-f_t(E_t,x)) \\ & - p_s(E_t) r_{in}(E_t,x) f_t(E_t,x) \\ & n_g(E_t) r_{in}(E_t,x)(1-f_t(E_t,x)) \\ & - p_g(E_t) r_{in}(E_t,x) f_t(E_t,x), \end{aligned} \tag{3}$$

where the subscript s stands for substrate quantities and g refers to poly-gate quantities. This refined model is also referred to as the extended fixed level model in the following.

Up to this point, it is assumed that energy levels do not depend on the charge state of the defect. This assumption has been proven to be unjustified. In fact, level shifts do occur after defects have been occupied by charge carriers. When a trapping process takes place, the defect configuration [9] rearranges itself and alters the nearby bond lengths (see Fig. 1), particularly in the amorphous layers used as dielectrics. This is combined with a change in the electrostatics due to the introduced charge. Both effects together cause a trap level shift which has been confirmed for a series of investigated defects suspected to be oxide traps [10,11]. In our level shift model, these level shifts are considered by introducing two types of energy levels, namely one for e^- capture (E_{in}) and another for e^- release (E_{out}):

$$\begin{aligned} \partial_t f_t(E_t,x) = \quad & n(E_{in}) r_{in}(E_{in},x)(1-f_t(E_{in},x)) \\ & - p(E_{out}) r_{in}(E_{out},x) f_t(E_{out},x) \end{aligned} \tag{4}$$

Table I

VALUES USED FOR THE FIXED LEVEL MODEL WITH A NARROW TRAP DISTRIBUTION. THE TRAP LEVELS ARE RELATIVE TO THE CONDUCTION BAND EDGE OF SiO_2. $v_{0,if}$ AND $v_{0,band}$ RELATE TO THE PREFACTOR USED FOR TRAPPING FROM INTERFACE WITHIN THE BANDGAP OR FROM THE BANDS, RESPECTIVELY. SINCE THE THE DISTRIBUTION OF TRAP LEVELS IS ASSUMED TO BE UNIFORM, $\Delta_{IN/OUT}$ RANGES FROM THE TOPMOST TO THE LOWERMOST TRAP LEVEL. m_t AND m_e DENOTES THE TUNNELING MASS AND THE ELECTRON MASS, RESPECTIVELY.

N_t	$3\cdot10^{18}$ cm^{-3}
E_{in}	-4.8 eV
Δ_{in}	0.2 eV
E_{out}	-4.8 eV
Δ_{out}	0.2 eV
$v_{0,if}$	$6.3\cdot10^{-1}$ s^{-1} cm^2 eV
$v_{0,band}$	$6.3\cdot10^{-12}$ s^{-1} cm^3 eV
m_t	$0.5\cdot m_e$

Table II

VALUES USED FOR THE FIXED LEVEL MODEL WITH A BROAD TRAP DISTRIBUTION.

N_t	$3\cdot10^{18}$ cm^{-3}
E_{in}	-4.8 eV
Δ_{in}	1.6 eV
E_{out}	-4.8 eV
Δ_{out}	1.6 eV
$v_{0,if}$	$6.3\cdot10^{-1}$ s^{-1} cm^2 eV
$v_{0,band}$	$6.3\cdot10^{-12}$ s^{-1} cm^3 eV
m_t	$0.5\cdot m_e$

where the level shift Δ is given by

$$\Delta = E_{in} - E_{out} \tag{5}$$

Solving these differential equations for each trap delivers trap occupancies which can finally be mapped to a measureable threshold voltage shift by making use of

$$\Delta V_{th} = \frac{q_0}{C_{ox}} \int_0^{t_{ox}} (1 - \frac{x}{t_{ox}}) \rho_t \Delta f_t(E_t,x) dx, \tag{6}$$

where C_{ox} denotes the capacitance of the dielectric, t_{ox} the thickness of the dielectric, and $\Delta f_t(E_t,x)$ the change in the trap occupancy.

In the following, a comparison between the individual models will be undertaken, thereby highlighting the differences observed in the timescales for the fixed level model and the level shift model. Numerical simulations based on the evaluation of the rate equations are performed coupled to a Poisson solver assuming Boltzmann statistics for the carrier concentrations [12].

III. THE FIXED LEVEL MODEL

Tewksbury's description of charge trapping is restricted to charge injection from the substrate and ignores the presence of the poly-gate interface as a source/sink of charge carriers. Recall that this assumption loses its justification when the gate dielectric shrinks into the nanometer range. At first, the fixed level model is recapitulated and on its basis the impact of the poly-gate interface will be discussed. Numerical simulations are performed on a pMOSFET with a 3 nm thick silicon dioxide

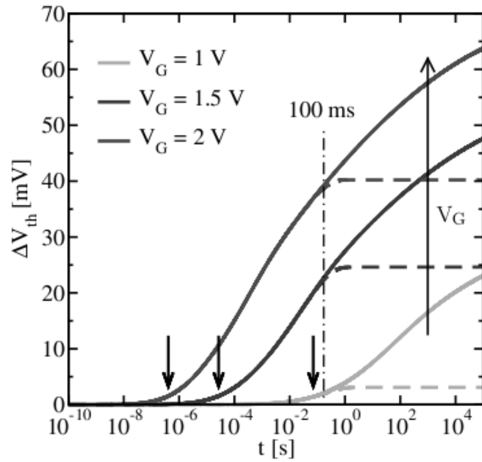

Fig. 2. Fixed level model: Time evolution of the threshold voltage during the on-state phase for different gate voltages. The solid lines denote charge trapping curves according to the conventional fixed level model, while the dashed lines belong to the extension of this model with a poly-gate interface. Within the extended fixed level model, only traps near the substrate interface (with short tunneling time constants) are capable of capturing h^+. This reflects in an early saturation (indicated by the vertical arrows) during the on-state for the conventional fixed level model. The vertical line shows the beginning of the extended saturation behavior for all three gate voltages at approximately 100 ms.

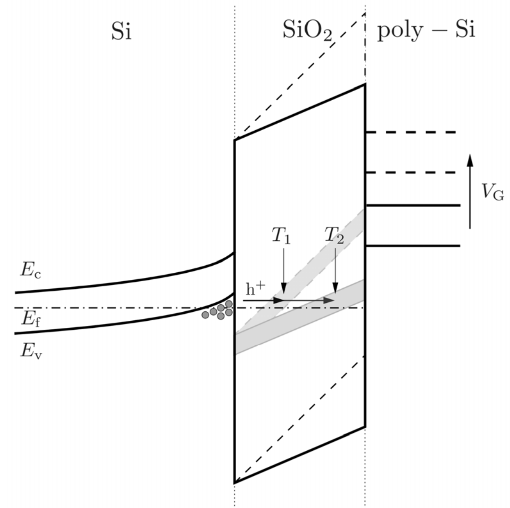

Fig. 4. Schematic of the band diagram for 2 different voltages. The crossing point between the Fermi level and the band of trap levels (grey regions) is linked to the earliest trapping events (T_1 and T_2) giving rise to the beginning of charge trapping. When the gate bias is increased, the crossing point is shifted closer to the substrate interface where traps with smaller tunneling time constants are situated. This leads to more earlier onset of charge trapping in T_1 compared to T_2, where the latter one corresponds to a higher gate voltage.

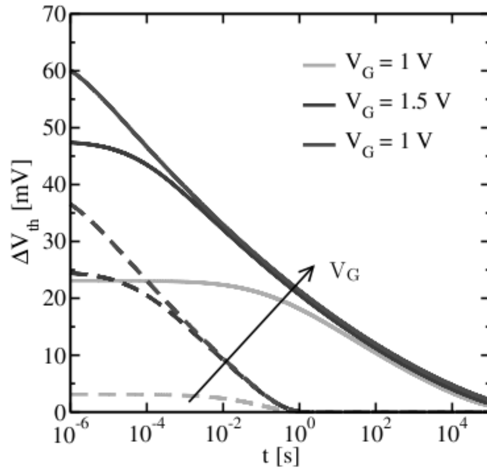

Fig. 3. The same as in Fig. 2 but for the off-state. Within the extended fixed level model, only traps with small tunneling times participate in charge trapping which is reflected in an early erase of trapped charges. They cause a slow decay of the threshold voltage shift during the off-state. In the case of the conventional fixed level model, also traps charged with long tunneling times are involved in detrapping again which results in slow decay in the V_{th}.

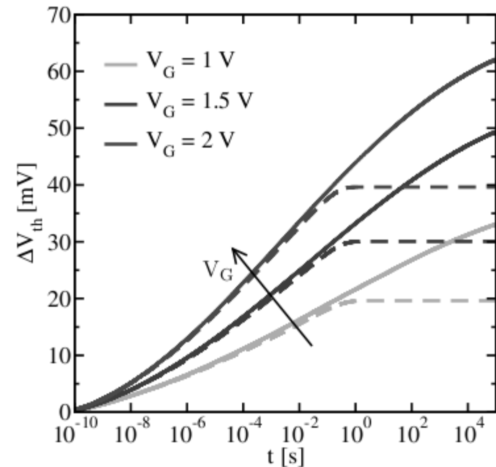

Fig. 5. The same as in Fig. 2 but for a wide spread of trap levels according to Table II. The onset of charge trapping occurs at the same time point which lies outside the measurable timescales. The different voltages are reflected in the different slopes of the curves.

layer and an n-poly-gate. The defect density N_t is assumed to amount to approximately $3 \cdot 10^{18}$ cm^{-3}. The corresponding trap level is placed 0.55 eV below the substrate valence band edge with an uniform spread of 0.1 eV. Used quantities are listed in Table I. The first on-state phase is preceded by an equilibrium simulation. The off-phase directly continues after the end of the on-phase. For a proper analysis the tunneling time constants measured for thick oxides in [8] are converted into the respective v_0 applied for the present simulations.

In the conventional fixed level model, the e^- capture level coincides with the h^+ capture level. Hence, the high h^+ concentration in the valence band favors h^+ emission into traps at energies close to and above the Fermi energy. The decay of the h^+ concentration in energy scale, however, suppresses their capture in traps far below the Fermi level. The dependence of the WKB coefficient on the spatial depth of traps gives rise to increasing tunneling time constants from the substrate. At the beginning of the on-state, the negative gate bias decreases the Fermi level accompanied by a strong increase in the h^+ concentration and consequently the onset of h^+ trapping. Then the trapped h^+ front penetrates into the gate dielectric with increasing time. The return to the off-state triggers the temporal refilling of traps which again proceeds from the substrate

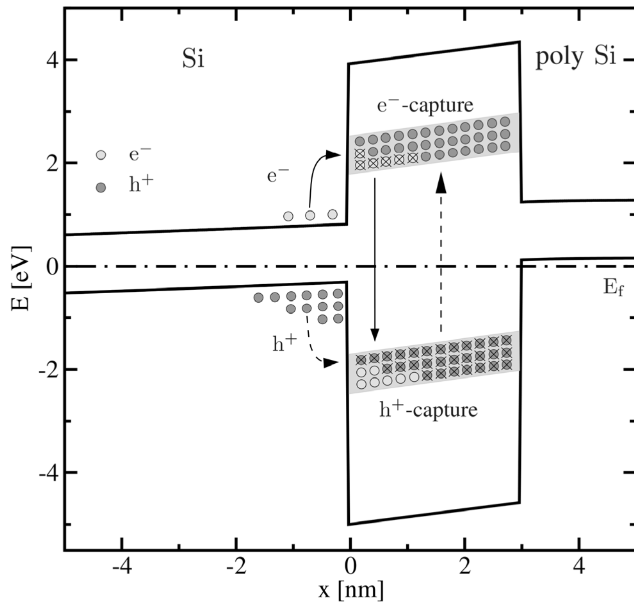

Fig. 6. Schematic band diagram including trap levels. The upper trap level indicated by the grey box enables only e$^-$ (bright circles) capture. When this level is occupied, it is shifted down instantaneously and is capable of capturing h$^+$ (dark circles) from the silicon valence band.

interface deep into the dielectric. Hence, positive charges built up during the on-state are swept out again.

Taking the poly-gate interface into account, traps with long tunneling time constants situated far from the substrate interface do not participate in charge trapping. For these traps, the capture rate of gate e$^-$ outbalances the capture rate of substrate h$^+$. Hence, the presence of the poly-gate interface establishes a spatial border to the penetrating h$^+$ front. Only traps with small tunneling times are involved in charge trapping entailing an early saturation during the on-state and a fast erase of stored positive charges during the off-state.

Data of numerical simulations for the on-state and the off-state are depicted in Fig. 2 and 3. Fig. 2 clearly demonstrates the importance of accounting for the poly-gate interface in the on-state. As compared to the conventional Tewksbury model, the extended fixed level model yields an early saturation of the threshold voltage shift during the on-state. This saturation is reached at approximately 100 ms after the beginning of the on-state. While the off-state of the conventional Tewksbury's model covers many decades during the off-state, consideration of the poly-gate interface results in an early erase of trapped charges (see Fig. 3). A complete removal of trapped charges is already achieved after 1 s.

This behavior cannot explain NBTI measurements on thin oxide devices which yield long relaxation tails lasting for more than 10 s. Moreover, an earlier onset of trapping for higher voltages can be recognized in Fig. 2. This is originated in different regions of traps involved in charge trapping (see Fig. 4). For increasing voltage the trap levels are tilted upwards so that the ones situated at the same energy as the Fermi energy are located closer to the interface. These traps are associated with the earliest trapping events and the onset of charge trapping in the V_{th} transients. Simulations for traps centered 0.55 eV below

Table III

VALUES USED FOR THE LEVEL SHIFT MODEL WITH A NARROW TRAP DISTRIBUTION. THE PREFACTORS $v_{0,in}$ AND $v_{0,out}$ REFER TO THE TRAP LEVEL AT AN ENERGY E_{in} OR E_{out}, RESPECTIVELY. NO PREFACTORS $v_{0,if}$ ARE GIVEN SINCE NO TRAPPING FROM STATES WITHIN THE BANDGAP IS ASSUMED.

N_t	$3{\cdot}10^{18}$ cm^{-3}
E_{in}	-2.6 eV
Δ_{in}	0.2 eV
E_{out}	-5.0 eV
Δ_{out}	1.4 eV
$v_{0,in}$	$6.3{\cdot}10^{4}$ s^{-1} cm^3 eV
$v_{0,out}$	$6.3{\cdot}10^{-16}$ s^{-1} cm^3 eV
m_t	$0.5{\cdot}m_e$

the substrate valence band edge with a wide spread are presented in Fig. 5. One can recognize that charge trapping sets in at the same time point for different gate voltages. However, a saturation of charge trapping is still not remedied by the broad distribution of traps and occurs at approximately 100 ms after beginning of the on-state again.

IV. THE LEVEL SHIFT MODEL

In the following, we discuss the implications emerging from the level shift. A band diagram indicating the trapping and detrapping processes is given in Fig. 6. Within the framework of this model h$^+$ can only be injected into the e$^-$ emission levels (lower trap levels), while e$^-$ are only permitted to be captured by the e$^-$ capture levels (upper trap levels). Hence a situation arises where two opposite processes, namely h$^+$ capture and e$^-$ capture, compete and determine whether trapping or detrapping occurs. The magnitude of their rates is governed by their corresponding concentrations $n(E_{in})$ and $p(E_{out})$ which are primarily affected by the position of the Fermi level at the interface.

For comparison between the fixed level model and the level shift model, the same device geometry, doping concentrations, and trap concentration have been used as in the case of the fixed level model. The e$^-$ capture levels with only a small spread of 0.1 eV are assumed to be situated 0.5 eV above the silicon conduction band edge, while the h$^+$ capture levels cover a wide energetical range of more than 1 eV (see Table II). In contrast to the fixed level model, the level shift model does not require to take charge trapping from interface states into account. The different nature of e$^-$ capture levels and h$^+$ capture levels is reflected in their respective prefactors v_0 (in r_{in} and r_{out} of equation (4)). However, the values of v_0 for the substrate and for the poly-gate must coincide since both describe trapping between band states of silicon bulk and the same sort of traps.

Data for the on-state and the off-state are shown in Fig. 7 and Fig. 8, respectively. When the device is operated in inversion, the Fermi level falls below the silicon valence band so that e$^-$ injection into traps is impeded due to a lack of e$^-$ above the conduction band edge. On the other hand, the high h$^+$ concentration in the inversion layer gives rise to strong h$^+$ trapping. During the on-phase, the level shift model predicts charge trapping in the long timescales as it is found for NBTI (cf. Fig. 7). When returning to the off-state (cf. Fig. 8), the Fermi

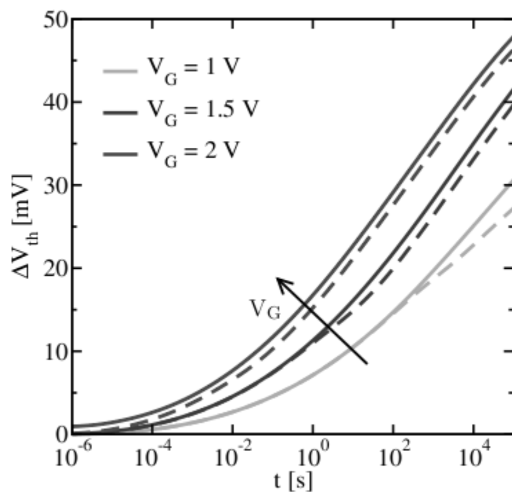

Fig. 7. The same as in Fig. 2 but for the level shift model. As in the fixed level model, the V_{th} transients shows that charge trapping sets in nearly simultaneously for different gate voltages. The simulations show that the influence of the poly-gate interface is of minor importance during the short-term part.

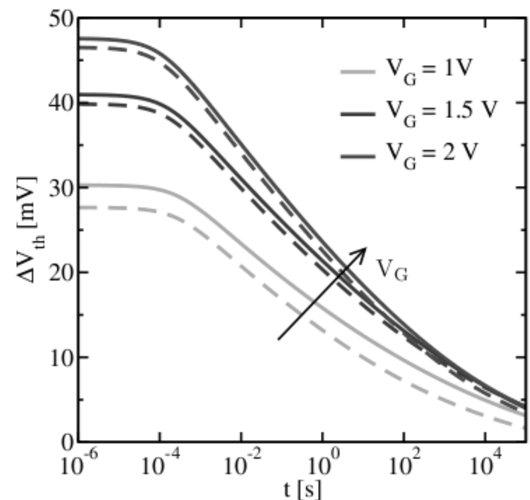

Fig. 8. The same as in Fig. 3 but for the level shift model. The V_{th} transients cover a wide range of decades in timescale.

level is situated above the silicon valence band accompanied by an increase of e^- injection into e^- capture levels and a vanishing h^+ injection into e^- emission levels. In contrast to the fixed level model, the V_{th} transient plotted in Fig. 8 shows an overlap only at the tails of the curves for different voltages. For the case where the poly-gate interface is accounted for, no remarkable changes can be observed (see Fig. 7). This can be traced back to a small upwards shift of the gate Fermi level which prefers e^- injection from poly-gate interface. The small amount of trapped e^- from the poly-gate interface during the on-state is removed during the off-state again. This yields a similar detrapping behavior during the off-state as depicted in Fig. 8 for the level shift model without consideration the poly-gate interface.

V. CONCLUSION

We have shown that the extended fixed level model based on Tewksbury's approach shows a saturation behavior at 1 s due to the impact of the poly-gate interface [13]. This can be traced back to the fact that only traps with short tunneling times are involved in charge trapping. For the first time, trap level shifts have been rigorously incorporated into a new model and yield V_{th} transients covering a several decades for the on-state as well as the off-state. Even for the case where a second interface is taken into account, theoretical results still cover the timescales of interest.

REFERENCES

[1] J.F Conley, P.M. Lenahan, ”Room Temperature Reactions Involving Silicon Dangling Bond Centers and Molecular Hydrogen in Amorphous SiO2Thin Films On Silicon”, IEEE Trans. Nucl. Sci., vol. 39, no. 6, pp. 2186-2191 (1992).

[2] J.P. Campbell, P.M. Lenahan, A.T. Krishnan, S. Krishnan, Atomic-Scale Defects Involved in NBTI in Plasma-Nitrided pMOSFETs, 2007 IEEE IIRW Final Report, 12, (2007).

[3] J.F. Zhang, C.Z. Zhao, A.H. Chen, G. Groeseneken, R. Degraeve, ”Hole Traps in Silicon Dioxides — Part I: Properties”, IEEE Trans. Electr. Dev., vol. 51, no. 8, pp. 1267-1273 (2004).

[4] A.J. Lelis, H.E. Bosch, T.R. Oldham, F.B. McLean, ”Reversibility of Trapped Hole Annealing”, IEEE Trans. Nucl. Sci., vol. 35, no. 6, 1186-1191 (1988).

[5] Y.L. Yang, M.H. White, Charge Retention of Scaled SONOS Nonvotatile Memory Devices at Elevated Temperatures, Solid-State Electronics, vol. 44, 949 (2000).

[6] D.S. Ang, S. Wang, Recovery of the NBTI-Stressed Ultrathin Gate pMOSFET: The Role of Deep-Level Hole Traps, IEEE EDL, vol. 27, no. 11, 914 (2006).

[7] V. Huard, M. Denais, F. Perrier, N. Revil, C. Parthasarathy, A. Bravaix, E. Vicent, ”A Thorough Investigation of MOSFETs NBTI Degradation”, Microelectronics Reliability 45, 83-98 (2005).

[8] T.L. Tewksbury, ”Relaxation Effects in MOS Devices due to Tunneling Exchange with Near-Interface Oxide Traps”, doctor thesis, 1992, Massachusetts Institute of Technology.

[9] P.E. Blöchl, ”First-Principles Calculations of Defects in Oxygen-Deficient Silica Exposed to Hydrogen”, Phys. Rev. B, vol. 62, no. 10, pp. 6158-6179 (2000).

[10] W. Goes, T. Grasser, First-Principles Investigations on Oxide Trapping, SISPAD Proceedings 2007, 157-160 (2007).

[11] W. Goes, T. Grasser, Charging and Discharging of Oxide Defects in Reliability Issues, 2007 IEEE IIRW Final Report, 27, (2007).

[12] M. Karner, A. Gehring, S. Holzer, M. Pourfath, M. Wagner, W. Goes, M. Vasicek, O. Baumgartner, Ch. Kernstock, K. Schnass, G. Zeiler, T. Grasser, H. Kosina, S. Selberherr, "A Multi-Purpose Schrödinger-Poisson Solver for TCAD Applications", Journ. Comp. Electron., vol. 6, pp. 179-182 (2007)

[13] A.E. Islam, H. Kuflouglu, D. Varghese, S. Mahapatra, M.A. Alam, Recent Issues in Negative-Bias Temperature Instability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects, and Relaxation, IEEE TED, vol. 54, no. 9, 2143 (2007).