

Possible Correlation between Flicker Noise and Bias Temperature Stress

Paul-Jürgen Wagner*, Thomas Aichinger†, Tibor Grasser*,
Michael Nelhiebel† and Lode K. J. Vandamme**

* Christian Doppler Laboratory for TCAD in Microelectronics, Institute for Microelectronics,
Technische Universität Wien, 1040 Wien, Austria

† Kompetenzzentrum für Automobile und Industrielektronik, 9524 Villach, Austria

** Department of Electrical Engineering, Eindhoven University of Technology,
5600 MB Eindhoven, The Netherlands

Abstract. A link between Bias Temperature Stress (BTS, NBTI) and flicker noise ($1/f$ -noise) is explored by comparing flicker noise data to charge pumping data. Large-area devices are shown to initially have very low, bias independent normalized flicker noise. After BTS the normalized noise increases considerably and becomes gate bias dependent. Small-area devices are shown to exhibit bias dependent burst noise (RTS) in addition to flicker noise, regardless of BTS.

Keywords: Reliability, MOSFET, BTS, NBTI, charge pumping, flicker noise

PACS: 85.30.Tv, 85.40.Qx

INTRODUCTION

When subjected to strong-inversion bias and high temperatures, the drain current of MOSFETs degrades, a phenomenon known as *Bias Temperature stress (BTS)*. The drain current degradation is often described as an increase of the threshold voltage, but other parameters, foremost the carrier mobility and the sub-threshold slope, degrade as well. The exact physical mechanism responsible for BTS are still controversial, but there is ample evidence that both interface states, possibly created by breaking the bonds of passivating hydrogen [1], and oxide traps play a role [2].

Since flicker noise has been used as a diagnostic tool in various places before [3, 4], we conducted a series of flicker noise measurements on MOSFETs that previously experienced BTS degradation. To assess the amount of degradation, the increase in interface state density was monitored using charge pumping measurements [5].

METHODOLOGY

The devices measured were pMOSFETs with $W/L = 50\mu\text{m}/10\mu\text{m}$ and $t_{\text{ox}} = 30\text{nm}$. We studied three wafers that differed only in the back-end-of-line processing, described in [6]. One process variant resulted in a high initial interface trap density $N_{\text{it}0}$, but showed a comparatively low increase ΔN_{it} after BTS; this wafer is referred to as wafer A. Wafer B had both medium initial interface traps and medium increase of traps after BTS. The third wafer (C) exhibited a high ΔN_{it} , resulting in the highest post-stress interface state

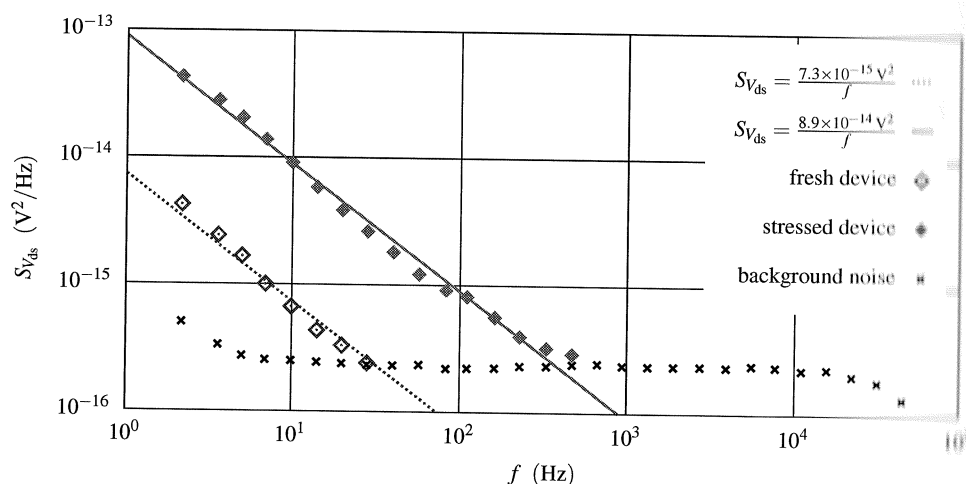


FIGURE 1. Noise spectrum of a large-area MOSFET (wafer C) biased at $V_{gs} = -1.54$ V before and after BTS and respective least-squares fits. The crosses show the background noise ($I_d = 0$).

density, despite the fact that this wafer's initial interface state density was lowest. On every wafer at least two neighbouring devices were measured using constant-baselevel charge pumping at 2MHz [71]. Next, on every wafer one device was stressed for 10^3 s at $V_{gs} = -17.5$ V and 175°C , and charge pumping was done again immediately upon release of stress.

Then, noise measurements were performed in the linear region of the MOSFETs ($|V_{ds}| < 0.3$ V) at gate voltages $V_{gs} = -1.54$ V, -3.07 V, -4.59 V. Figure 1 depicts the spectra for a fresh and a stressed device at weak inversion. Although the bias point is approximately the same, the noise power density is tenfold for the stressed device. Prior to the noise measurements, the $I_d(V_{gs})$ -characteristic of a fresh device was measured, and the SPICE level-1 model was fitted yielding the parameters $V_t = -0.95$ V, $\beta = 1.23 \times 10^{-4}$ A/V², and $\theta = 0.128$ V⁻¹.

In addition to the large-area transistors, small-area transistors with $W/L = 2.4\mu\text{m}/2.6\mu\text{m}$ were examined. Figure 2 shows that with these devices the noise is not conveniently described by a pure $1/f$ -dependence. Because of the smaller number of free carriers the Lorentzians of distinct traps may be visible, and their superposition yields $1/f^\gamma$ -noise with γ appreciably deviating from unity, as predicted by the criterion $N < 1/(4\pi\alpha)$ in [8].

Using the empirical relation [9]

$$\left. \frac{S_{V_{ds}}}{V_{ds}^2} \right|_{I_d=\text{const}} = \left. \frac{S_{I_d}}{I_d^2} \right|_{V_{ds}=\text{const}} = \frac{S_{r_{ds}}}{r_{ds}^2} = \frac{\alpha}{Nf}, \quad (1)$$

an α was calculated for every device at every bias by taking $f_0 S_{V_{ds}}(f_0)/V_{ds}^2$ at $f_0 = 10\text{ Hz}$. Care was taken to verify a $1/f$ -dependence of $S_{V_{ds}}$ around f_0 , which was the case for all large-area transistors. Assuming a homogeneous channel, the number of carriers in

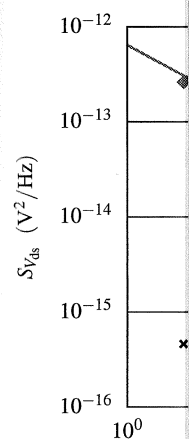


FIGURE 2. Noise does not deviate from the $1/f^2$ -spectrum. The situation is changed in the time domain.

the channel N
resistance at V_{ds}
from the SPICE

The fresh device dependent on the gate devices exhibited that moreover the devices was up and stressed de

Since the con-
mobility μ , ass-
 $\alpha_\mu + \alpha_N$. In a
are negligible, l-
(fresh) devices
effect. Continui-
 $\Delta\alpha$ is the flicke-
McWhorter the-

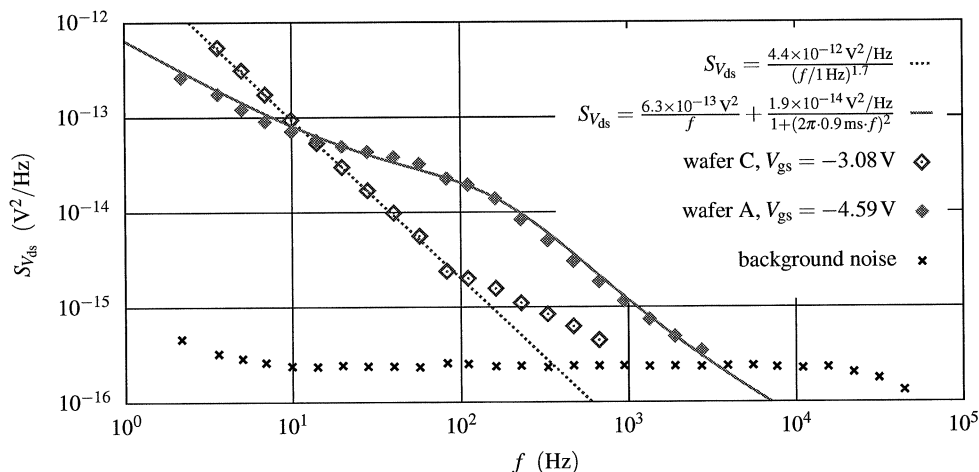


FIGURE 2. Noise spectra of small-area MOSFETs (unstressed) for different biases. The spectra clearly deviate from the $1/f$ -form: One can partly be fitted with a much higher slope, thus more resembling a $1/f^2$ -spectrum. The other one can be fitted by a superposition of a 'true' $1/f$ -component and a Lorentzian. This situation is characteristic for the presence of a single dominant trap. These traps were also visible in the time domain.

the channel N was obtained via $N = L^2/(\mu q r_{ds})$, where r_{ds} is the (measured) channel resistance at $V_{ds} \approx 0$, q the elementary charge, and the carrier mobility μ was calculated from the SPICE model parameter β .

RESULTS

The fresh devices showed very low α values around 10^{-6} that were only weakly dependent on the gate voltage. The values were quite similar for all three wafers. The stressed devices exhibited considerably higher noise power, corresponding to higher α values, that moreover turned out to be bias dependent: For weak inversion, α of the stressed devices was up to ten times the value of the fresh ones, where at strong inversion fresh and stressed devices had comparable α values, cf. Figure 3.

Since the conductivity is proportional to the product of carrier number N and carrier mobility μ , assuming that both N and μ fluctuate *independently* allows to split $\alpha = \alpha_\mu + \alpha_N$. In a first order approximation, mobility reduction and parasitic resistances are negligible, hence α_μ is *independent of gate bias*. It seems likely that the unstressed (fresh) devices just show this kind of flicker noise, i.e. $\alpha_f = \alpha_\mu$, which is a bulk noise effect. Continuing with this interpretation, for stressed devices $\alpha_N = \alpha - \alpha_\mu = \alpha_s - \alpha_f = \Delta\alpha$ is the flicker noise component due to carrier number fluctuations. According to the McWhorter theory, $\alpha_N \propto 1/V_g^*$, as nicely confirmed by Figure 3.

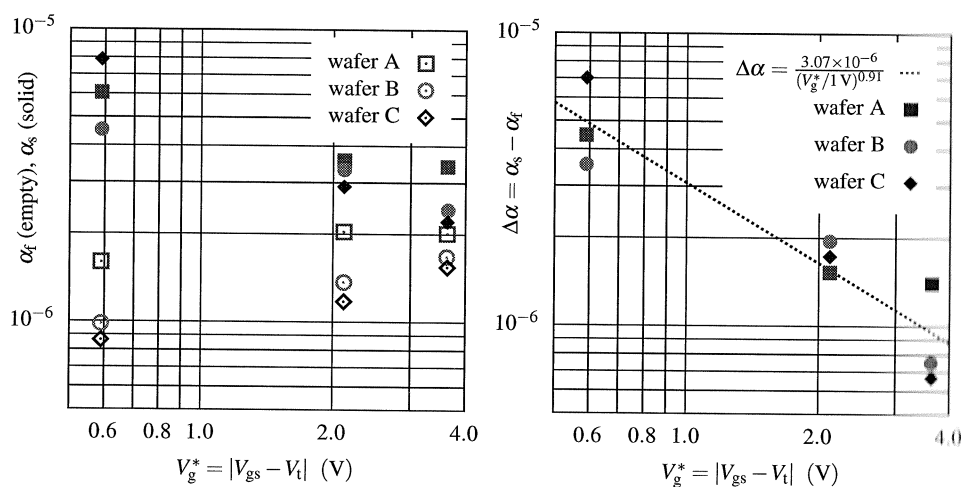


FIGURE 3. Left: Dependence of calculated α values on the effective gate voltage (empty symbols: fresh devices; solid symbols: stressed devices). Right: Increase of α due to BTS, and least squares fit to the data, indicating $\Delta\alpha \propto 1/V_g^*$.

CONCLUSIONS

The low-frequency noise behaviour of large-area pMOSFETs subjected to bias temperature stress was investigated. Unstressed devices showed very low and gate bias independent α values around 10^{-6} , pointing to a bulk origin for the flicker noise in these devices. After BTS, the devices showed considerably increased, gate bias dependent α values, indicating that in competition with the bulk mobility noise, a surface-provoked noise component of the McWhorter type emerges.

REFERENCES

1. K. Jeppson, and C. Svensson, *Journal of Applied Physics* **48**, 2004–2014 (1977).
2. V. Huard, M. Denais, and C. Parthasarathy, *Microelectronics Reliability* **46**, 1–23 (2006).
3. J. Scofield, T. Doerr, and D. Fleetwood, *IEEE Transactions on Nuclear Science* **36**, 1946–1953 (1989).
4. X. Li, and L. K. J. Vandamme, *Solid-State Electronics* **35**, 1477–1481 (1992).
5. G. Groeseneken, H. Maes, N. Beltran, and R. de Keersmaecker, *IEEE Transactions on Electron Devices* **ED-31**, 42–53 (1984).
6. M. Nelhiebel, J. Wissenwasser, T. Detzel, A. Timmerer, and E. Bertagnolli, *Microelectronics Reliability* **45**, 1355 – 1359 (2005).
7. T. Aichinger, and M. Nelhiebel, *IEEE Integrated Reliability Workshop 2007 Final Report* pp. 63–69 (2007).
8. L. Vandamme, and F. Hooge, *IEEE Transactions on Electron Devices* **55**, 3070–3085 (2008).
9. F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, *Reports on Progress in Physics* **44**, 479–532 (1981).