Ultra-scaled Z-RAM cell

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Abstract

Ultra-scaled Z-RAM cells based on MuGFETs are demonstrated for the first time. Effects of physical parameters such as channel doping concentration, fin width, and gate length on Z-RAM cell performance are discussed. Transient measurements and simulations prove that the basic operational principles are effective on Z-RAM cells with a gate length down to 12.5 nm.

Introduction

Multiple-gate MOSFETs (MuGFETs) are very promising devices for deep submicron CMOS applications as they push silicon integration beyond the limits of classical planar technologies [1]. MuGFET devices have been drawing considerable attention in recent years. Z-RAM memory [2] uses a single transistor (1T) and no capacitor bitcell (hence the "Z" for Zero capacitor RAM), unlike traditional one transistor plus one capacitor (1T/1C) DRAM bitcells. In this work we demonstrate ultra-scaled Z-RAM cells based on MuGFETs, thus extending the Z-RAM roadmap to future DRAM generations.

Results and discussion

Figure 1 shows a Z-RAM memory cell. The transistor's Floating Body (FB) acts as a storage node. Z-RAM is based on the Bipolar Junction Transistor (BJT) present in the MOS structure. In the case of an n-channel device the N^+ source, the P-type body, and the N^+ drain form the emitter, the base, and the collector of an NPN bipolar transistor. In a FB SOI device the body (*i.e.* the base of the bipolar transistor) is used as a storage node. Both writing and reading use bipolar current. Z-RAM provides high margin and does not require any back gate bias and thin BOX unlike other FBC concepts [3, 4]. An important advantage of Z-RAM is its applicability to non-planar devices such as MuGFETs (Figure 2).

Unibond SOI wafers with a 60 nm top silicon layer and a 150 nm buried oxide were used to build the MuGFETs (Figure 3). Fins down to 11 nm were patterned and a 1.8 nm gate oxide was grown by wet oxidation. To form the gate metal stack, a 6 nm thick TiSiN gate layer was deposited on the gate oxide. The initial doping concentration was $2x10^{15}$ cm^{-3}. Some devices were doped by boron implantation to reach a concentration of $2x10^{18}$ cm^{-3}. The effective channel length is down to 50 nm.

Z-RAM cell operation was extensively studied using MINIMOS-NT and ATLAS 2-D numerical simulators. An example of the simulated impact ionization rate for doped and undoped devices is shown on Figure 4. To experimentally investigate Z-RAM operation, transient measurements where performed. Figure 5 shows the cell current during write and read. Even an undoped cell with an 11 nm fin shows nice digital behavior and a good margin (Figure 6). Without any device optimization a retention time close to 1 ms at 125°C was measured (Figure 7). Reliability measurements (Figure 8) do not show any decrease of the cell current during aging. Figure 9 presents the cell programming window measured on a 1-fin MuGFET. Given the limited data on the sub 100 nm devices, this work presents the highest programming window yet reported (Figure 10).

To evaluate Z-RAM scalability (even further down) we performed simulations of an extremely small device with L=12.5 nm and fin width of 3 nm (Figure 11). Even such a small device demonstrates a reliable memory effect, and indicates an excellent Z-RAM scalability. We believe that these transistors are the smallest silicon dynamic memory devices ever published.

Conclusion

We demonstrated ultra-scaled Z-RAM cells based on MuGFETs built with a logic process. Z-RAM operation is proven on both doped and undoped devices. Effects of physical parameters such as fin width and gate length on Z-RAM cell performance are discussed. Simulations and transient measurements prove excellent Z-RAM scalability.

References

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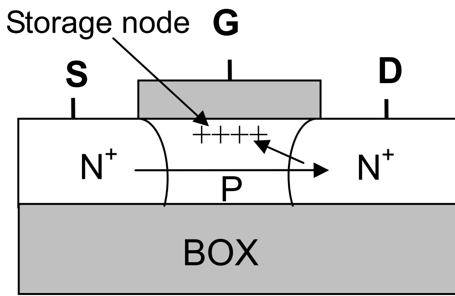

Fig. 1 Z-RAM memory cell

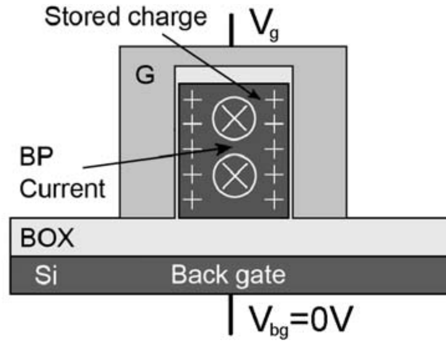

Fig. 2 Z-RAM MuGFET cross-section

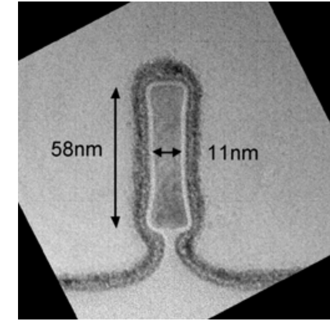

Fig. 3 Cross-section of MuGFET fin

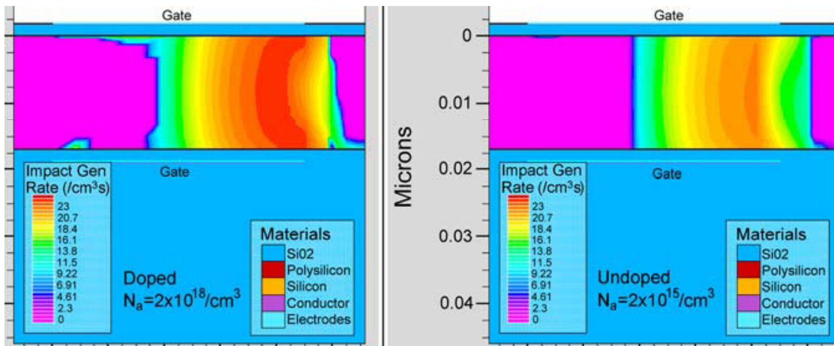

Fig. 4 Simulated impact generation rate in doped and undoped devices with the fin width of 17nm and length of 45 nm at Vds=1.5V and Vgs=0V

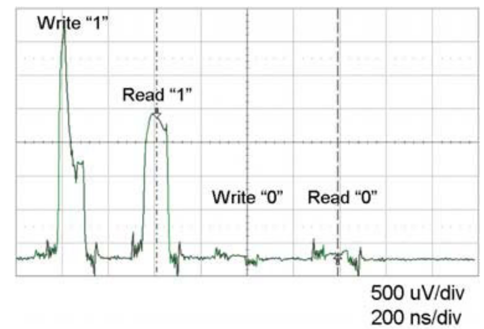

Fig. 5 Cell current measured during cell operation for device with the fin length of 55 nm, and width of 11 nm

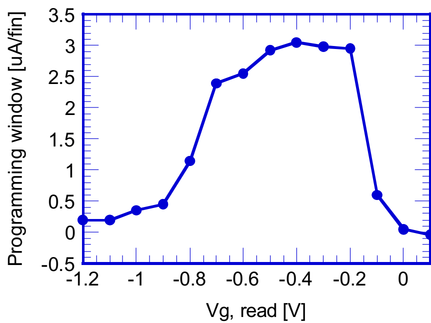

Fig. 6 Measured programming window for a MuGFET with fin width of 11 nm and gate length of 50 nm

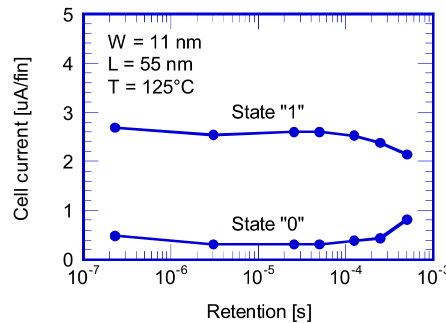

Fig. 7 Retention measured at 125°C on undoped device

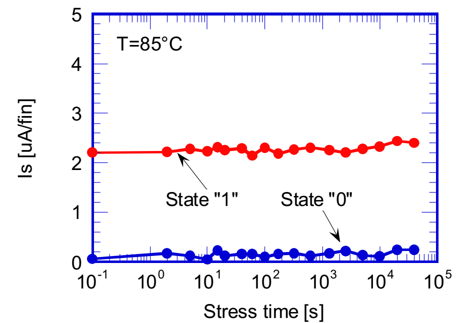

Fig. 8 "1"and "0" cell currents, measured during aging on a MuGFET with fin width of 11 nm and gate length of 55 nm

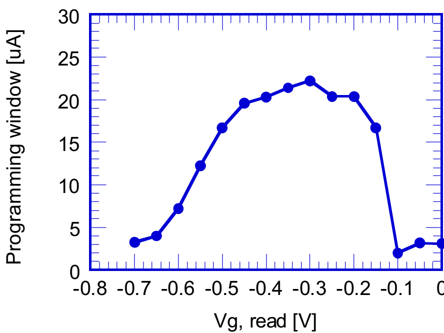

Fig. 9 Measured programming window for a 1-fin MuGFET with fin width of 31 nm and gate length of 55 nm

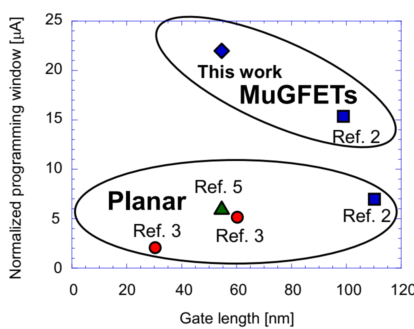

Fig. 10 Experimental programming window data on FBC devices. For planar devices it is normalized per cell (W=70nm)

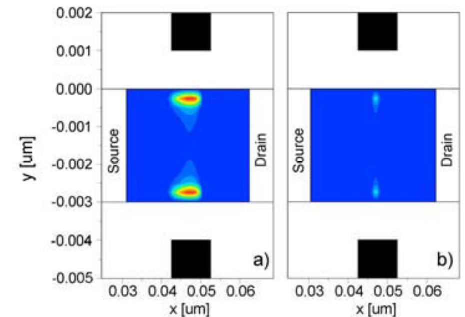

Fig. 11 Simulated hole concentration along the fin in states "1" (a) and "0" (b) for 12.5 nm Z-RAM device

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